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Design, development and verification of a new multilevel inverter for reduced power switches

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Abstract: Due to recent developments in the field of high-power and medium-voltage, the multilevel inverter has raised to such an extent owing to some of its amazing facts regarding harmonic spectrum, ease in control, reduced electromagnetic interference (EMI), filterless circuit, stress on power switches, common-mode voltage. This paper well describes a novel architecture of a single-phase multilevel inverter using a lesser number of overall components, especially the power switches. The proposed topology is generalized in the structure that can generate any number of voltage steps. A 7-level structure of the proposed topology is explained and is elaborately discussed. Simulation is carried out in MATLAB and corresponding experimental results verify the existence of the proposed multilevel inverter. The real-time experimental results were presented and are well verified by the simulation results for 7-level as well for 13-level across RL-Load. The nature of load current is also indicated as per the nature of load voltage. Nevertheless, the topology is further compared with some of the recent literature and found superior in each respect.

Key words: 7-level/13-level inverter, DC-AC converters, power-electronic switches, sinusoidal PWM

1. Introduction

The multilevel inverter (MLI) is a power electronic device introduced in the year 1981, being the most emerging topic of research that produces arbitrary voltage output waveform with consuming required DC sources and power switches. The desired voltage at the output is attained by applying a particular switching arrangement on the available power switches [1]. The undesirable harmonics in the output voltage and current waveforms are not eliminated in the traditional inverters resulting in excessive power loss [2, 3]. Some of the foremost applications of MLIs are in flexible AC transmission systems (FACTs) [4], renewable energy systems [5], electric drives [6], and active filters [7]. The basic and most renowned multilevel inverters are: neutral-point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) [8]. This above-mentioned technology can generate the output voltage with higher power quality, lower total harmonic distortion (THD), and a lower electromagnetic interface [9]. Further, MLI configurations are categorized as symmetrical and asymmetrical configurations depending on the magnitudes of DC sources [10] whereas symmetrical configuration of MLIs comprises DC sources of equal magnitudes and asymmetrical configuration of MLIs comprises DC sources of unequal magnitudes. A treaty lies between both the configurations (symmetrical and asymmetrical DC sources) that the asymmetrical MLI stands better in terms of generated voltage levels for the same number of required power switches whereas symmetrical MLI stands better in terms of a variety of required DC sources. The quantity of power switches and DC sources is the soul to achieve a sinusoidal waveform. An increase in the number of power switches is considered one of the key disadvantages of multilevel inverters as it reflects in cost enhancement and complexity in control thus reducing the overall reliability. However, the possibility of the occurrence of the fault between the power switches is increasing day by day where 21% of faults arise in power semiconductor switches and faults in the module include 34% of total failures in a converter system [11].

Reduced components MLI inverter is thereby introduced by researchers to generate voltage levels and keep trying to reduce the power switches. Both the symmetric and asymmetric values of DC sources are executed for the proposed topology. A 7-level symmetrical and 13-level asymmetrical value of DC sources is designed and tested in a MATLAB environment. Nevertheless, an experimental setup is designed and executed in the laboratory. Simulation results are obtained through MATLAB and are then verified by the corresponding experimental results considering RL-Load. In addition, various recent topologies suggested in [12–21] are compared with the proposed topology having the best asymmetric voltage ratio (1:2:4), and hence can be increased similarly. The limitation of the proposed topology is many required DC sources.

2. Proposed topology

Figure 1(a): the proposed MLI, as shown in, is generalized and thus it can generate levels as per the requirement of the application. Units are added, as shown in Fig. 1(a), to generate higher voltage levels in the output. One DC source with two power switches is required for a unit. Figure 1(b) shows the proposed topology that can generate 7-level/9-level/11-level/13-level/15-level using different values of DC sources and this structure can be further extended by adding the aforementioned units. Unit-1 contains two power switches (S_{11} and S_{12}) and one

DC source (V_1). Unit-2 contains two power switches (S_{21} and S_{22}) with one DC source (V_2). Unit-3 contains two power switches (S_{31} and S_{32}) with one DC source (V_3). Unit-n contains two power switches (S_{n1} and S_{n2}) with one DC source (V_n). A noticeable point shows that there are only two switches (S_x and S'_x) with a DC source (V_x) needed instead of an H-bridge where V_x is the addition of the total voltage in units. All the power switches employed in the entire circuit are unidirectional.

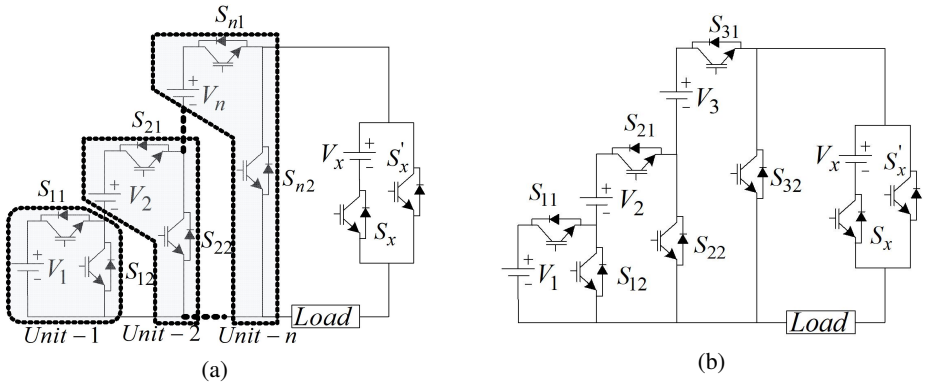


Fig. 1. Generalized structure of proposed topology (a); proposed topology with different voltage-levels (b)

(i) 7-level

$$V_1 = V_2 = V_3 = V_{\mathrm{dc}}\,, \quad V_x = 3V_{\mathrm{dc}}\,, \tag{1}$$

(ii) 9-level

$$V_1 = V_{\mathrm{dc}}\,, \quad V_2 = V_{\mathrm{dc}}\,, \quad V_3 = 2V_{\mathrm{dc}}\,, \quad V_x = 4V_{\mathrm{dc}}\,, \tag{2}$$

(iii) 11-level

$$V_1 = V_{\mathrm{dc}}\,, \quad V_2 = 2V_{\mathrm{dc}}\,, \quad V_3 = 2V_{\mathrm{dc}}\,, \quad V_x = 5V_{\mathrm{dc}}\,, \tag{3}$$

(iv) 13-level

$$V_1 = V_{\mathrm{dc}}\,, \quad V_2 = 2V_{\mathrm{dc}}\,, \quad V_3 = 3V_{\mathrm{dc}}\,, \quad V_x = 6V_{\mathrm{dc}}\,, \tag{4}$$

(v) 15-level

$$V_1 = V_{\mathrm{dc}}\,, \quad V_2 = 2V_{\mathrm{dc}}\,, \quad V_3 = 4V_{\mathrm{dc}}\,, \quad V_x = 7V_{\mathrm{dc}}\,. \tag{5}$$

The magnitude of voltage sources can be set as symmetrical as well as asymmetrical. The attractiveness of the proposed MLI structure confirms its operation for the binary ratio, i.e., $1{:}2{:}4{:}8{:}\ldots{:}2^{N_{\mathrm{dc}}-1}$, where N_{dc} symbolizes the number of DC sources. For example, 3–level output voltage is offered with one unit consisting of one DC source ($V_1 = V_{\mathrm{dc}}$), where V_x is a DC source with a total magnitude of DC source ($V_x = V_{\mathrm{dc}}$). In addition, further next unit (Unit-2) having one DC source ($V_2 = 2V_{\mathrm{dc}}$) is added in addition to the earlier DC source ($V_1 = V_{\mathrm{dc}}$) of Unit-1. The magnitude of the DC source, $V_x = 3V_{\mathrm{dc}}$ changes magnitude with the addition of each unit. Next to 3-level, 7-level, 15-level, 31-level, and so on, voltage levels are obtained with every time change in magnitude of DC source i.e., $V_x = 3V_{\mathrm{dc}}$, $V_x = 7V_{\mathrm{dc}}$, $V_x = 15V_{\mathrm{dc}}$, $V_x = 31V_{\mathrm{dc}}$ and so on respectively.

3. Modes of operation

The approach of the controller for the MLI proposed in this paper is the pulse width modulation (PWM) technique. In this simple and well-defined technique, triangular carriers are chosen, and a reference sine signal is compared to produce the corresponding pulse pattern of the power switches. Level-shifted PWM (LS-PWM) is chosen among some of the well-known control strategies, i.e., phase-shifted PWM [18], nearest-level control (NLC) [19], selective harmonic elimination (SHE) [20], LS-PWM [21], [22–25] to cultivate the pulses in MATLAB.

The PWM method generates several pulses with varying ON and OFF time duration or duty cycle such that the average value of the voltage over a half-cycle is varying sinusoidally. In order to obtain a suitable duty cycle for each switch, many modulation methods have been developed for the voltage source inverter (VSI). On the other hand, for the MLI, the lower-order harmonic components can be suppressed by increasing the number of the inverter voltage levels. Thus, for an MLI, a lesser switching frequency is usually preferred to lower the switching losses and improve efficiency. Figure 2 shows two popular modulation schemes and their corresponding output voltage or switching patterns. The level-shifted PWM (LS-PWM) technique is a high-frequency carrier-based PWM technique that generates a staircase voltage with a PWM pulse pattern, as observed from Fig. 2. This high-frequency PWM technique provides good harmonic profiles of the output voltage for an MLI with comparatively lesser voltage levels. The real-time simulator, dSPACE-1103 is used to produce the real-time pulses. Nevertheless, the switching pulses and switching table for the proposed inverter (symmetrical 7-level) are merged as well in Table 1. Pulse patterns obtained from the simulation as well as experimental results are shown in Fig. 3, respectively.

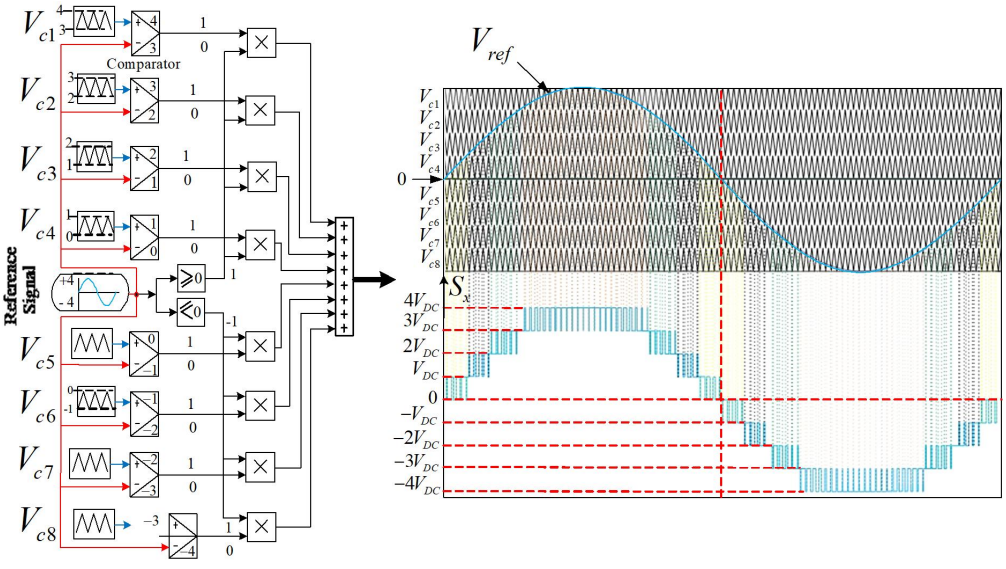


Fig. 2. Modulation of an MLI using SPWM technique for a 9-level inverter and its corresponding switching pattern

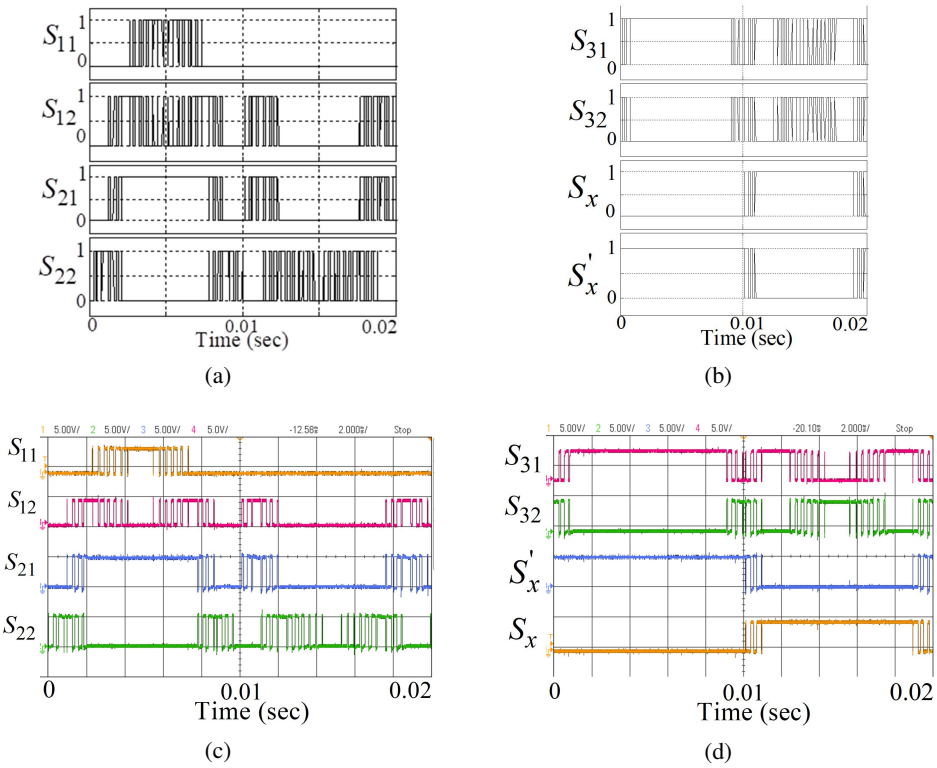


Fig. 3. Switching pulses of the power switches: S_{11}, S_{12}, S_{21} and S_{22} for simulation (a); S_{31}, S_{32}, S_x and S'_x for simulation (b); S_{11}, S_{12}, S_{21} and S_{22} for experimental (c); S_{31}, S_{32}, S_x and S'_x for experimental (d)

Mode 1: Power switches S_{11}, S_{21}, S_{31}, and S'_x are switched ON along with the three DC sources $V_1 = 38$ V, $V_2 = 38$ V, and $V_3 = 38$ V generate +114 V, i.e., $+3V_{\text{dc}}$.

Mode 2: Power switches S_{21}, S_{31}, S_{12}, and S'_x are switched ON along with the two DC sources $V_2 = 38$ V and $V_3 = 38$ V generating +76 V, i.e., $+2V_{\text{dc}}$.

Mode 3: Power switches S_{22}, S_{31}, and S'_x are switched ON along with only one DC source $V_3 = 38$ V generates +38 V, i.e., $+V_{\text{dc}}$.

Mode 4: Power switches S_{32} and S'_x are switched ON along with no DC source generating 0 V, i.e., zero.

Mode 5: Power switches S_{12}, S_{21}, S_{31}, and S_x are switched ON along with three DC sources, $V_2 = 38$ V, $V_3 = 38$ V, and $V_x = 114$ V generate –38 V, i.e., $-V_{\text{dc}}$.

Mode 6: In this mode, power switches S_{22}, S_{31}, and S_x are switched ON along with the two DC sources $V_3 = 38$ V and $V_x = 114$ V generating –76 V, i.e., $-2V_{\text{dc}}$.

Mode 7: Power switches S_{32} and S_x are switched ON along with only one DC source, $V_x = 114$ V generates –114 V, i.e., $-3V_{\text{dc}}$.

Generation of the different voltage steps at different modes for the 7-level inverter has been addressed below and is portrayed in Fig. 4.

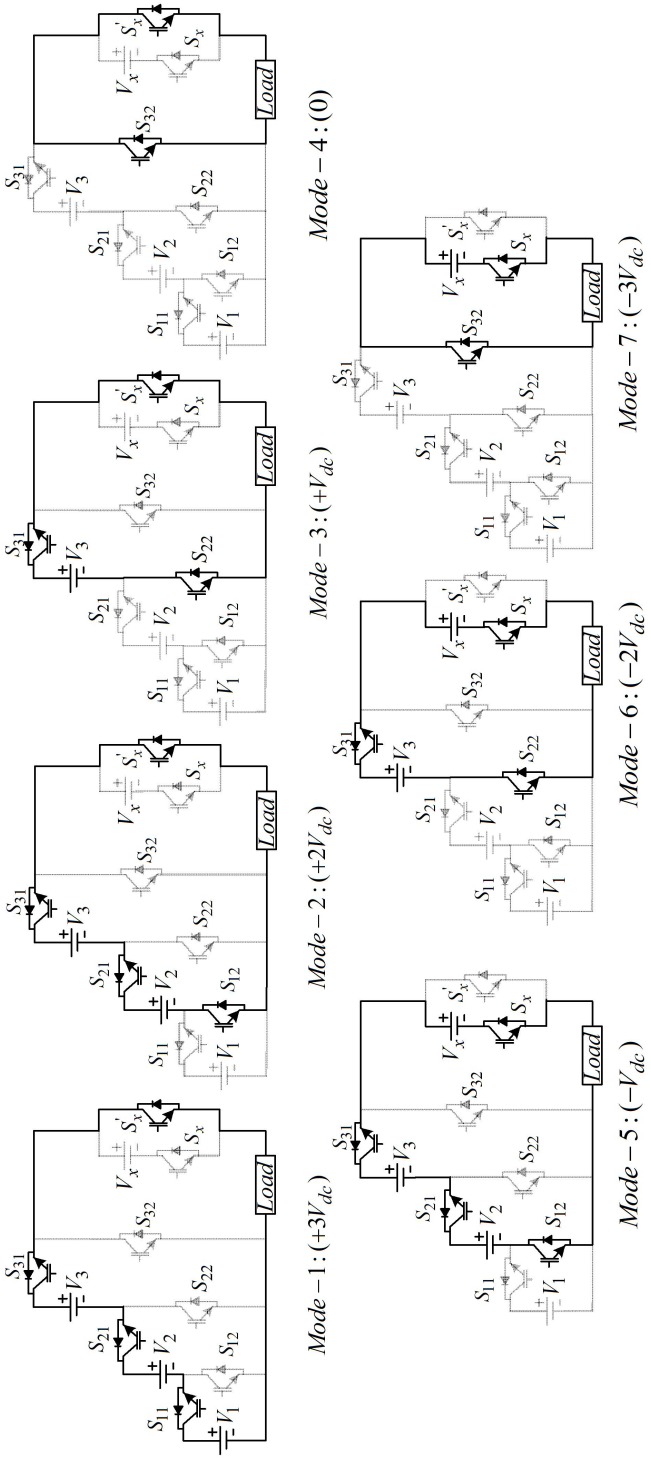


Fig. 4. Modes of operation

Table 1. Switching table for proposed 7-Level MLI ($V_1 = V_2 = V_3 = V_{dc}$) symmetrical

Conducting switches status: 1 = ON; 0 = OFF								**Voltage levels**
S_{11}	S_{12}	S_{21}	S_{22}	S_{31}	S_{32}	S_x	S'_x	
1	0	1	0	1	0	0	1	$+3V_{dc}$
0	1	1	0	1	0	0	1	$+2V_{dc}$
0	0	0	1	1	0	0	1	$+V_{dc}$
0	0	0	0	0	1	0	1	0
0	1	1	0	1	0	1	0	$-V_{dc}$
0	0	0	1	1	0	1	0	$-2V_{dc}$
0	0	0	0	0	1	1	0	$3-3V_{dc}$

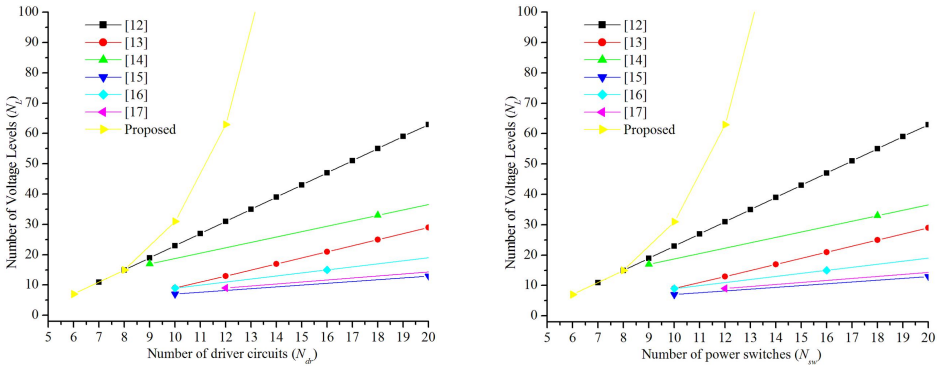
4. Comparison with new topologies

The generalized formulae are derived for all the required components i.e., a total number of DC sources (N_{dc}), power switches (N_{sw}), uni-directional switches (N_U), bi-directional switches (N_B) of the discussed topology are accorded with all the parameters of topologies studied in [12–17] that have been listed in Table 2. A comparison of the required components for the proposed MLI topology is made for the voltage ratio of 1:2:4:8.

Table 2. Generalized formulae of the required components for recently compared topologies and the proposed topology

Types of MLI	**Components count**			
	(N_L)	(N_B)	(N_U)	(N_{dc})
[12]	$(4N_{sw} - 17)$	$N_{sw} - 6$	6	$N_{sw} - 3$
[13]	$(2N_{sw} - 11)$	*NA*	N_{sw}	$N_{sw} - 6$
[14]	$(16N_{sw} + 9)/9$	$N_{sw}/3$	$2N_{sw}/3$	$4N_{sw}/9$
[15]	$(3N_{sw} + 4)/4$	*NA*	N_{sw}	$3N_{sw}/8$
[16]	$(N_{sw} - 1)$	*NA*	N_{sw}	$(N_{sw} - 2)/2$
[17]	$(2N_{sw} + 3)/3$	*NA*	N_{sw}	$N_{sw}/4$
Proposed	$[2^{(N_{sw}/2)} - 1]$	*NA*	N_{sw}	$(N_{sw} - 2)/2$

Besides, the graph is plotted (Fig. 5) between voltage levels (N_L) against the power switches (N_{sw}) as well as driver circuits (N_{dr}). Thus, it is concluded that the reduced power switches reduce the driver circuits thereby reducing maintenance for the circuit, easier to implement, lower cost, and less complex.



(a) (b)

Fig. 5. Graph showing the comparison b/w proposed MLI and other existing MLIs: N_L versus N_{dr} (a); N_L versus N_{sw} (b)

5. Simulation and experimental results

Figure 6 schematically explains the experimental set-up of the proposed 13-level inverter.

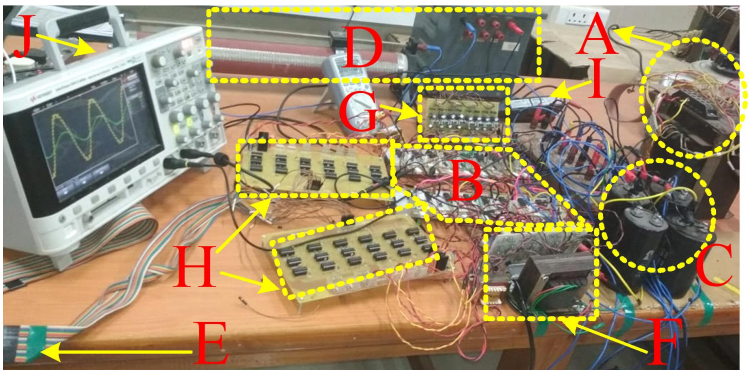


Fig. 6. Experimental set-up of the proposed 13-level inverter consists of: **A** – transformer (220 V/5 A) and rectifier capacitor based DC source; **B** – IGBT-based 13-level MLI with driver ICs; **C** – electrolytic capacitors (400 V, 4700 µF); **D** – R–L load (R = 60 Ω and L = 100 mH); **E** – flat ribbon cable from DS1103 connector; **F** and **G** – isolated supply for driver ICs (220 V/20 V, 500 mA) and delay circuit (220 V/5 V); **H** – delay circuit board; **I** – current probe (1146B, 100 kHz/100 A) and **J** – DSO-X 2024A

The inverter circuit is constituted of:

a) a single 1:1 isolation transformer rated at 220 V/5 A, 50 Hz (supplied from an auto-transformer connected to the primary, and a rectifier-capacitor arrangement connected at the secondary),

b) proposed 13-level inverter circuit constituting of 8 numbers of IGBT switches and gate drivers mounted on the heat sink,

c) four electrolytic capacitors for the 13-level inverter (two electrolytic capacitors for the basic 9-level module) individually rated at 400 V, 4 700 μF,
d) R–L load with R = 60 Ω and L = 100 mH,
e) flat ribbon cable connectors for fetching gate pulses from the connector of DS1103 based controller,
f) two numbers of 220 V/20 V, 500 mA isolation transformer for 8 numbers of gate driver power supply for the 13-level inverter and a single 220 V/20 V isolation transformer used for supplying 8 numbers of gate drivers for the proposed 9-level inverter,
g) rectifier, capacitor and linear voltage regulator (LM series) connected at the secondary of the individual 220 V/20 V transformer (used for gate drivers) for generating constant +20 V DC supply to the gate drivers,
h) external delay circuit board used to provide delayed pulses to the gate drivers to avoid short circuiting of IGBT switches, the delay used is 2 μs,
i) an extra 220 V/5 V isolation transformer with rectifier filter arrangement is required to provide +5 V DC power supply for proper functioning of the digital ICs used in the external delay board and also to protect the digital ICs from the 220 V power supply voltages,
j) four channel DSO-X 2024A from KEYSIGHT used for calibrating various results obtained from the 7-level/13-level SC-MLI.

The Proposed MLI for symmetric voltage (7-Level inverter) is developed and being tested in a MATLAB environment with the DC sources of magnitude as 38 V, i.e., $V_1 = V_2 = V_3 = V_{dc}$ = 38 V and V_x = 114 V. Thus, the peak voltage of output (maximum) is +114 V and the peak voltage of output (minimum) is –114 V. The simulation is then carried out with RL-Load, R = 170 Ω, L = 100 mH. The results of voltage and current (load) are presented for 5-cycles and 2.5-cycles as represented in Figs. 7(a) and 7(b), respectively.

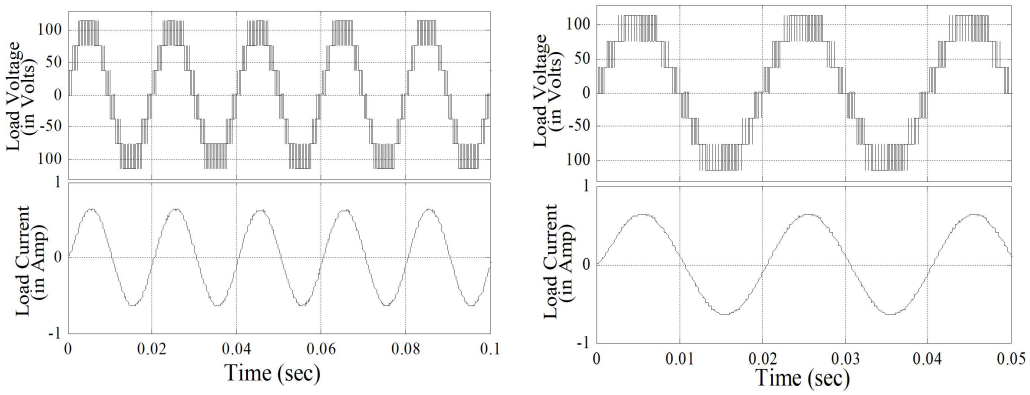
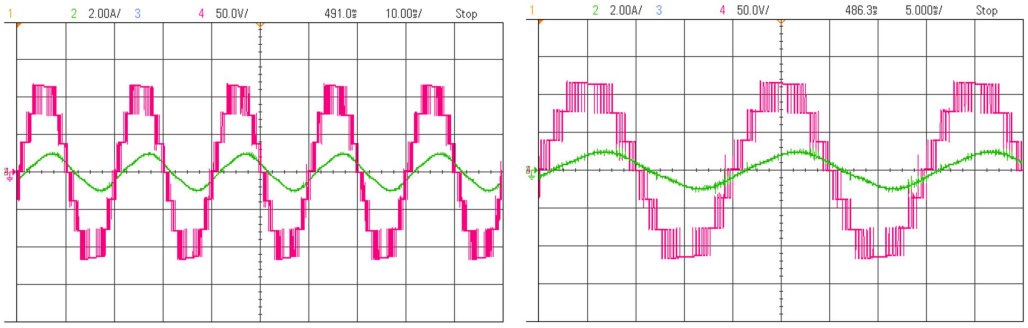


Fig. 7. Simulation results of 7-level: load voltage and current (5-cycles) (a); load voltage and current (2.5-cycles) (b)

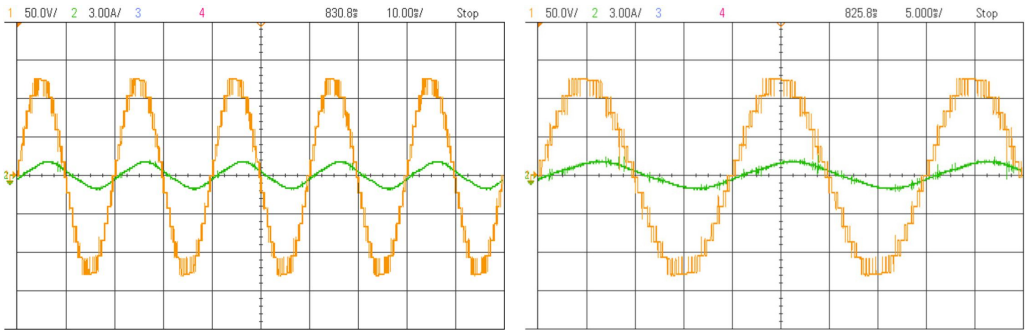
An experimental set-up is also executed for the same, i.e., for a 7-level inverter (symmetrical) where the experimental results are verified by the simulation result as shown in Figs. 8(a) (2.5-

cycles) and 8(b) (5-cycles), respectively. Moreover, a 13-level inverter is considered by choosing the magnitude of DC voltage in the ratio of 1:2:3, i.e., $V_1 = 21$ V,$V_2 = 42$ V, $V_3 = 63$ V, $V_x = 126$ V thereby generating +126 V as the peak of output voltage (maximum) and –126 V as the peak of output voltage (minimum) for load remaining the same, i.e., $R = 170\ \Omega$, $L = 100$ mH. Figures 9(a) and 9(b) show the load voltage and current for 5-cycles and 2.5-cycles respectively. All the results (symmetrical and asymmetrical) are incorporated to prove the effectiveness of the proposed topology.



(a) (b)

Fig. 8. Experimental results of 7-level: load voltage and current (5-cycles) (a); load voltage and current (2.5-cycles) (b)



(a) (b)

Fig. 9. Experimental results of 13-level: load voltage and current (5-cycles) (a); load voltage and current (2.5-cycles) (b)

The voltage waveform of the proposed 13-level inverter under dynamic conditions like variation of m_i is shown in Fig. 10. It is observed that for different values of m_i the proposed 13-level inverter generates three levels, five levels, seven levels, nine levels, and 11 levels respectively.

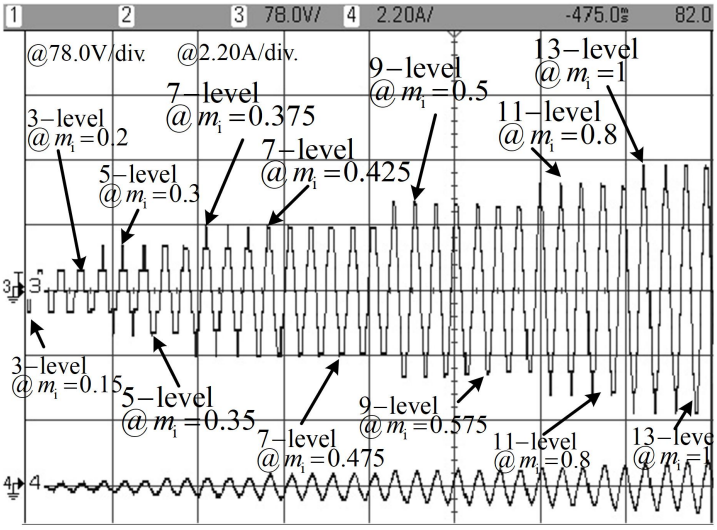


Fig. 10. Experimental results of output voltage and current of the proposed 13-level inverter for the transition of m_i from 0.15 to 1.0

6. Conclusions

This paper presents a novel and generalized topology which can be extended by adding the units. Based on the proposed MLI structure, 7-level (symmetrical) and 13-level (asymmetrical) inverters are simulated, and the results are experimentally verified with RL-Load. The topology shows better outcomes in terms of overall required components. The generalized formula for each required components is also derived for the proposed topology and suggested recent MLI topologies. The proposed topology was found better in terms of the economic cost, simpler circuit, and control, less maintenance, and less space requirement. Thus, the proposed reduced switch MLI is concluded to be better than the newly suggested MLIs.

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