A. WOJENSKI [1], K. T. POZNIAK [1], D. MAZON [2], M. CHERNYSHOVA [3]
[1] WARSAW UNIVERSITY OF TECHNOLOGY, INSTITUTE OF ELECTRONIC SYSTEMS
15/19 Nowowiejska St, 00-665 Warsaw, Poland
[2] CEA, IRFM F-13108 Saint-Paul-lez-Durance, France
[3] INSTITUTE OF PLASMA PHYSICS AND LASER MICROFUSION
23 Hery St., 01-497 Warsaw, Poland

Multiboard trigger link synchronization and diagnostics for the soft X-ray plasma radiation measurements

Abstract

Soft X-ray (SXR) plasma measurements are important type of diagnostics especially in tokamak facilities. Main output products are energy and topology spectra distributed in time. In case of Gas Electron Multiplier (GEM) detectors, used as radiation sensors, large number of analog readout channels must be provided. For this purpose Field-Programmable Gate Arrays (FPGAs) are used. Data quality monitoring (DQM) is important topic in case of asynchronous events registered by the measurement unit. Due to numerous FPGAs used it is necessary to provide advanced trigger synchronization between them. In the paper is proposed an algorithmic approach for the trigger link training and diagnostics. It is a key component in order to provide consistent measurement data for DQM analysis. The contents of the article covers the plasma experiments and related DQM topics. In following chapters explanation of the synchronization problem is described. The proposed algorithm will be used for trigger link synchronization and diagnostics aspects. The simulations are also discussed. Currently, the proposed ideas are at the stage of implementation and tests on real hardware. Simulation were successfully performed. Summary of the work carried out is presented at the end of the paper.

Keywords: Data Quality Monitoring, FPGA, GEM detector, soft X-ray plasma diagnostics, trigger distribution, measurement system.

1. Introduction

Undergoing studies on the tokamaks plasma impurities transport are one of the main topics regarding efficient phenomena control [1-3]. The measurement systems are working in robust environment, including high magnetic field and intense radiation. The unique feature of the plasma radiation is emission of asynchronous, random events with variable intensity. The data quality monitoring (DQM) is an important topic regarding spectra computation especially when working in a feedback loop with tokamak control systems. DQM block can track malformed signals, mark raw data, provide statistical counts or work as a filtering unit in order to provide only correct data.

In the mentioned system Gas Electron Multiplier (GEM) detectors are being used for soft X-ray radiation (SXR) measurement purpose [4, 5]. One of the main features of GEM detector is a large number of readout channels. The readout is often performed by the Field-Programmable Gate Arrays (FPGAs). However, due to limited number of I/O pins, it is necessary to use several FPGAs for readout from one GEM detector. When taking into account DQM aspects, it is necessary to provide consistent recording of the GEM detector signals. Thus, advanced trigger link synchronization and training needs be implemented.

The system consists of FPGA backplane units supporting 64 input channels each. To the backplane boards are connected Analog-Digital Board (ADB, up to 4) supporting 16 analog input channels each. The ADBs are connected to the Analog-Frontend Boards (AFEs) situated in the GEM detector. The AFE boards are designed radiation hard and placed close to the tokamak. The communication between AFE and ADB boards is based on analog Low-Voltage Differential Signaling (LVDS) links. The preprocessing data algorithms are implemented in the FPGAs. The data is sent for further post processing in high-end server using PCI-Express Gen2 interface for FPGA communication. More information about the construction of the system and additional software/ firmware can be found in [6-8].

In the following sections modular and universal approach to the trigger link training and diagnostics is presented, with first simulations results described.

2. Trigger signal distribution model

Trigger signal can perform various functions and be related to the different parts of the measurement system. In scope of the discussed system there are proposed two different kinds of the triggers:

- Global trigger *Algorithm Enable*
- Side trigger *ExtTrg* from FPGA backplane board.

The first one is directly related to the tokamak control system. When the plasma pulse is expected to begin, an adequate signal is being distributed along different kinds of measurement systems in order to prepare the acquisition. In case of multiple data registration units is necessary to have all of the acquisition units armed at the exact same time. Therefore, it is necessary to have one signal distribution unit (master), interfacing the signal distribution network with connected to it slave devices (FPGAs) in case of the described system. The scheme of connection is presented in Fig.1.

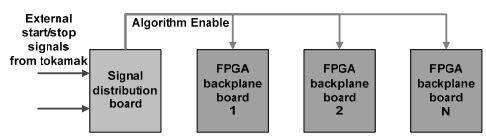

Fig. 1. Global trigger *Algorithm Enable* distribution scheme including signal distribution board and FPGA backplane boards as receiving units

When working with global triggering in raw data acquisition mode, it is necessary to have consistent data registered among all FPGAs (interfacing Analog-Digital Converters - ADCs). Once one of the boards registers photon event, rest of the boards should also register the incoming signals. The registered signal can be either part of the photon pulse (avalanche of electrons spread among different detector strips), noise or some interferences. All of the signal types (even "empty channels") are interesting for the DQM analysis. Thus, it is necessary to provide mechanism of information exchange about start of an event registration. The direct trigger signal *ExtTrg* can be implemented for this purpose. The scheme of connection among board is presented in Fig. 2.

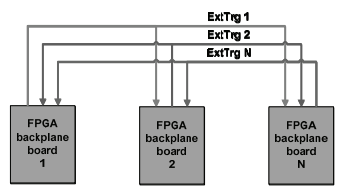

Fig. 2. *ExtTrg* signal distribution schematic. Each of the *ExtTrg* signals is being distributed among other boards

In the described system, multipoint LVDS (MLVDS) interface is used for triggering lines. Another additional components on signal line are voltage level translator and signal buffers. The multiple delay sources of the trigger signal, can be modeled as shown in Fig. 3.

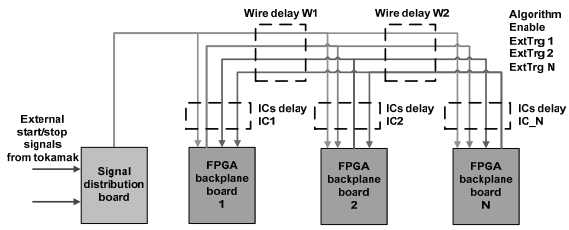

Fig. 3. Schematic of *Algorithm Enable* and external triggers distribution network

Two aspects should be taken into account when designing advanced trigger link synchronization for DQM analysis. Clock jitter and phase mismatch in the source and target FPGAs. The improper configuration of the IDELAYE2 components in the FPGAs can result it:

- Metastable reception of the trigger signal
- Random delay or overhead of the trigger signal

The effect of this particular case is a one-clock delay shift of the trigger signal (can be either forward or backward shift). Thus, it is necessary to fine-tune all of the signal receivers, so the introduced delay can be removed.

Based on scheme from Fig.3 the delay between backplane boards can be formulated as:

$$delayNto(N+1) = \Delta T_{IC_{N\_transm}} + \Delta T_{W_N} + \Delta T_{IC_{N+1}\_recv} \quad (1)$$

$$delayNto(N+2) = \Delta T_{IC_{N\_transm}} + \Delta T_{W_N} + \Delta T_{W_{N+1}}\, \Delta T_{IC_{N+2}\_recv} \quad \text{etc.} \quad (2)$$

where (assuming components parameters spread):

$$\Delta T_{W_{N+1}} \neq \Delta T_{W_N}, \Delta T_{IC_{N+i_{recv}}} \neq \Delta T_{IC_{N+j_{recv}}},$$
$$\Delta T_{IC_{N+i}\_transm} \neq \Delta T_{IC_{N+j}\_transm} \quad (4)$$

Due to presented assumptions, it is necessary to determine the maximum trigger delay among all of the boards used in the system. The local data registration triggers need to be delayed by the computed value. The proper local trigger distribution system in the FPGA unit should also be designed.

3. Trigger link synchronization and diagnostics algorithm

Based on the signal distribution model presented in section 2, it is necessary to design the algorithm with following features:

- Proper setup/ hold times of the input signal
- Removes the inducted delay difference of the signal among multiple boards (by wires, buffers, different ICs, etc.).

The setup/ hold time can be fine-tuned by IDELAYE2 blocks use, available in the Xilinx FPGAs [9]. However, in order to determine the proper value of the input wire signal delay, it is necessary to provide a test signal. Signal tests needs to be performed for longer period of time for "skipping" bits detection purpose.

In order to optimize the number of MLVDS lines used, one MLVDS line is related with one trigger line (one backplane).

The proposed training pattern for IDELAYE2 components is a deterministic, pseudorandom data stream based on linear feedback shift register (LFSR) algorithm block [10]. The number of logic resources used by the LFSR block is very low.

The LFSR data stream is generated by the master device (source) and received by a slave FPGA (target). The target latches the first incoming data word. The value is used to set a seed for local LFSR generator and start generating values using the same algorithm. The next incoming data word is compared with the own, generated data by target device. If they are the same, that means that the transmission is correct (flag *correctTransmission*). However, the most of the timing related problems (skipping bits) occur after period of time. Therefore, it is necessary to run the test with a long data stream.

In order to determine the skipping bits, the bitskip monitoring unit checks the state of flag *correctTransmission*. If it changed the state even once for whole transmission, this means that the bits are skipping and the IDELAYE2 block should be modified (tap number modification). The optimal IDELAYE2 tap is based on LFSR stream.

The state machine is as follows:

- Master unit generates the LFSR stream
- Slave unit:
  - Sets tap to staring value (i.e. 0)
  - Reads the input stream to latch one word as seed
  - Runs comparators between locally generated words (n_{local}+1, n_{local}+2, …) and received stream data words (n_{master}+1, n_{master}+2, …)
  - Runs bitskip monitoring unit to check the *correctTransmission* flag for *T* time:
    - Flag did not change over time and *correctTransmission* flag is set to 1, assume the current tap as start or stop value
    - Otherwise do not store IDELAYE2 value
  - Increments IDELAYE2 value (tap)
    - If maximum tap reached, stops the algorithm.

Once the algorithm has finished, the proper tap setting for IDELAYE2 input buffer will be:

$$tapOptimal = tapStart + \frac{(tapEnd - tapStart)}{2} \quad (5)$$

The equation sets the average value of IDELAYE2 component, where proper transmission can be achieved - most optimal setting.

Once the IDELAYE2 input buffer for trigger input is correctly tuned for setup/hold time margins, one can run routing delay removal algorithm, as mentioned in section 2.

The proposed routing delay removal algorithm is based on signal transmission loopback concept between two boards. The master units switches the trained trigger line from logic 0 to logic 1 (generates rising edge). The signal is received by the slave FPGA board (loopback board) and transmitted back to the master board – resulting in full loopback of the signal. In each FPGA signal resynchronization is needed by using Flip-Flops to prevent glitches on the input lines. The master unit sets the *loopbackDone* flag once received logic "1" from the loopback line.

In parallel to the signal transmission, the master units counts number of cycles between sent test signal and *loopbackDone* is set to 1. The resulting number of counts consists:

- Delay of internal logic in each FPGA (algorithm or resynchronization dependent).
- Additional delays introduced by clocks phase mismatch, long wires, ICs mounted on PCBs etc.

The local trigger on the slave (loopback) board should be delayed by number of cycles based on following equation:

$$TrgDelay = (DelayReadout - 2 * InternalDelay)/2 \quad (6)$$

In order to provide the exact same time for recording of the events in each FPGA (related to the photons registered by GEM detector) it is necessary to delay the local trigger. The arrival time of *ExtTrg* signal needs to be time-matched with locally generated trigger signal.

Special consideration should be taken when using more than 2 backplane boards. In this case, one triggering line can have different delay among boards. Therefore, additional compensation among one trigger line needs to be implemented in each receiving backplane board (referred as Delay2 in Fig. 4). The proper value can be determined based on *TrgDelay* values among board with detection of maximum value based on loopback testes.

The algorithms starts registration of event when the threshold value is exceeded by ADC input signal. It is necessary that all of the boards have enabled data registration algorithm at very same time moment. The *Algorithm Enable* signal should be received by all of the boards with the same delay. The signal can be also used

to synchronize the timestamp counter on each of the boards. Thus, it should be delayed by the value calculated from equation 6.

The trigger distribution system implemented in each FPGA, should consisted logic presented in Fig. 4. It is assumed that signal is registered as a window consisting several samples.

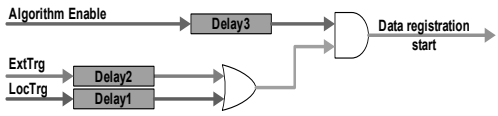

Fig. 4. Implementation of trigger distribution system for data registration start in FPGA logic

The proposed approach can be easily expanded to support more boards connected to the system. It is worth to mention that the algorithms can work also as a hardware lines diagnostic utilities. In case of any kind of malfunction of the MLVDS lines, either IDELAYE2 or loopback algorithm will result in incorrect flag setting. This provides direct information about hardware status.

4. Simulation of the algorithms

The proposed algorithms have been implemented in Verilog language. Testbench simulations were performed using ISIM under Vivado 2015.4.2. The resources used after synthesis of all necessary components to perform link synchronization for each FPGA are:

- Look-up table: 561 units
- Flip-flop: 609 units

The testbench includes following components:

- One main *Algorithm Enable* signal distribution board
- Two FPGA backplane boards with *ExtTrg* signals connected
- Bidirectional connections (simulation of MLVDS lines) between boards
- Configurable PCB delay lines blocks – simulation of delays inferred from signal lines, buffers, ICs etc. – delay set as a number of clock cycles
- Raw data registration algorithms
- Data storage in the memory

For the simulation, each of PCB delay lines have been set to different values, to simulate the influence of length of the MLVDS cable among multiple boards.

The master boards generate pseudo-random stream, received by each backplane boards. The onboard algorithms latch the incoming data and set *correctTransmission* flag to 1, once the pattern is correctly recognized. This ensures correct timing of incoming signals (due to complex implementation, taps are not incremented in testbench, tests will be performed on hardware).

Second stage of link training is signal loopback test. The master board generates the pulse signal. The signal passes each of backplane boards (separate lines) and is sent back to master board. The delay of the signal to be set is corresponding backplane boards is computed upon equation 6. Based on algorithm described in section 3, the delay value is set for each board.

To verify the correctness of trigger link synchronization between backplane boards and master unit, the analog input signal is generated in testbench. The signal simulates incoming ADC data. Each signal registered by the board has a corresponding timestamp. In case of synchronized trigger, all of the boards should have signal registered with the same timestamp.

In simulations, links were successfully trained. It was possible to register events on all FPGA boards with consistent timestamp.

After successful simulation verification, HDL codes for Xilinx Artix7 and Spartan6 FPGAs have been implemented. In parallel to the firmware, PC software has been developed in order to implement particular fragments of described algorithms in software and provide control interface. The communication is done using PCI-E interface. The firmware is now under first tests on real hardware.

5. Conclusions

The processed data from the soft X-ray plasma diagnostic systems, especially working in the feedback loop with the tokamak control units, should be monitored in real-time in order to provide reliable output products. The Data Quality Monitoring is an important topic. To provide consistent raw data for data quality analysis, it is necessary to design precise algorithms for trigger signals distribution. The proposed approach is based on IDELAYE2 blocks, LFSR data patterns and signal loopbacks. The key benefits of the proposal are as follows:

- Simple mechanism in FPGA using low amount of resources
- Training and link diagnostics function
- Easily expandable

The proposed algorithms have been designed and successfully simulated in ISIM software. Verilog implementations have been developed for both Xilinx Artix7 and Spartan6 FPGAs. Currently, the design is being tested on real hardware.

The Author of the paper received funding under the doctoral scholarship financing program from National Science Centre, number 2016/20/T/ST7/00203.

6. References

[1] Sertoli M. et al.: Modification of impurity transport in the presence of saturated (m, n) = (1,1) MHD activity at ASDEX Upgrade. Plasma Physics and Controlled Fusion,vol. 57(7), 2015.
[2] Mazon D., et al.: GEM detectors for WEST and potential application for heavy impurity transport studies. J. of Instrum. ,vol. 11 (8), 2016.
[3] Vezinet D. et al.: Fast nickel and iron density estimation using soft X-ray measurements in Tore Supra: preliminary study. Fusion Science and Technology, vol. 63(1),2013.
[4] Sauli F.: GEM: A new concept for electron amplification in gas detectors. Nuclear Instruments and Methods in Phys. Res A,vol. 386, p. 531-534 , 1997.
[5] Chernyshova M. et al.: Conceptual design and development of GEM based detecting system for tomographic tungsten focused transport monitoring. Journal of Instrumentation, vol. 10, 2015.
[6] Wojenski A., et al.: Multichannel reconfigurable measurement system for hot plasma diagnostics based on GEM-2D detector. Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, vol. 364, 2015.
[7] Wojenski A., et al.: Concept and Current Status of Data Acquisition Technique for GEM Detector Based SXR Diagnostics. Fusion Science and Technology, vol. 69 (3), 2016.
[8] Wojenski A., et al.: FPGA-based GEM detector signal acquisition for SXR spectroscopy system. J. of Instrument., vol. 11, November 2016.
[9] Xilinx 7 Series FPGAs SelectIO Resources User Guide, UG471, 2016.
[10] Panda A. K. et al: FPGA Implementation of 8, 16 and 32 Bit LFSR with Maximum Length Feedback Polynomial Using VHDL. 2012 International Conference on Communication Systems and Network Technologies, Rajkot, 2012, pp. 769-773.

Received: 21.03.2017 Paper reviewed Accepted: 03.05.2017

Andrzej WOJENSKI, MSc, eng.

PhD student at The Faculty of Electronics and Information Technology, Warsaw University of Technology, Poland. The area of research consists first, modular measurement systems for plasma physics and high energy physics experiments. The main scope of work is FPGA firmware development, along with algorithms, transmission links, and low-level control software design, and hardware verification of measurement systems.

e-mail: A.Wojenski@elka.pw.edu.pl