Design of Low Power Analog Front-End for 13.56MHz RFID Transponder

Sherif Saleh, Mohamed Osman, Ghada Hamdy, Amal Zaki, and Hamed Elsemary

***Abstract*—This paper presents the design of 13.56MHz RF Front-end circuit for low-power medical applications. It converts RF power into DC and then extracts the clock and the data. The design includes rectifier, voltage multiplier, voltage regulator, data demodulator, ring oscillator, RF voltage limiter and LC matching network. It provides an excellent trade-off between high performance, simplicity of architecture, and low power consumption. It is designed to be fully integrated on chip. Simulation is done using 0.35-µm CMOS technology and the results are compared with other reported RFID systems. The total power consumption is adjusted to be around 4 µW at the minimum input power.**

***Index Terms*—Analog front frond, RFID, charge pump, OOK**

I. Introduction

PASSIVE radio frequency identification (RFID) technology enables battery-free wearable and implantable sensors with an unlimited lifespan and small size [1]. These proper- ties facilitate advanced biomedical research. An integrated RF rectifier converts the incoming RF power to DC power for the entire design. The RFID system has two parts, the tag and the reader. The tag can be stated as a small device, which is usually, fabricated using silicon technology complemented by an antenna. The reader can be considered as a system, which communicates with the tag along with providing sufficient RF energy. Some applications require long-range operations; therefore, it is crucial to attain low power dissipation. Some applications require long-range operations and therefore it is crucial to attain low power dissipation. Circuit integration offers effective possibilities to realize ultra-low power designs [2]. The front end of the Tag introduced in this paper, is designed to satisfy the low power requirement to reach a power consumption of 2µW. This paper is organized as follows. An overview of the entire designed system is reported in Section II. Section III presents the system architecture and the detailed building blocks. The simulation results and the comparison with the other reported systems are discussed in Section IV. Finally, a conclusion is drawn in Section V.

II. System Overview

The conceptual diagram of the complete block diagram is depicted in Fig. 1. It consists of rectifier, voltage multiplier, voltage regulator, data demodulator, ring oscillator, RF voltage limiter, and LC matching network. The principle of operation is as follows, the power rectifier converts the incoming electromagnetic RF wave to DC supply for the entire circuits of the transponder. Charge pump is addressed for that purpose. Since the incoming signal has a low input voltage, the charge pump will not only rectify the incoming signal, but also it raises the signal to a higher value to be convenient for long-range applications. If the DC supply voltage reaches a defined level, the power-on-reset (not shown) generates a reset signal, which places the digital part into a known state. The ASK demodulator recovers the information and delivers the data to the digital part. The voltage limiter protects the analog frontend at high RF levels and define the upper limit of the incoming signal. In addition, a voltage regulator is used to keep the voltage at 2 V, which be the supply voltage for the rest of the chip. An ultra-low-power ring oscillator is designed to provide a clock signal to the digital part.

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III. Analog Building Blocks

The implemented RF front-end of integrated passive transponders topology depends on the requirements given by a specific application. Thus, for an ultra-low-power frontend design, it is essential to know the behavior and the interaction of the non-linear devices and the field of application. In this section, the analog building blocks of the RF frontend of an UHF RFID transponder are illustrated in Fig. 1.

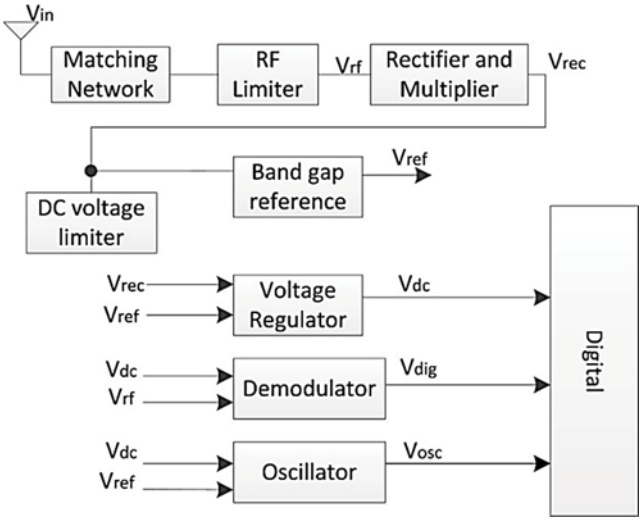

Fig. 1. Architecture of a 13.56 MHz RFID tag system

A. Ultra-Low-Power Rectification and Voltage Multiplier

The rectifier is used to provide the envelope of the RF signal to the demodulator and to apply a DC voltage to the first stage of the charge pump. The input unmodulated signal at the rectifier terminals can be written as:

$$V_{in} = V_{rf} sin\ (\omega t)\ ) = V_{in}\ sin\ (2\pi/T_0) \quad (1)$$

where V_{rf} is RF carrier signal and T_0 is the period of the incoming RF carrier. The basic operation of the circuit can be

explained with the help of Dickson charge pump, shown in Fig. 2. At the operating frequencies, assuming a very low current consumption and 2 pF equivalent capacitance, the voltage drop at the output due to the capacitor discharge is estimated in few mV, so it can be neglected in the calculations. Therefore, the rectified voltage after the bridge can be approximated as [3], [4]

$$Vrec = N\,(Vrf - Vd) \tag{2}$$

where N is the number of stages of the charge pump and V_d is the voltage drop across each diode. The rectifier cannot provide a sufficient supply level to the core of the system when the tag is located far from the reader. A voltage multiplier (charge-pump) is thus introduced; the schematic of the circuit is presented in Fig. 2. The RF rectifier employs a 6-stage Dickson charge-pump topology using Schottky diodes with shunting capacitors to provide an output DC voltage of 3.3 V from an incoming RF input signal of 900 mV.

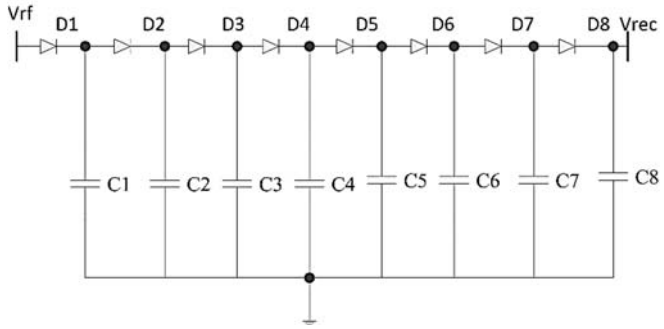

Fig. 2. Half-wave rectifier and charge pump

B. DC Voltage Limiter and Band-gab Reference

Due to the strong fluctuations in the input signal, the output voltage of the charge pump is constantly varying. However, as the input RF signal gets higher, the rectified signal V_{rec} also becomes higher, which posing a risk to the transistors. Therefore, inserting a DC voltage limiter is needed. Fig. 3 shows the DC voltage limiter used in this work. The transistors (M1-M4) are diode-connected transistors with a combined threshold value of 3.3 V. As soon as this voltage is reached, current will start to flow through this branch, results in turning on the transistors M5 and M6 and thus shunting Vrec to ground. The feedback loop is implemented to have a constant voltage at much defined magnitude. This voltage is used as a supply for the band-gap reference circuit to produce a reference voltage of 1.3 V, which is used as a supply voltage for the other circuits.

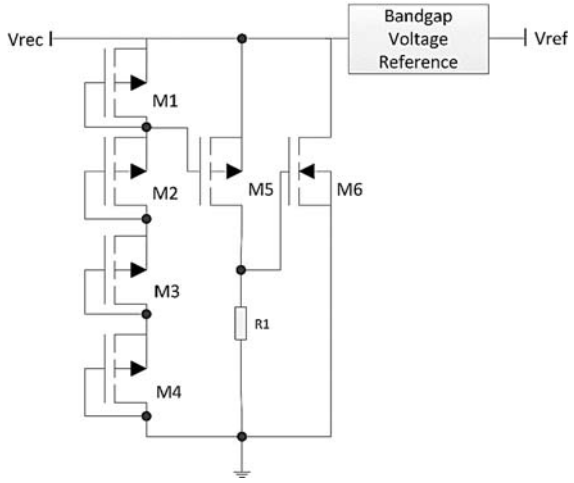

Fig. 3. DC-voltage limiter

C. Voltage Regulator

The supply voltage provided at the output of the charge pump is strongly dependent on process variations and temperature. Furthermore, this potential is also determined by the current consumption of the circuit and the distance from the reader: moving the tag with respect to the reader causes a variation of the V_{dc} that could be noticeable along the whole reader-tag transmission stream [5]. The DC voltage limiter is designed to have an upper limit of 3.3 V. As long as the On-Off keying modulation technique is employed in this work, so when the incoming signal is low i.e. 0V, the capacitor in the charge pump will discharge, results in decreasing the output voltage until the RF signal becomes high again. The varying in the voltage cannot be used as a source voltage for the entire circuits; this will detain the normal working of the chip.

This problem might be overcome with the solution of using a capacitor at the output port of the charge pump, but this causes a slow response due the charging time of the capacitor. It is therefore mandatory to introduce a voltage-regulation system, allowing also achieving a better control of the digital gates behavior. The regulator presented in Fig. 4, has the well-known structure of a series transistor on the power path driven by an op-amp. The designed voltage reference, left part of Fig. 4, is a diode-connected nMOS transistors biased with the current given by nMOS transistor M5. Setting the aspect ratios of the MOS devices allows to achieve relatively small variations with temperature, while employing channel lengths higher than the minimum one grants both good supply independency and very low power consumption.

pMOS transistor is used as a pass device to vary the resistance depending on input and load voltage levels. The diode-connected transistors driver (behave as resistors), M7-M10, senses the load voltage. A part of it, matches the given reference voltage, is feed back to the error amplifier's negative terminal whose output controls the pass device. The gain and the bandwidth of the error amplifier must be as large as possible so

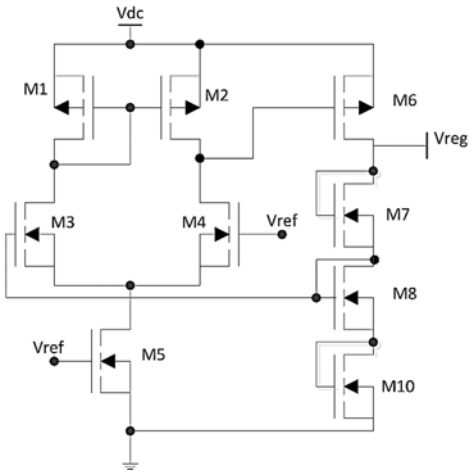

Fig. 4. Voltage regulator

that high frequency changes at the input are nullified very soon. The output of the voltage regulator is set to 2 V, which acts as a supply voltage for the entire design. Figure 10 presents the voltage regulator output at maximum and minimum input signal, where its output voltage is kept between 1.5 – 2 V.

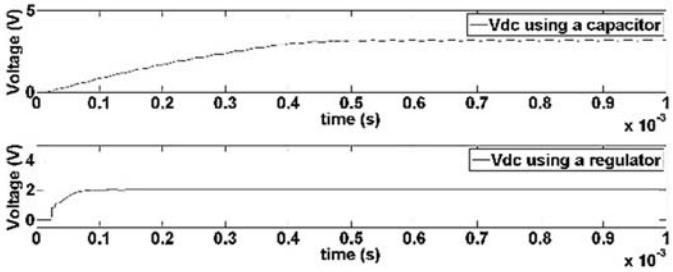

Fig. 5. Comparison between using a capacitor and voltage regulator

D. On-Off Keying Demodulator

The envelope of the AM signal obtained from the rectifier is translated into CMOS levels with the On-Off keying demodulator circuit shown in its simpler version in Fig. 6. In order to provide suitable input to a comparator, the average level of rectifier is retrieved by means of an RC low pass filter able to track long-term variations of the rectified level. For the sake of low power requirements, it consists of a full-wave rectifier followed by two RC low pass filters in series, whose output are fed to a comparator. The bandwidth of the first filter has to be equal to the bandwidth of the transmitter data rate, so that it can detect the signal envelope.

The second filter is designed to provide an average of the signal as a dynamic reference voltage. The first filter pole frequency is designed at 63.69 kHz, with nominal R_1C_1 values of 250 kΩ and 10 pF, respectively, while the second filter is tuned at 6.36 kHz with R_2C_2 values of 250 kΩ and 100 pF, respectively.

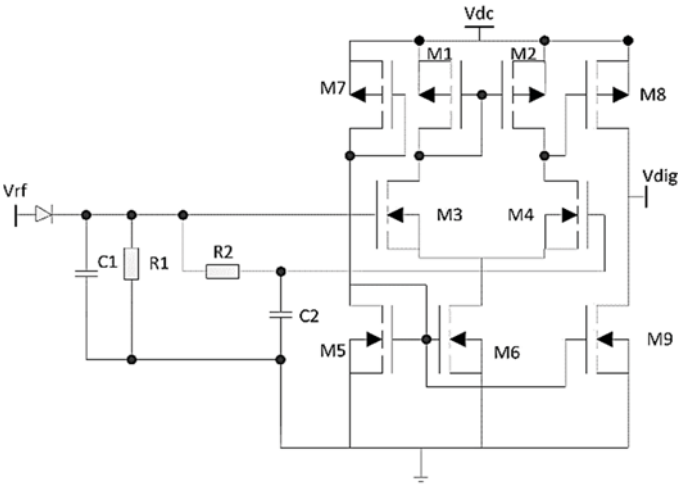

Fig. 6. On-Off keying demodulator circuit

E. Ring Oscillator

Due to the power and area constraints, a ring oscillator, shown in Fig. 7, is designed by combining an odd number of inverters in a closed loop. The circuit is designed to generate a 400 kHz clock frequency, which can be adjusted by matching the number of inverters in the chain and setting the transistor's ratios (W/L).

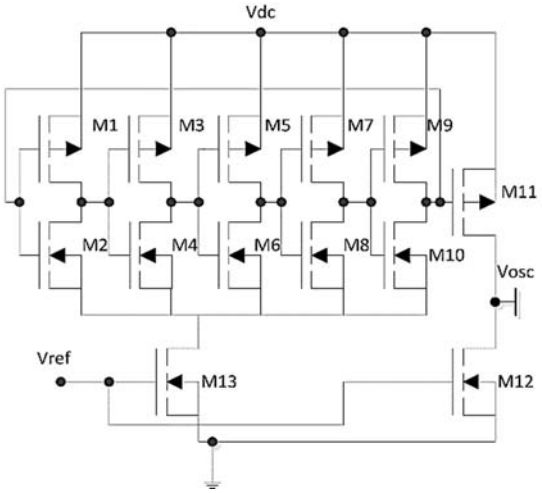

Fig. 7. Ring oscillator circuit

F. RF Voltage Limiter

The voltage limiter protects the analog frontend at high RF levels due to the large induced voltages in the presence of high excitation field amplitudes. Applying this way, the input signal to the data demodulator is also constrained to an adequate level. For this purpose, three-diodes in forward bias and the same in the reverse bias are implemented, as presented in Fig. 8. The incoming RF input signal will never exceeds 2.3 V, since each diode presents a threshold value of around 760 mV.

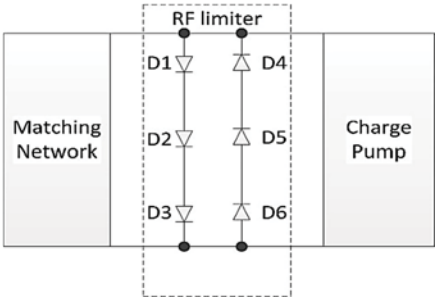

Fig. 8. RF voltage limiter circuit

G. LC-Matching Network

In order to improve the efficiency of the circuit capacitor C is connected in parallel with the coil antenna L, and the tag to form a parallel resonant circuit with a resonance frequency corresponds to the RFID carrier frequency. The values of L and C are calculated to be 1.5 μH and 137.8 pF, respectively, at the frequency of 13.56 MHz.

IV. Simulation Results and Discussion

The front-end of the transponder is simulated in a 0.35 μm CMOS process technology in Cadence environment. The incoming modulated RF signal frequency was 13.56 MHz with a data rate of 64Kbps. Monte Carlo verification has been carried out to check the design performance during process variations. The simulation is performed in 200 iterations to investigate the transponder performance towards DC-reference biasing voltage. The transponder is able to create a DC-reference voltage of 2.01 – 2.03 V over 35% of the process variations which is increased to 80% for a DC-voltage between 2.0 – 2.05 V. However, it achieves 100%, when it covers the range of 1.99 – 2.065 V as depicted in Fig. 9.

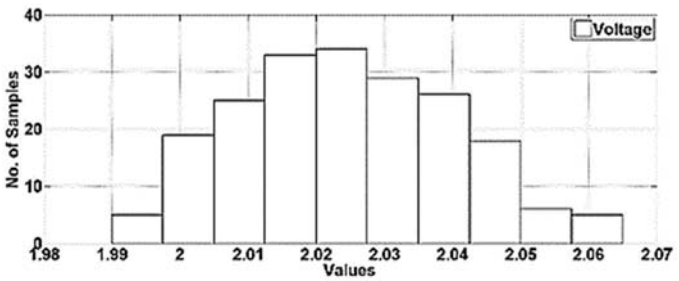

Fig. 9. MC waveforms for 2 V reference voltage

This is an acceptable result as a reference voltage for the entire design. However, this can be improved by modifying the charge pump and the limiter regulator, by utilizing active diode-connected transistors with a minimum threshold voltage. Fig. 10 shows the regulator transient response in cases of maximum and minimum input voltages. Currently the local oscillator is designed to generate a clock frequency of 0.4 MHz and consume 1.3 μW at the minimum input power of 20 μW. The total power consumption in the tag front-end, including the charge pump, ring oscillator, ASK demodulator, shunt regulator and the digital logics is only 4 μW at 1 MΩ load. Table I shows a comparison of this work with the other reported RFID systems. As noticed, the power efficiency of this design is very competitive compared to that of previous work. In addition, the consumed power has an excellent value compared to the previously reported works.

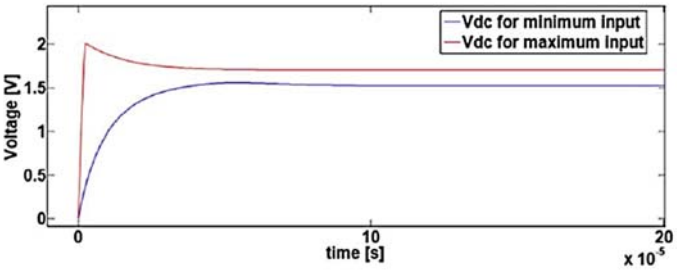

Fig.10. Vout of the voltage regulator at maximum and input RF signal

V. Conclusion

This paper presents a low power-consuming analog front-end for passive RFID tags working at 13.56 MHz. The low power analog blocks including the bias, data detection circuits consume less than 2 μA current.

Table I shows a comparison of this work with the other reported RFID systems. As noticed, the power efficiency of this design is very competitive compared to that of previous work. In addition, the consumed power has an excellent value compared to the previously reported works. A significant improvement in performance beyond the state-of- the-art was achieved by merging the load modulation and voltage clamping into the voltage doubler rectifier circuits to achieve longer operation distance.

TABLE I.
COMPARISON OF RFID SYSTEMS

Ref.	Power efficiency	Power cons. (μW)	Voltage (V)	Current (μA)
[6]	< 13%	2.25	1.5	2.25
[2]	< 1%	1.2	1.5	1.2
This work*	30%	4	2	2

* The power is delivered to 1MΩ load

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