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Dual Virtual Flux-based Direct Power Control for rectifier under harmonically distorted voltage condition

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Abstract: This paper presents an improved Virtual Flux-based Direct Power Control (VF-DPC) applied for a three-phase pulse width modulation rectifier. The proposed control approach incorporates an enhanced Virtual Flux estimator made up of a cascade second-degree low-pass filter. This latter guarantees the attenuation of the highest harmonics. The introduced control concept presented in this paper has interesting features such as reducing the current harmonics distortion. In other words, it ensures that the input current drawn from the power supply is perfectly sinusoidal whatever the state of the network voltage. The proposed method also allows to maintain the DC side capacitor voltage at the required level and assure that the input current is in phase with the respective voltage to satisfy the unity power factor function. The results obtained from the numerical simulation have proved the effectiveness of the proposed method for disturbed grid voltage and system parameters variation.

Key words: Direct Power Control (DPC), Dual Virtual Flux (DVF), Phase Locked Loop (PLL), Pulse with Modulation (PWM), rectifiers, Virtual Flux (VF)

1. Introduction

Since the renewable energies are progessively integrated in smart grids, it is expected that the electrical production manner will be less dependent on the conventionel concept. Unfortunately, stability problems are a result of the increased penetration of renewable energy into the grid. An improvement in the performance of the system is therefore necessary [1].

Many studies have focused on the advanced control of the operation of renewable energy. To adjust the produced power parameters required by the grid, electronic converters are used for disturbed conditions. However, these advanced control methods require accurate information to ensure proper operation.

The Direct Power Control (DPC) strategy has attracted much attention among researchers in recent years because of its many advantages. They have shown that the use of DPC in two and three level converters is more beneficial because of its: simple structure, quick response and great robustness [2]. The instantaneous power theory proposed by Japanese researchers in 1980 is inspired by the Direct Torque Control (DTC) proposed in [3]. The theory of the DPC of a three-phase Pulse With Modulation (PWM) converter has been analysed and applied progressively [4].

Another operating technique without a tension sensor is presented in [5, 6] which offers technical and economic advantages to the interesting system such as the isolation of the power part of the control part and the reduction of the number of knife sensors.

The quality of electricity is mainly reduced to the quality of the voltage wave delivered. When this voltage is present, the main phenomena that can affect it are: voltage dips of short or long duration, flicker, overvoltage, imbalance or harmonics. Unfortunately, the DPC scheme with conventional instantaneous active and reactive power definitions cannot function properly under unbalanced line voltage. The authors in [7] proposed a method to solve the performance degradation of conventional DPC-Space Vector Modulation (SVM) under unbalanced network voltage conditions. Their idea is that the original Instantaneous Powers theory is replaced by an extended Instantaneous Powers theory. In [8] the power compensation is calculated and added to the original referenced power to obtain a balanced input current. The use of a Multiple Complex Coefficient Filter (MCCF) allows one to extract the positive and negative sequences of the voltage and current.

The authors in [9] studied the Linear-Quadratic Regulator (LQR) based control system for a 3-level rectifier. They demonstrated that the selection of weighting matrices in the LQR can be performed effectively using particle swarm optimization, which led to satisfactory results concerning not only the stationary states but also various types of transient states.

A neural filter-based integrator is proposed in [10] and used to estimate Virtual Flux (VF) in order to eliminate harmonic distortions applied to predictive DPC based on VF. The authors in [11] proposed the DPC method to control both active and reactive powers by analyzing the influence of each voltage vector of the converter. This provides constant active and reactive powers as well as sinusoidal network currents through an appropriate switching table.

To trace the power grid standard and improve converter operation, a Phase Locked Loop (PLL) is crucial to accurately detect the phase angle of the network when the grid voltage is polluted by harmonics and imbalance. Various methods of DPC have been proposed to solve these problems, but these methods are generally complicated and difficult to use because of the complexity of their structures.

The Synchronous Reference Frame-PLL (SRF-PLL) method is the most commonly used approach for grid synchronization. As shown in Fig. 1, in a conventional SRF-PLL, also called the dq-PLL, the grid three-phase voltages (V_a, V_b and V_c) are converted to V_α and V_β, and then to a rotating frame reference (*de-qe*) using the Clarke and Park transformations. The output of conversion is then regulated using a loop control which forces V_q to zero in a steady state. As concluded in [12] and [13], when the network voltage is balanced, the SRF-PLL is able to obtain

a very high bandwidth and a very fast dynamic response. However, his efficiency is no longer insured under disturbed network conditions.

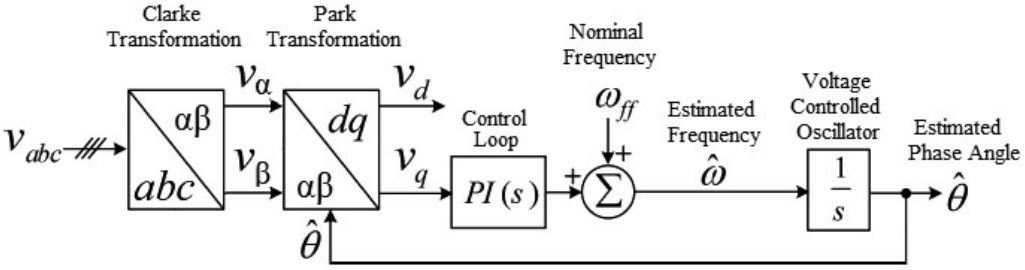


Fig. 1. The Synchronous Reference Frame Phase Locked Loop (SRF-PLL)

Many researchers have made improvements to the conventional SRF-PLL method by proposing different variants. The Dual SRF PLL (DSRF-PLL) and decoupled DSRF (DDSRF), which are based on the use of two SRF systems that can detect the negative and positive sequences of the disturbed network voltage, have been proposed, respectively, in [14] and [15]. The SRF-PLL method with a Sinusoidal Signal Integrator (SSI) has been presented in [16] and it has been proved that it gives a significant reduction in computation burden. A Double Second-Order Generalized Integrator based on PLL (DSOGI-PLL) has been proposed in [17] that has given a fast, accurate and adaptable response under faulty grid conditions.

The main contribution of this paper is the proposition of a novel Virtual Flux detection technique incorporated in a Direct Power Control (VF-DPC) scheme for a three-phase PWM rectifier. The VF algorithm has an open-loop structure and uses the output fundamental orthogonal signals which are obtained directly from estimating the fundamental active and reactive powers. This method provides a quasi-sinusoidal input current waveforms under different input voltage conditions and achieves good stability that improves the performance of the VF-DPC.

2. System description and modeling

The PWM rectifier is crucial in the field of energy conversion and is widely used to connect an AC electrical grid with a DC-link circuit, e.g. wind turbines and PV panels. It offers many advantages such as the sine current on the mains side with a low Total Harmonic Distortion (THD), bidirectional energy flow and unity power factor [18].

The voltage equation in the rotating $\alpha\beta$ reference frame is Eq. (1). It donates a clear description of the configuration of the two-level three-phase rectifier illustrated in Fig. 2.

$$\begin{pmatrix} L\dfrac{\mathrm{d}i_\alpha}{\mathrm{d}t} \\ L\dfrac{\mathrm{d}i_\beta}{\mathrm{d}t} \\ C\dfrac{\mathrm{d}U_{dc}}{\mathrm{d}t} \end{pmatrix} = \begin{pmatrix} U_\alpha \\ U_\beta \\ 0 \end{pmatrix} - \begin{pmatrix} R & 0 & 0 \\ 0 & R & 0 \\ -S_\alpha & -S_\beta & 0 \end{pmatrix} \begin{pmatrix} i_\alpha \\ i_\beta \\ U_{dc} \end{pmatrix} - \begin{pmatrix} 0 \\ 0 \\ i_{rd} \end{pmatrix} - \begin{pmatrix} U_{r\alpha} \\ U_{r\beta} \\ 0 \end{pmatrix}, \tag{1}$$

where: $U_{\alpha\beta}$ and $i_{\alpha\beta}$ are the line side input voltage and current after the Clark transformation, L and R are the line side inductance and resistance, C is the capacitance of the DC-bus capacitor, i_{rd} is the rectified current, $U_{r\alpha\beta}$ represents the input phase voltages of the rectifier, $S_{\alpha\beta}$ represents the switch functions and U_{dc} is the output DC voltage.

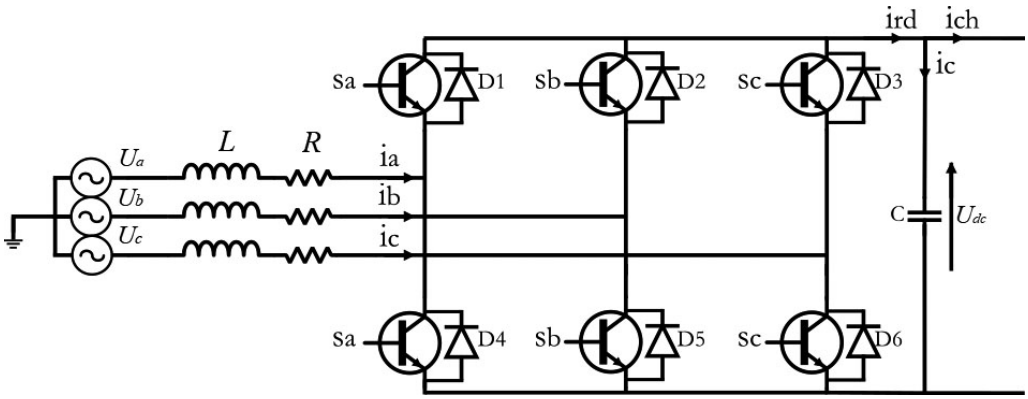


Fig. 2. Representation of a two-level three-phase rectifier

2.1. Virtual Flux estimation

The conventional DPC without a voltage sensor uses a power estimation strategy based on (VF-DPC) which is defined as the integration of the network voltage [19] and its representation is illustrated in Fig. 3. The components of the VF are calculated in the stationary $\alpha\beta$ coordinate system as:

$$\psi_{\alpha\beta} = \int U_{\alpha\beta}\,\mathrm{d}t = \begin{pmatrix} \int U_\alpha\,\mathrm{d}t \\ \int U_\beta\,\mathrm{d}t \end{pmatrix} = \begin{pmatrix} \psi_\alpha \\ \psi_\beta \end{pmatrix}. \tag{2}$$

Then:

$$\Psi = \int \left(L\frac{\mathrm{d}i}{\mathrm{d}t} + U_r + Ri \right) \mathrm{d}t, \tag{3}$$

where $\Psi_{\alpha\beta}$ and U_r are respectively the flux components in the stationary frame and the rectifier input voltage vector.

With:

$$U_r = \begin{pmatrix} U_{r\alpha} \\ U_{r\beta} \end{pmatrix} = \begin{pmatrix} \frac{2}{3}U_{dc}\left(S_a - \frac{1}{2}(S_b + S_c)\right) \\ \frac{1}{\sqrt{3}}U_{dc}(S_b - S_c) \end{pmatrix}, \tag{4}$$

where: U_r is the the rectifier input voltage vector and $U_{dc}$is the output DC voltage.

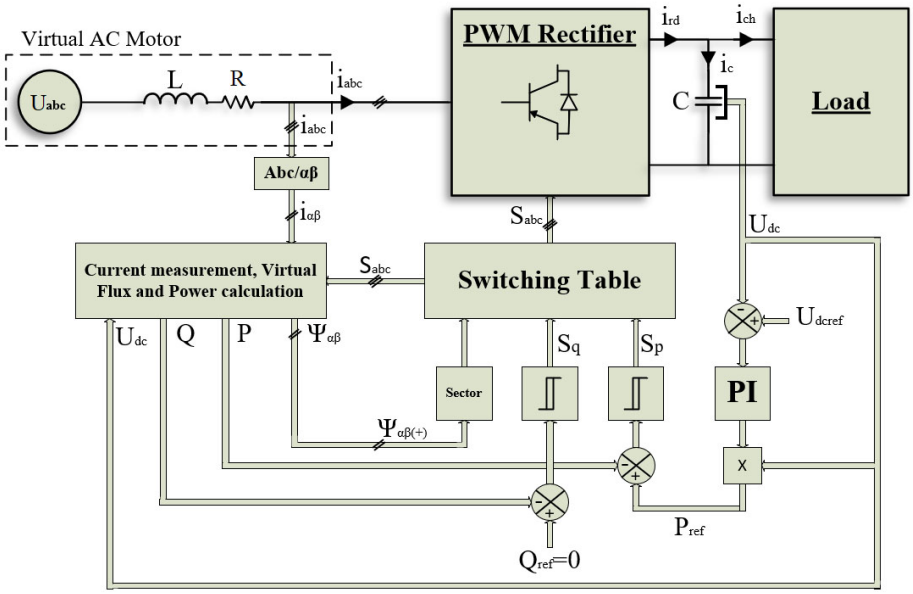


Fig. 3. VF-DPC conventional diagram of voltage sensor-less

2.2. Active and reactive power calculation

Line current and Virtual Flux components are used in power calculations. They can be calculated by the following expressions:

$$\begin{cases} P = \omega \left(\psi_\alpha \imath_\beta - \psi_\beta \imath_\alpha \right) \\ Q = \omega \left(\psi_\alpha \imath_\alpha + \psi_\beta \imath_\beta \right) \end{cases}, \tag{5}$$

where: P is the active power, Q is the reactive power and ω is the angular frequency of the grid fundamental wave.

2.3. Sector selection

Knowledge of the measured voltage range is necessary to choose the optimal switching states. The plane of the space vector is divided into 12 sectors of 30° as a function of the position of the voltage vector $V_{\alpha\beta}$. The division of the plane into 12 sectors instead of 6 sectors leads to effectively reduce the errors of the powers, the harmonics and the fluctuation of the DC voltage. The distribution of θ is shown in Fig. 4 governed by the following equation:

$$\theta = \arctan\left(\frac{\Psi_\beta}{\Psi_\alpha}\right), \tag{6}$$

where θ is the phase angle.

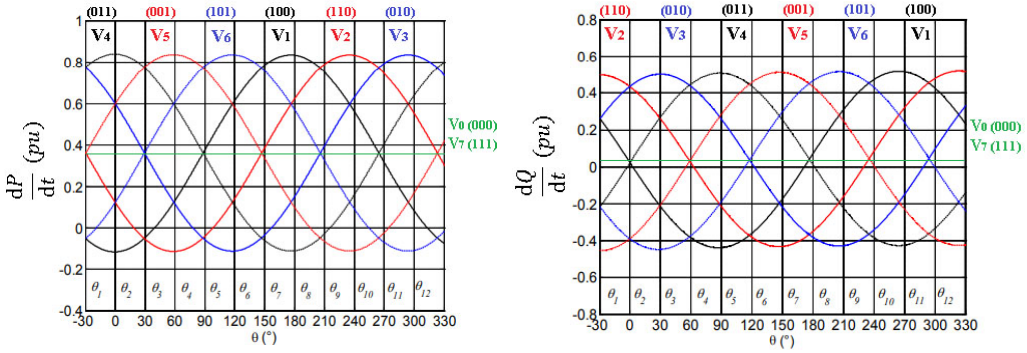


Fig. 4. Voltage and sector

2.4. PI regulator

The functional diagram of the U_{dc} voltage regulation based on the classic PI regulator is given in Fig. 5. It corrects the error between the measured DC voltage and its reference.

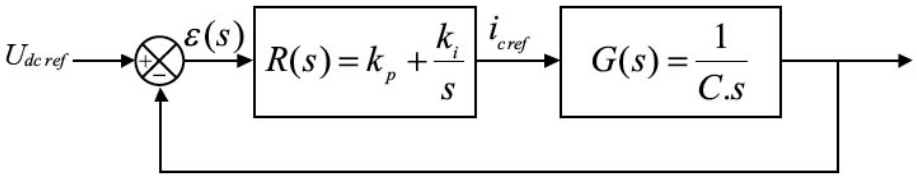


Fig. 5. DC capacitor voltage regulation

The product of the reference DC current with the DC voltage gives the active reference power. The closed loop transfer function is given by:

$$H(s) = \frac{R(s)G(s)}{1 + R(s)G(s)} = \frac{k_p s + k_i}{Cs^2 + k_p s + k_i}. \tag{7}$$

To control the closed loop system, the coefficients k_i and k_p must be chosen. The transfer of a second order function system is given by:

$$F(s) = \frac{\omega_c^2}{s^2 + 2\xi\omega_c s + \omega_c^2}. \tag{8}$$

So, $k_p = 2C\xi\omega_c$ and $k_i = C\omega_c$.

3. Voltage sensor-less DPC based on Dual Virtual Flux

The three-phase converter with DPC control is limited to ideal voltage sources, while there is always a certain imbalance in our network. This imbalance causes a current distortion and a large

variation in the DC bus. DPC consists in selecting a control vector from a switch table. *SP* and *SQ* are provided by the two-level hysteresis regulators. According to the value of voltage vectors in this position, the plane $\alpha\beta$ is divided into twelve sectors where it is necessary to specify a logical state for each sector. The reference of the active power is given by regulating the DC voltage, from a PI regulator. While ensuring a unity power factor, control of the reactive power to zero is performed. Fig. 6 shows the global configuration of the DPC with a VF for a three-phase PWM rectifier.

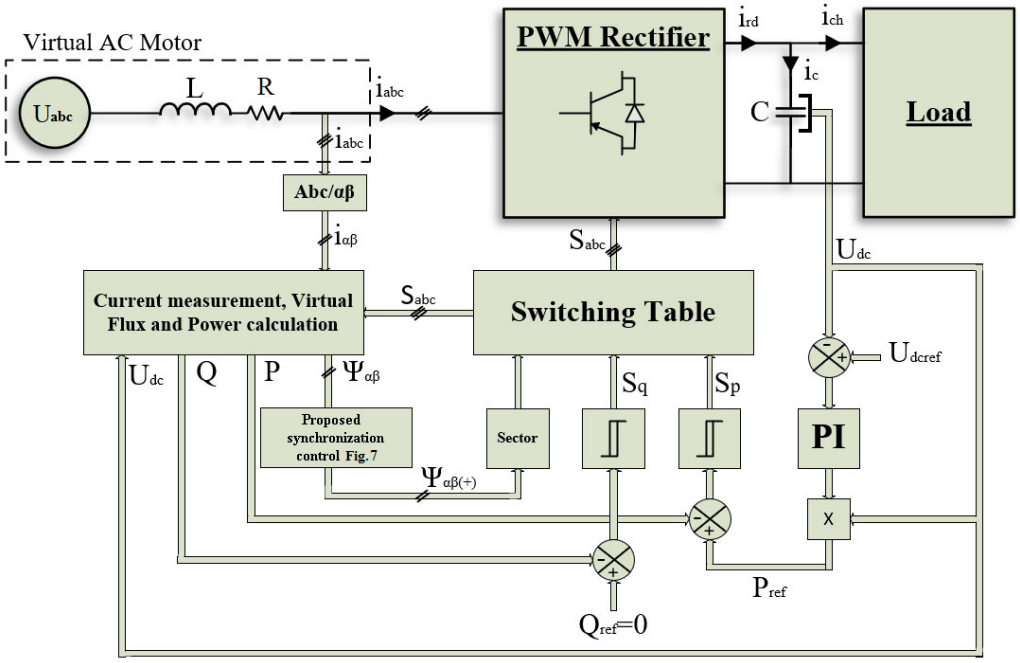


Fig. 6. Structure of modified DPC controller with Dual Virtual Flux

Basically, the Virtual Flux was used as the estimator of the network voltage. The integration feature of our estimator ensures the attenuation of the highest harmonics. The phase angle hence can be calculated directly from the estimated VF. The authors in [20] suggested to introduce the VF into the SRF-PLL basic schema to enhance its performance. In practice, a pure integrator for VF estimation cannot be used because of the problem of its initial value of this pure integrator, which leads the output signal to saturation. A sufficient solution is to replace the pure integrator by a Low-Pass Filter (LPF) with a bandwidth lower than the network frequency and thus obtain the best property of the filter. The disadvantage of VF is a slower response in the time domain.

The solution of this problem is the Dual Virtual Flux (DVF), presented in [20] which gives a much faster time response. Moreover, the decoupling network is used to calculate a signal in two sequences: positive and negative. The use of the proposed DVF-PLL, based on the cascade of two adaptive filters illustrated in Fig. 7, is an optimized solution. The DVF-PLL filter function is based on the estimated voltage and measurements current. First, the voltage

reference signals are expressed in the stationary reference frame ($\alpha\beta$). Then the resistive voltage drop included in the model is subtracted. The latter is shifted in phase (90°) and gains unity for the fundamental frequency used to estimate the VF components with the second-order-low-pass filters. The estimated components of the VF are separated in positive and negative sequences with the same transfer function as that used for the estimation of the VF components. By using the estimated VF components in the stationary reference frame, the flux angles can be estimated by using a conventional Phase Locked Loop (PLL). The cutoff frequency is equal to 50 Hz and only the positive sequence is used to ensure adequate operation under faulty network conditions.

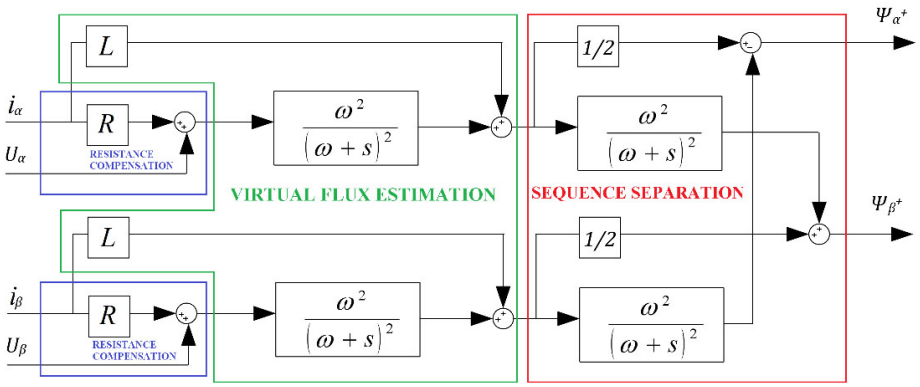


Fig. 7. The diagram of the proposed Dual Virtual Flux estimator

4. Simulation results

To provide benchmarking work, the standard and the proposed method under disturbed voltage conditions are implemented using the MATLAB/Simulink software. Initially, a voltage imbalance of 20% and 7th order harmonic of 20% are created and included in phase *A*. Then, the harmonics 5 and 7 with an amplitude of 20% and the imbalance of 20% are applied, and this represents the worst case of grid voltages. Finally, a voltage imbalance of 20% and 5th order harmonic of 20% are created and included in phase *A*. We define the power fluctuation and the THD factor of input current as comparative criteria to demonstrate the superiority of the proposed strategy using simulation results.

During all the simulations, Q_{ref} is kept at zero to ensure a Unity Power Factor (UPF) operation. The two methods compared are simulated under conditions described as follows:

– ideal network voltage conditions for 0 s $< t <$ 0.2 s and 0.5 s $< t <$ 0.55 s,
– unbalanced and distorted network voltage conditions for 0.2 s $< t <$ 0.5 s,
– 0.6 s $< t <$ 1.1 s U_{dc} goes to 200 V.

The following simulation results are obtained using the values of the parameters given in Table 1. Figs. 9(a–e) show the bus voltage curve, the grid current, the estimated Virtual Flux $\Psi_{\alpha\beta}$, the superposition current i and the voltage V in phase A and the active power P and reactive Q, respectively.

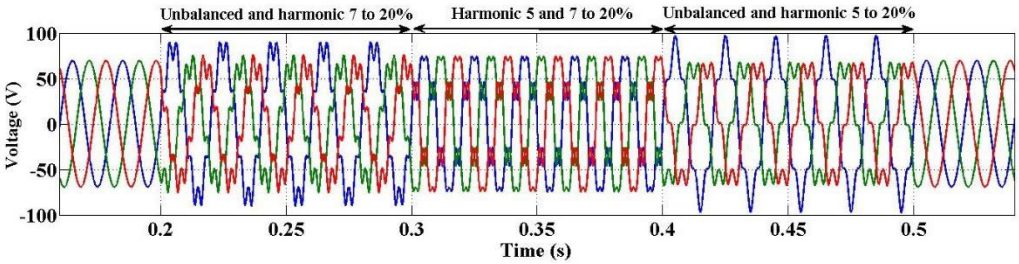


Fig. 8. The different voltage source condition applied to the rectifier

Table 1. The values of the electrical parameters [2]

Electrical Parameter	Symbol	Value	Unit
Resistance	R	0.56	Ω
Inductance	L	19.5	mH
Capacitor	C	1100	μF
Load	RL	68.6	Ω
AC voltage	E	85	$V_{r.m.s}$
Frequency	F	50	Hz
DC-bus voltage	U_{dc}	180	V
Coefficients proportional	K_P	0.04	–
Coefficients integral	K_I	0.81	–

The distribution of Fig. 10 is the same as in Fig. 9. We can see from Fig. 9 the conventional control that leads to fluctuations in the bus voltage curve. In addition, the grid current is affected by disturbed grid voltage conditions, which reduce the accuracy of the estimated flux as can be seen in Fig. 9(c).

In addition, the DC bus oscillates seriously below 5 V and the system does not operate under a unity power factor.

On the other hand, we can see in Fig. 10 that the current and the voltage are in phase. Although there are still some low-order harmonics, we can observe that they have limited influence compared to the one in Fig. 9. The oscillations of the estimated flux vector component $\Psi_{\alpha\beta}$ are sinusoidal and phase-shifted by π without disturbance and the fluctuation of the bus voltage is stabilized at around 2 V.

From Figs. 11-1 and 11-2, we can note that the total harmonic distortion (THD) factor rate of the grid current has been improved compared to the traditional control.

To highlight the contribution of the oscillatory terms, first, the results of the conventional control structure are presented in Fig. 11-2. The design and the optimization process were carried out in a similar way as the procedure presented above. This result expressly shows how the

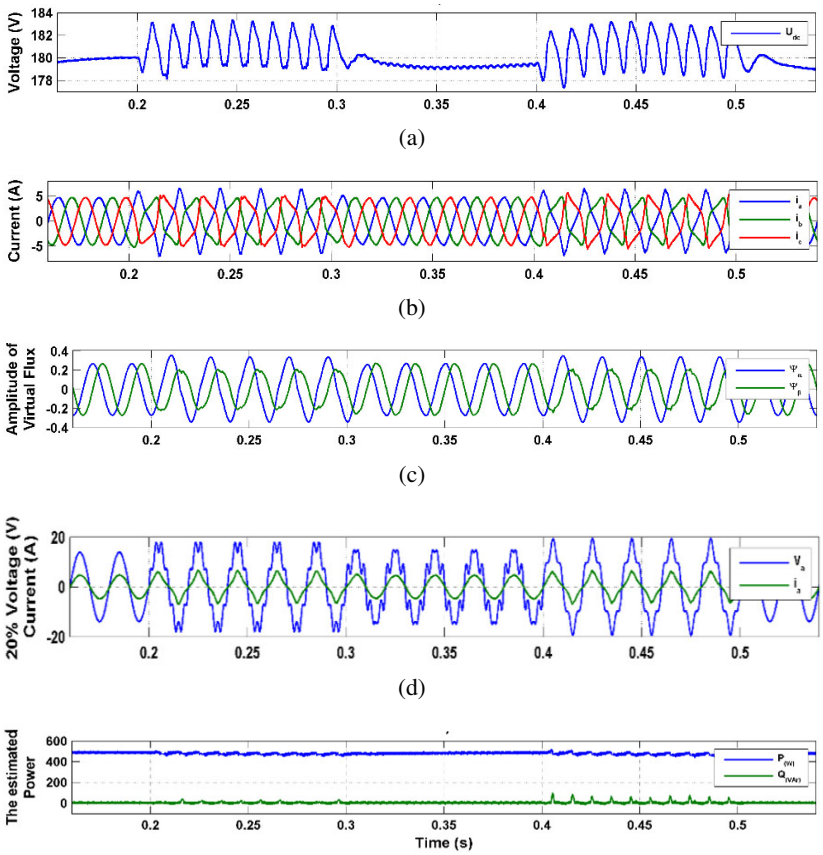
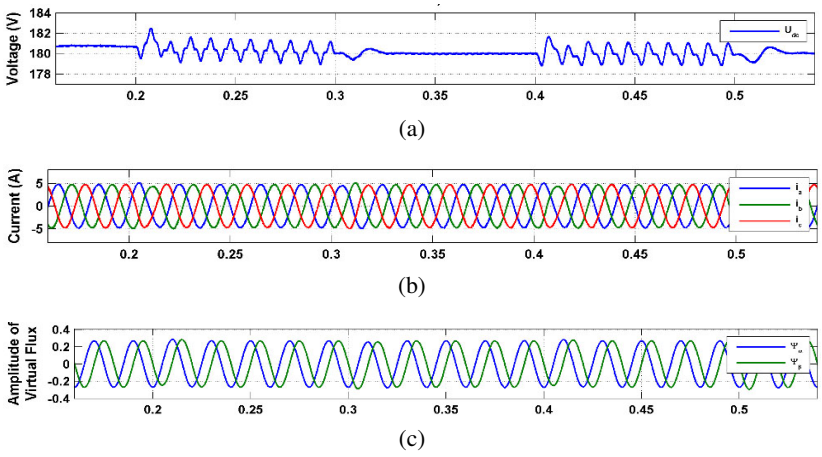
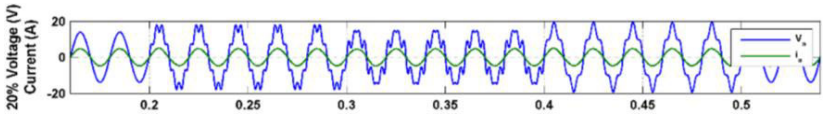
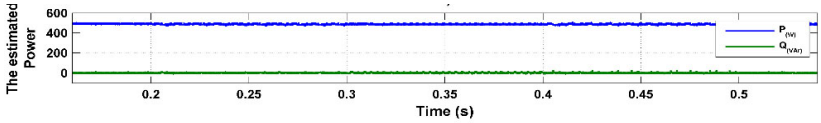


Fig. 9. Simulation results using conventionnel VF-DPC: (a) the bus voltage waveform; (b) current of grid; (c) flux estimation waveform $\alpha\beta$; (d) voltage V_a and current i_a; (e) instantaneous power P and Q





(d)



(e)

Fig. 10. Simulation results using the proposed VF-DPC: (a) the bus voltage waveform; (b) current of grid; (c) flux estimation waveform $\alpha\beta$; (d) voltage V_a and current i_a; (e) instantaneous power P and Q

components of low-order harmonics (5 and 7) with a symmetrical default of the grid voltage affect the grid current. To summarize the results, the following Table 2 presents a comparative analysis based on the current THD between the two strategy controls studied in this article, we note that:

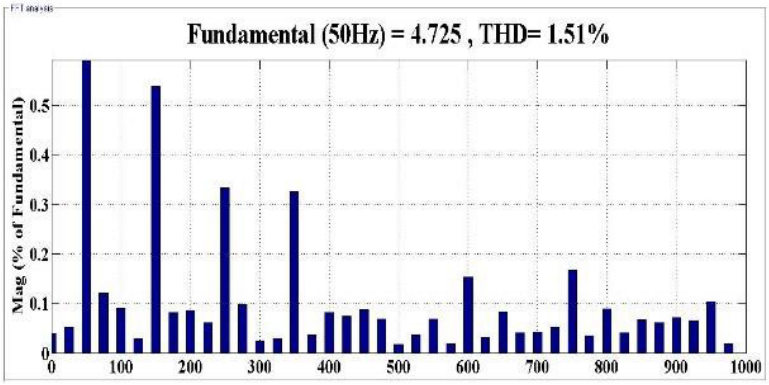
– Case 1: The results obtained from the input current spectrum show that a limitation of harmonic 3 and its multiples which are less than 0.6% of the fundamental and the harmonics 5 and 7 less than 0.4% of the fundamental in the DVF-DPC strategy means that most low-order harmonics are satisfactorily attenuated.
– Case 2: Harmonics 7 and 5 are less than 0.7% when using the DVF-DPC strategy.
– Case 3: The appearance of harmonic 3 and its multiples which are less than 1.6% and a clear reduction of harmonic 5 which is less than 0.5% of the fundamental thanks to the DVF-DPC, strategy unlike VF-DPC, results in no immunity against network pollution.

Table 2. Numerical results of THD factor rate in different cases

Cases	**Unbalance condition 20%**	**Harmonic 5 20%**	**Harmonic 7 20%**	**Applied method**	
				VF-DPC THD	**DVF-DPC THD**
1	Yes	No	Yes	22.38%	1.51%
2	No	Yes	Yes	2.05%	1.53%
3	Yes	Yes	No	20.96%	2.04%

To prove the reliability and robustness of the DVF-DPC, the parameters of the rectifier input filter (R, L) are modified. Fig. 12 illustrates the waveform of the DC bus voltage under the disturbance of the resistance (R~$2R$) as can be seen in Fig. 12(a) and the inductance (L~$2L$) as can be seen in Fig. 11(b). In Fig. 12, we can see that the DC bus voltage can quickly converge towards the desired value. This means that the improved control ensures satisfactory performance with various parameters.

1



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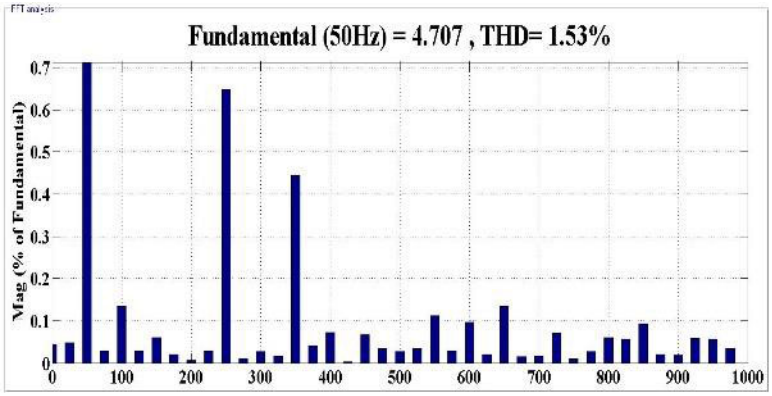

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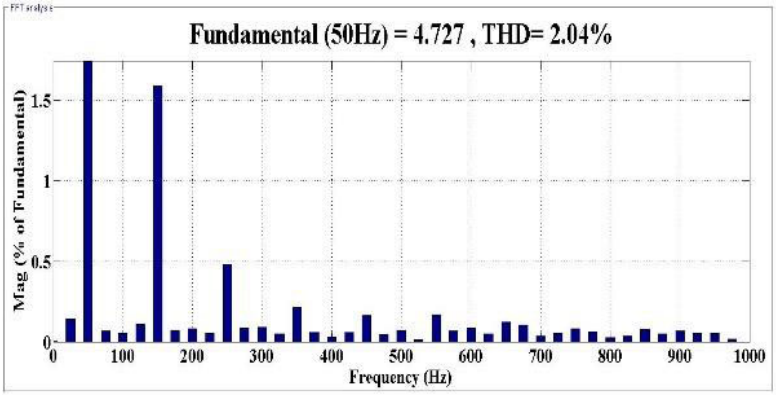

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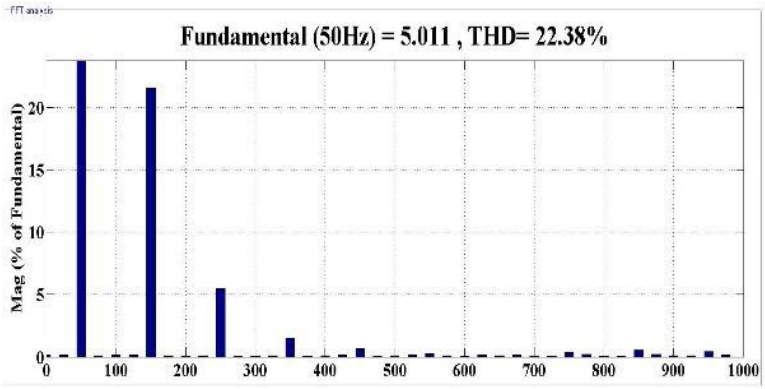

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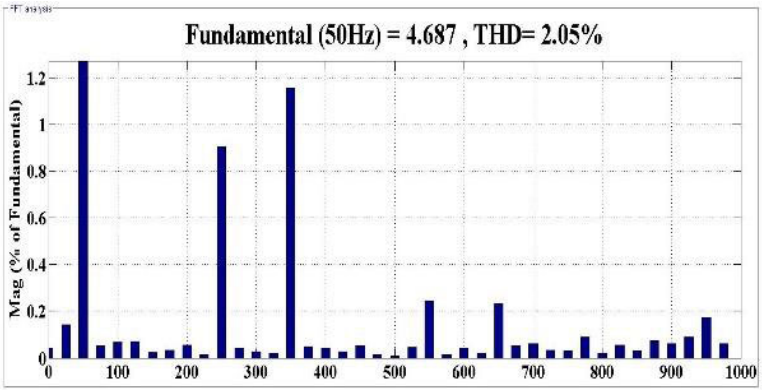

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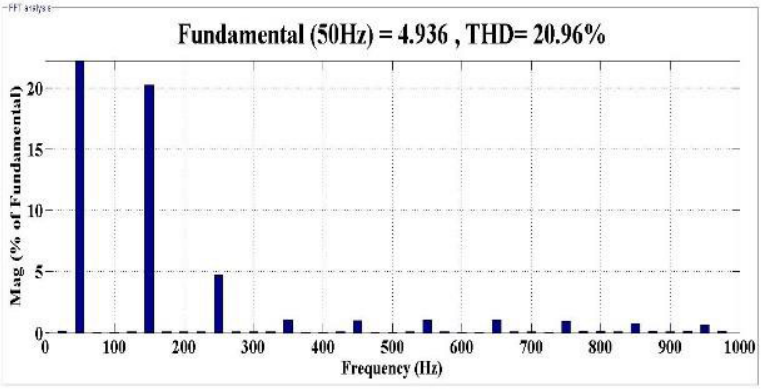
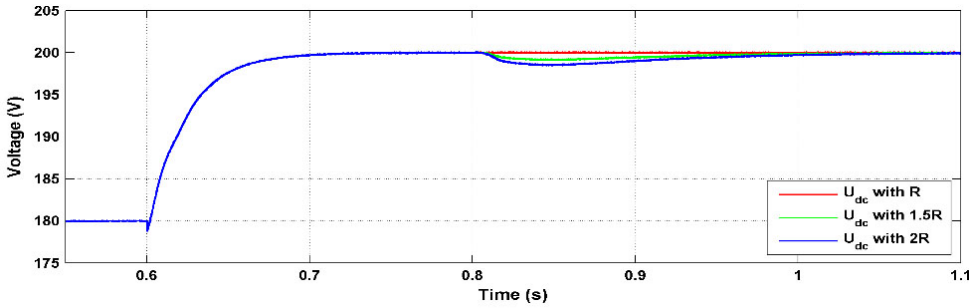
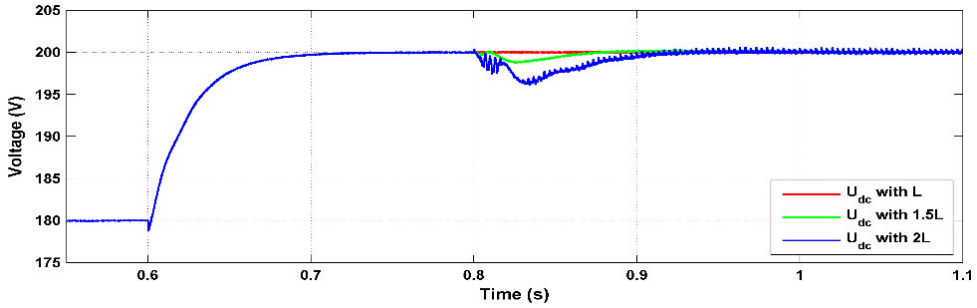


(c)

Fig. 11. FFT analysis showing THD in source current of both methods, 1 – proposed and 2 – conventional, under different network voltage conditions: (a) unbalanced and harmonic 7th; (b) harmonic 5th and 7th; (c) unbalanced and harmonic 5th



(a)



(b)

Fig. 12. System parameters influence on the evolution of the DC bus voltage: *R* (a); *L* (b)

5. Conclusions

This paper has presented the mathematical analysis and numerical implementation of a DPC-based enhanced Dual Virtual Flux (DVF-DPC) method for three-phase PWM rectifiers. The main objectives of the proposed control strategy are obtaining sinusoidal input currents under different input voltage conditions and maintaining the DC bus voltage at the required level.

In these situations, components of harmonics appear on the network voltage, causing current distortion and imbalance if the power reference is kept constant. However, the use of the DVF, which is based on the principle of disturbance rejection, leads to achieving a low THD input current compared to the conventional method.

The proposed control method could offer many advantages and achieves good performance with less calculation burden, without the need to specify the power calculation term, nor to extract positive/negative voltage sequence. It can therefore be said that this control method is capable of improving the quality of the input current.

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