Distributed Electrothermal Modeling Methodology for MOS Gated Power Devices Simulations

Emmanuel Marcault, Patrick Tounsi, Jean-Luc Massol, and Jean-Marie Dorkel

***Abstract*—Currently electro-thermal simulations performed with 3D FEM simulators like ANSYS or COMSOL Multiphysics are limited to an imposed current flow through resistive materials. However, in the case of power MOS gated transistors like VDMOS transistors or IGBT, the channel resistance evolves with the gate voltage. This phenomenon is usually neglected in ON-state applications but seems to be determinant in switching application. Furthermore all the MOS cells of the transistors are not at the same temperature. This paper deals with a methodology that could allow taking into account the impact of the gate control and the MOS cells current distribution during 3D FEM electro-thermal simulations.**

***Index Terms*—Electro-thermal simulations, Reliability, 3D FEM simulations**

I. INTRODUCTION

PRESENTLY, electro-thermo-mechanical simulations are of great interest for studying and improving the reliability of the power components.

Indeed, they allow performing detailed analysis of phenomena like focalization of the temperature and current densities due to the structure topology [1] which may explain the failure by melting of a bonding wire. This kind of simulation is also of great interest for the study of material resistivity variation that occurs during component ageing [2] and allow to obtain good results close to the experiment. However, these simulations performed with 3D FEM simulators like ANSYS or COMSOL Multiphysics are limited to an imposed current flow through resistive materials (figure 1) and sometime, it’s could be insufficient. Specially, in the case of power MOS gated transistors like VDMOS transistors or IGBT, why the channel resistance is modified with the gate voltage, temperature and many other phenomena.

Thereby, it should be interesting to include these phenomena by using electrical models like SPICE, VHDL-AMS … to describe the real component behavior [3].

Moreover, the 3D FEM simulations do not model phenomena like current focalization in a cell which may result in a hot spot apparition leading to cell destruction (figure 2). To model this kind of failures, it would be necessary to dissociate the different cells within of the power device.

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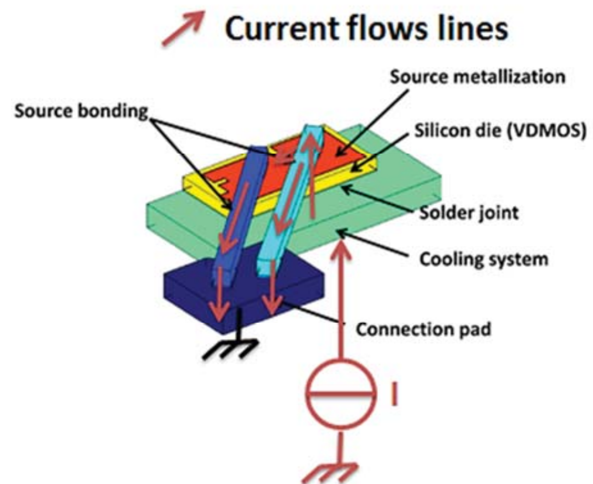

Fig. 1. Principle of conventional 3D electrothermal simulation.

II. A STUDIED CASE SHOWING THE LIMITATIONS OF THE "CLASSICAL" TECHNIQUE

The studied case presented here concerns the impact on the top metallization ageing on the electro thermal behavior of a power device. The power semiconductor device used to carry out the experiment is operated in ON-OFF mode. Experimental conditions are the following: the ambient temperature is maintained at 70°C, a drain current of 85A is imposed to flow through the device for about 5.5ms. This cycle is repeated up to 250 000 times. It results in a degradation of the top metallization appreciated by comparing fig. 2 a and b (initial state and after 250 kcycles respectively) due to the mechanical stress. For the aged metallization (b), the number of aluminum grains increases and their size decreases [4].

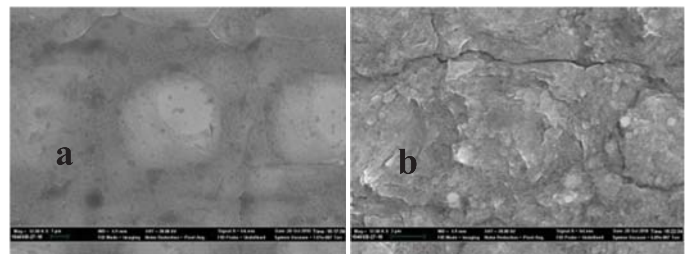

Fig. 2. a) SEM observation of top metallization before ageing;
b) SEM observation of top metallization after an ageing of 250 kcycles.

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To model these phenomena, two sets of simulations were performed by changing the thermal and the electrical resistivities of the top metallization as present figure 3.

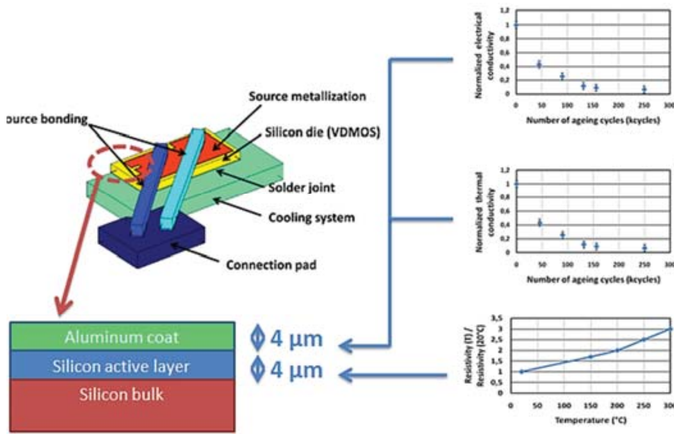

Fig. 3. Principle of conventional 3D electrothermal simulation taking into account material evolution during ageing.

A. Simulations results

One can observe figure 4 that the simulation results obtained by this method and the infrared measurement are in agreement till 50 kcycles. Indeed, from 150 kcycles materials defect (figure 5) appears and cause hot spots. That is not taking into account on the simulations. Thereby, to model this kind of failures, it would be necessary to dissociate the different cells within of the power device.

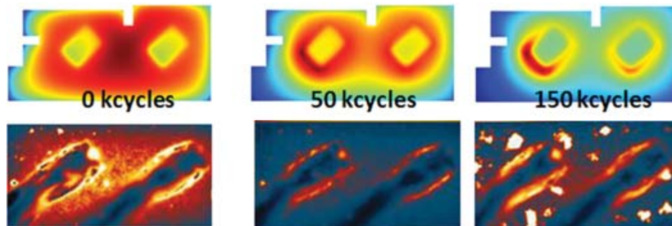

Fig. 4. Simulation and experimental results showing the evolution in the temperature distribution as function of source.

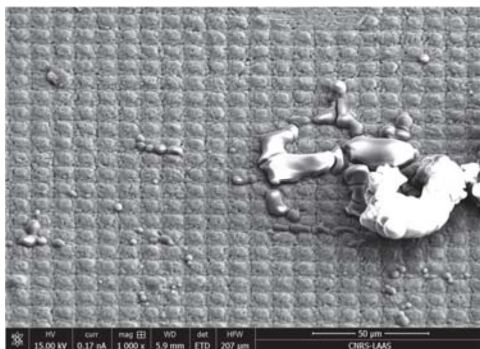

Fig. 5. SEM imaging focusing on a defect occurred during ageing test

III. Distributed Electrothermal Simulations

A. Distributed electrical simulation

As the gate voltage distribution effect appears to be negligible [5] for the studied switching frequencies, one could consider that the transistor cells share the same gate-source potential. Thereby, only the source potential was distributed on a 3D FEM structure. This structure presented in figure 6 is representative to the source metallization and the wire bonding of a power device connected to 16 MOS "macro-cells".

One could note that due to a scaling problem between the cells and the whole component, it is not possible to model each cell. That is why, we actually defined "macro-cells" representing a group of elementary cells and that we simply call "cells".

Associated to this geometry, a SPICE netlist composed of 16 MOS cells was added to take into account MOS electrical parameters as R_G, C_{GD}, C_{GS}, … The MOS model used here is the model already implemented in the COMSOL data given figure 6 [6].

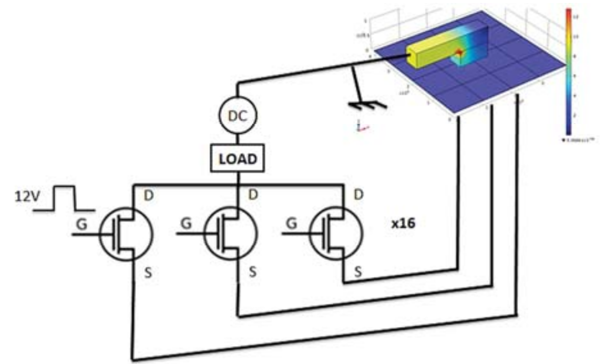

Fig. 6. 3D source potential distribution.

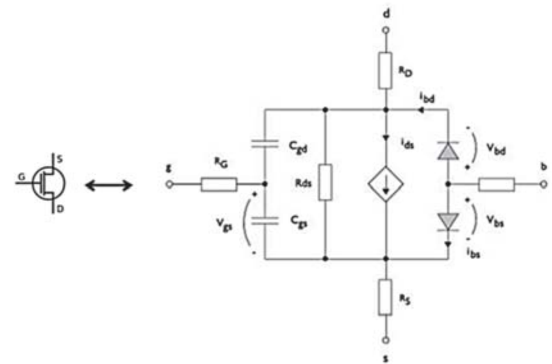

Fig. 7. MOS transistor spice circuit [4].

Wherein the drain current is expressed as :

$$i_{ds} = \begin{cases} \frac{W}{L}\frac{K_P}{2}(1+\Lambda v_{ds})v_{ds}(2v_{th}-v_{ds}) & v_{ds} < v_{th} \\ \frac{W}{L}\frac{K_P}{2}(1+\Lambda v_{ds}){v_{th}}^2 & v_{ds} \geq v_{th} \\ 0 & v_{ds} < v_{th} \leq 0 \end{cases}$$

with the drain saturation voltage:

$$v_{th} = v_{gs} - V_T$$

As the threshold voltage (V_T) and transconductance (K_P) are sensitive to temperature effect, we extract MOS parameters from experimental measurement at further temperatures which allow us to identify the following expressions:

$$K_P = K_{P0} - \frac{\Delta K_P}{\Delta T}(T - T_0)$$

and

$$V_T = V_{T0} - \frac{\Delta V_T}{\Delta T}(T - T_0)$$

The model parameters as the follows:

TABLE I
VDMOS SPICE PARAMETERS

Parameter	*Value*	*Description*
T_0	25°C	Reference temperature
W	10E-6 [m]	Gate Width
L	2E-6 [m]	Gate Length
K_{P0}	4 [A/V²]	Transconductance at T_0
Λ	1	Channel length modulation
v_{ds}	0-12 [V]	Drain-source voltage
v_{gs}	0-12 [V]	Gate-source voltage
V_{T0}	4,22 [V]	Threshold voltage at T_0
$\frac{\Delta K_P}{\Delta T}$	0,0044	
$\frac{\Delta V_T}{\Delta T}$	0,0029	

Thus, this model exhibits the following behavior of the drain current as function of the gate-source voltage (figure 8) and the drain current as function of the drain source voltage (figure 9) for further temperatures.

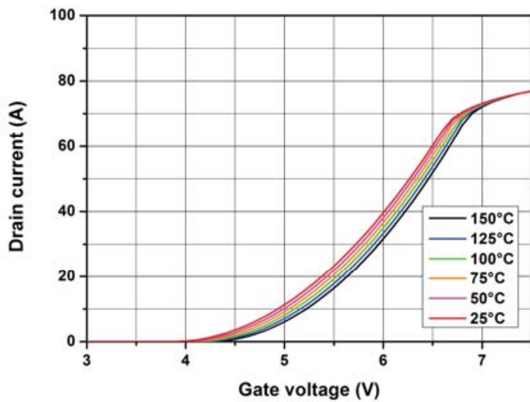

Fig. 8. Drain current as a function of gate-source voltage for different ambient temperature values.

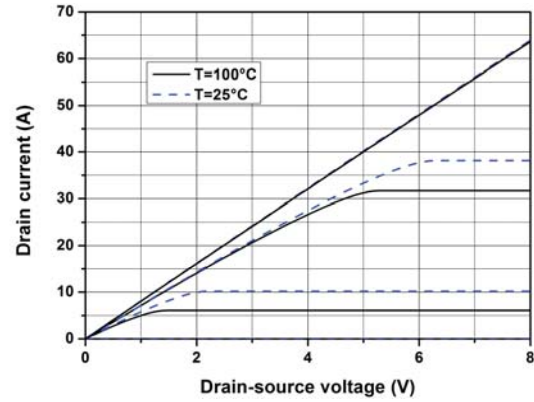

Fig. 9. Drain current as a function of drain voltage for different gate-source voltage and temperature values.

This electrical simulation allows computing the current drain and the drain-source voltage of each MOS cell within the transistor. Consequently, it becomes possible to compute the dissipated power in each MOS cell and in the transistor during MOS switching (figure 10). For the sake of the methodology illustration, the rise time is deliberately long: 100ms.

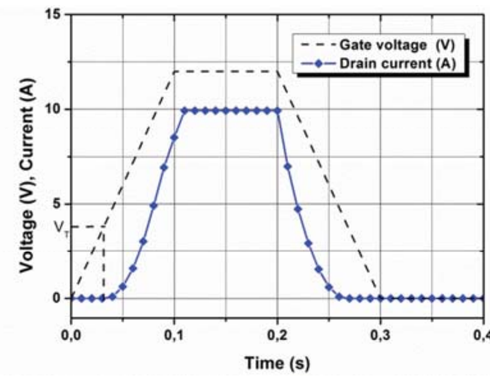

Fig. 10. Drain current evolution of the transistor during switching at 25°C and without thermal feedback.

B. Distributed thermal simulation

The induced temperature can be calculated by injecting the dissipated power in a second 3D structure (figure 11). In this structure, 16 active areas where the power is injected are added under the source metallization and a silicon bulk with boundary conditions corresponding to a cooling system is also added. All other boundaries are thermally insulated.

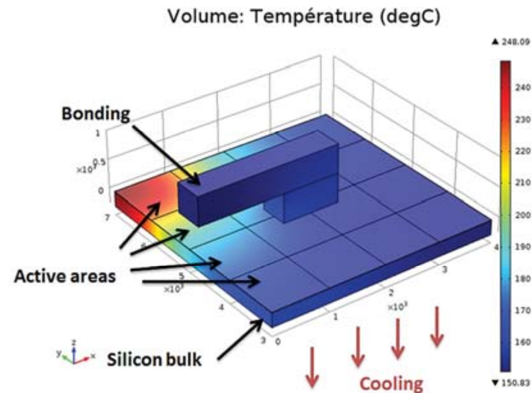

Fig. 11. 3D source potential distribution.

C. *Distributed electro-thermal simulation*

The developed method (validated for 16 cells) runs as follows:

1. The current and potential calculated using the electrical SPICE model of lateral MOS presented previously give the instantaneous power dissipated in each cell and for each time step of the simulation.
2. This instantaneous power is injected into the "active zones" of the thermal 3D FEM model (Figure 11), wherein the SPICE model is linked to the corresponding area.
3. The temperature of each cell is injected to the electric model corresponding to the time step.
4. This procedure is repeated at each time step of the simulation as presented in figure 12.

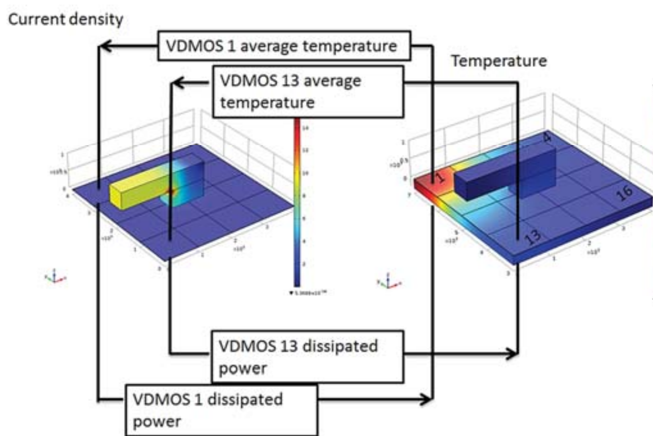

Fig. 12. Distributed electro-thermal simulation.

According to this procedure, the simulation results presented in figure 13 shows that the “ON” state leads to an increase in temperature due to the drain current conduction. Over this, compared with the purely electrical simulation which doesn’t take into account the temperature effect (figure 14), the temperature increase leads to a decrease of the drain current of about 2% at the end of the “on” state duration. This is due to the temperature influence on the SPICE parameters presented table1.

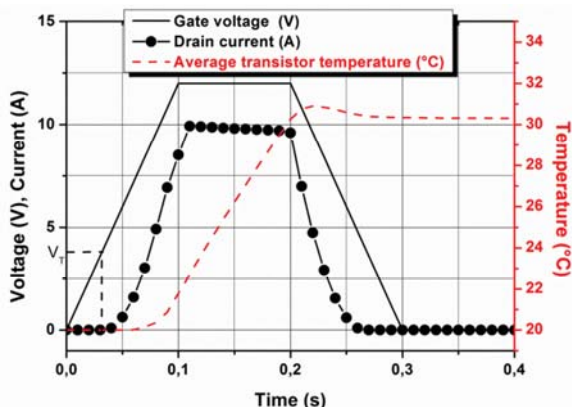

Fig. 13. Drain current and temperature evolution of the transistor during switching at 25°C.

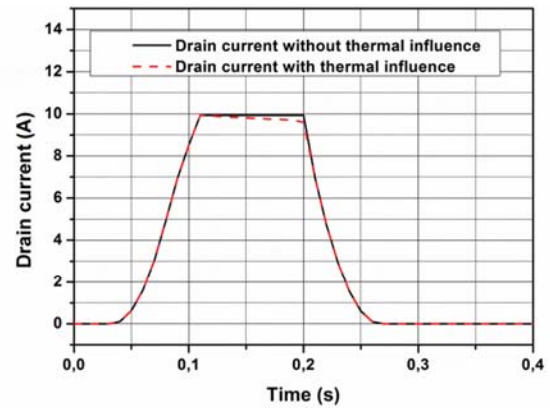

Fig. 14. Drain current evolution of the transistor during switching at 25°C, without and with thermal influence on the MOS transistor according equation 1.

IV. Application Note

According to this electrothermal simulation methodology, it becomes possible to study the impact of most MOS parameters drift during the MOS transistor ageing like local increase in serie resistance or threshold voltage variation.

A. *Case of a more resistive cell*

The distribution of 16 cells in the structure allows monitoring current and temperature in each cell. Thus, in the case of a more resistive MOS transistor cell (cell 6), that is made more resistive by increase in its serie resistance (R_S figure 4) from 0 to 10 mΩ, while the other cells have a 0 mΩ serie resistance (figure 15), one could observe that the more resistive cell (cell 6) has a lower temperature than the others (figure 15). This is due to the lower current flowing through compare to the other cells.

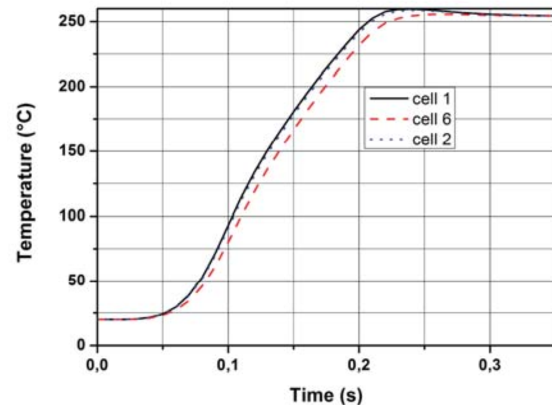

Fig. 15. Temperature evolution in two cells with different resistivities during switching (for indexing cells, see figure 12).

B. *Case of a cell with a lower threshold voltage*

In the same way, it becomes possible to study the impact of a MOS parameter drift like the threshold voltage. For this, we assume in the SPICE model that a cell has a threshold voltage of 2V whereas the others have a threshold voltage of 4V. Therefore, during the MOS transistor switching the cell having a lower threshold voltage “allows” current to pass before the other and begins to heat earlier (figure 16).

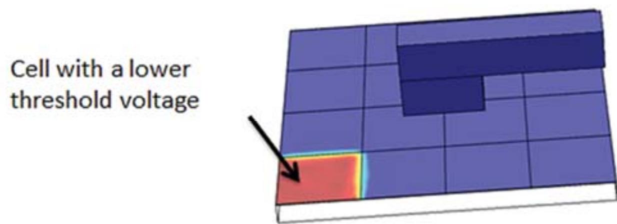

Fig. 16. Conduction of a cell having a lower threshold voltage than the other cells during MOS transistor switching (t=55ms).

V. Conclusion

The simulation methodology presented in this paper allows taking into account the real behavior of gated component (MOS, VDMOS, IGBT …) using the benefits of SPICE models coupling with the benefits of 3D FEM simulators. Indeed the SPICE simulators allow to take into account component characteristics as R_G, C_{GD}, C_{GS}, … and the 3D FEM simulator allows to take into account the component geometry (metallization, wire bonding, …) to compute potential and thermal distribution.

Thereby, it allows the study of phenomena hitherto difficult to model like current repartition due to conductance variation in the transistor cell, inhomogeneity between the threshold voltages of the various cells (figure 14).

Acknowledgement

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References

[1] J.B. Sauveplane, P. Tounsi, A. Deram, E. Scheid, X. Chauffleur, "Smart 3-D Finite-Element Modeling for the Design of Ultra-Low On-Resistance MOSFET", *Advanced Packaging, IEEE Transactions on*, vol. 30, no.4, pp.789-794, Nov. 2007

[2] E. Marcault, M. Breil, A. Bourennane, P. Tounsi, D. Martineau, P. Dupuy, "Impact of source metallization ageing on thermo-mechanical characteristics of a vertical power device", *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on* , vol., no., pp.1-7, Aug. 30 2011-Sept. 1 2011

[3] H. Dia, J.B. Sauveplane, P. Tounsi, J.-M. Dorkel, "A temperature-dependent power MOSFET model for switching application", *Thermal Investigations of ICs and Systems, 2009. THERMINIC 2009. 15th International Workshop on* , vol., no., pp.87-90, 7-9 Oct. 2009

[4] D. Martineau, T. Mazeaud, M. Legros, Ph. Dupuy; C. Levade, G. Vanderscaeve, "Characterization of ageing failures on power MOSFET devices by electron and ion microscopies", *Microelectronics and reliability*; 2009, vol. 49, n°9-11

[5] E. Marcault, J.L. Massol, P. Tounsi, J.-M. Dorkel, "Distributed electrothermal modeling methodology for MOS gated powerdevices simulations", 20th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES) 2013

[6] COMSOL® version 4.3a user guide concerning circuit module, 2012

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