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Basic Aspects of Designing a High-performance Processor Structure for Calculating a “true” Discrete Fractional Fourier Transform

Abstract

This paper presents a basic aspects of structural design of the high-performance processor for implementation of discrete fractional Fourier transform (DFrFT). The general idea of the possibility of parallelizing the calculation of the so-called “true” discrete Fourier transform on the basis of our previously developed algorithmic approach is presented. We specifically focused only on the general aspects of the organization of the structure of such a processor, since the details of a particular implementation always depend on the implementation platform used, while the general idea of constructing the structure of the processor remains unchanged.

Keywords: discrete fractional Fourier transform, parallelization of computations, hardware implementation, complexity reduction.

1. Introduction

The discrete fractional Fourier transform has been found many applications in various areas of digital signal and image processing such as signal and image recovery, image restoration and enhancement, image encryption and compression, pattern recognition, digital watermarking, radars [1-8]. The problem of a fast implementation of the DFrFT becomes extremely important for applications requiring real-time processing at high throughput especially in digital signal and image processing. Hence, to meet the stringent requirements to throughput, latency, and power-consumption constraints of real-time DSP systems, developing dedicated hardware implementations, such as application specific integrated circuits (ASICs) or field-programmable gate arrays (FPGAs), has of paramount importance [9-11]. In this paper, we focus on the basic aspects of structural implementation of the algorithmic solution, which was presented in [12], [13]. We named this type of algorithm as “true” DFRFT [13].

2. Preliminaries

A one-dimensional DFrFT can be expressed as a matrix-vector multiplication:

$$\mathbf{Y}_{N \times 1}^{(\alpha)} = \mathbf{F}_N^{(\alpha)} \mathbf{X}_{N \times 1} \quad (1)$$

where $\mathbf{X}_{N \times 1} = [x_0, x_1, \dots, x_{N-1}]^T$ is the input vector which has N elements, $\mathbf{F}_N^{(\alpha)}$ is the discrete fractional transform matrix and α is the fractional order.

The transform matrix of the DFrFT can then be defined as [3]

$$\mathbf{F}_N^{(\alpha)} = \left\| f_{k,n}^{(\alpha)} \right\| = \mathbf{Z}_N \mathbf{\Lambda}_N \mathbf{Z}_N^T \quad (2)$$

Where $k, n = 0, 1, \dots, N-1$, $\mathbf{\Lambda}_N$ is a diagonal matrix of size N , whose diagonal entries are the eigenvalues of the matrix \mathbf{E}_N , \mathbf{Z}_N is the matrix whose columns are normalized mutually orthogonal, eigenvectors of the matrix \mathbf{E}_N and $\mathbf{E}_N = \left\| w_N^{(k,n)} \right\|$ is the matrix of discrete exponential functions [14], $w_N^{(k,n)} = \exp(-j2\pi kn/N)$, and $j = \sqrt{-1}$ is an imaginary unit.

Direct calculation of matrix-vector product (1) requires N^2 multiplication and $N(N-1)$ additions. In some cases, this leads to a significant time delay. Below, we show how to reduce the computation time of DFrFT.

3. Algorithmic and structural aspects of DFrFT processor organization

We will write the matrix $\mathbf{F}_N^{(\alpha)}$ as a sum of three or two matrices and these matrices will have special structures as well. This trick may be useful to reduce the number of arithmetical operations when calculating a product of the matrix $\mathbf{F}_N^{(\alpha)}$ by a vector. The number of components of the sum depends on whether N is even or odd.

If N is even, the matrix $\mathbf{F}_N^{(\alpha)}$ can be written as a sum of three matrices

$$\mathbf{Y}_{N \times 1}^{(\alpha)} = \mathbf{F}_N^{(\alpha)} \mathbf{X}_{N \times 1} = \mathbf{A}_N^{(\alpha)} \mathbf{X}_{N \times 1} + \mathbf{B}_N^{(\alpha)} \mathbf{X}_{N \times 1} + \mathbf{C}_N^{(\alpha)} \mathbf{X}_{N \times 1} \quad (3)$$

where

$$\mathbf{A}_N^{(\alpha)} = \begin{bmatrix} f_{0,0}^{(\alpha)} & f_{0,1}^{(\alpha)} & \Lambda & f_{0,\frac{N}{2}-1}^{(\alpha)} & f_{0,\frac{N}{2}}^{(\alpha)} & f_{0,\frac{N}{2}+1}^{(\alpha)} & \Lambda & f_{0,1}^{(\alpha)} \\ \hline f_{0,1}^{(\alpha)} & 0 & \Lambda & 0 & 0 & 0 & \Lambda & 0 \\ \text{M} & \text{M} & \text{O} & \text{M} & \text{M} & \text{M} & \text{O} & \text{M} \\ f_{0,\frac{N}{2}-1}^{(\alpha)} & 0 & \Lambda & 0 & 0 & 0 & \Lambda & 0 \\ f_{0,\frac{N}{2}}^{(\alpha)} & 0 & \Lambda & 0 & 0 & 0 & \Lambda & 0 \\ f_{0,\frac{N}{2}+1}^{(\alpha)} & 0 & \Lambda & 0 & 0 & 0 & \Lambda & 0 \\ \text{M} & \text{M} & \text{O} & \text{M} & \text{M} & \text{M} & \text{O} & \text{M} \\ f_{0,1}^{(\alpha)} & 0 & \Lambda & 0 & 0 & 0 & \Lambda & 0 \end{bmatrix},$$

$$\mathbf{B}_N^{(\alpha)} = \begin{bmatrix} 0 & 0 & \Lambda & 0 & 0 & 0 & \Lambda & 0 \\ 0 & f_{1,1}^{(\alpha)} & \Lambda & f_{1,\frac{N}{2}-1}^{(\alpha)} & 0 & f_{1,\frac{N}{2}+1}^{(\alpha)} & \Lambda & f_{1,N-1}^{(\alpha)} \\ \text{M} & \text{M} & \text{O} & \text{M} & \text{M} & \text{M} & \text{O} & \text{M} \\ 0 & f_{1,\frac{N}{2}-1}^{(\alpha)} & \Lambda & f_{\frac{N}{2}-1,\frac{N}{2}-1}^{(\alpha)} & 0 & f_{\frac{N}{2}-1,\frac{N}{2}+1}^{(\alpha)} & \Lambda & f_{1,\frac{N}{2}+1}^{(\alpha)} \\ \hline 0 & 0 & \Lambda & 0 & 0 & 0 & \Lambda & 0 \\ 0 & f_{1,\frac{N}{2}+1}^{(\alpha)} & \Lambda & f_{\frac{N}{2}-1,\frac{N}{2}+1}^{(\alpha)} & 0 & f_{\frac{N}{2}-1,\frac{N}{2}-1}^{(\alpha)} & \Lambda & f_{1,\frac{N}{2}-1}^{(\alpha)} \\ \text{M} & \text{M} & \text{O} & \text{M} & \text{M} & \text{M} & \text{O} & \text{M} \\ 0 & f_{0,N-1}^{(\alpha)} & \Lambda & f_{1,\frac{N}{2}-1}^{(\alpha)} & 0 & f_{1,\frac{N}{2}-1}^{(\alpha)} & \Lambda & f_{1,1}^{(\alpha)} \end{bmatrix},$$

$$\mathbf{C}_N^{(\alpha)} = \begin{bmatrix} 0 & 0 & \Lambda & 0 & 0 & 0 & \Lambda & 0 \\ 0 & 0 & \Lambda & 0 & f_{1,\frac{N}{2}}^{(\alpha)} & 0 & \Lambda & 0 \\ \text{M} & \text{M} & \text{O} & \text{M} & \text{M} & \text{M} & \text{O} & \text{M} \\ 0 & 0 & \Lambda & 0 & f_{\frac{N}{2}-1,\frac{N}{2}}^{(\alpha)} & 0 & \Lambda & 0 \\ \hline 0 & f_{1,\frac{N}{2}}^{(\alpha)} & \Lambda & f_{\frac{N}{2}-1,\frac{N}{2}}^{(\alpha)} & f_{\frac{N}{2},\frac{N}{2}}^{(\alpha)} & f_{\frac{N}{2}-1,\frac{N}{2}}^{(\alpha)} & \Lambda & f_{1,\frac{N}{2}}^{(\alpha)} \\ 0 & 0 & \Lambda & 0 & f_{\frac{N}{2}-1,\frac{N}{2}}^{(\alpha)} & 0 & \Lambda & 0 \\ \text{M} & \text{M} & \text{O} & \text{M} & \text{M} & \text{M} & \text{O} & \text{M} \\ 0 & 0 & \Lambda & 0 & f_{1,\frac{N}{2}}^{(\alpha)} & 0 & \Lambda & 0 \end{bmatrix}.$$

Thus, the proposed solutions make it possible to accelerate the implementation of the DFrFT not only by parallelizing computations, but also by reducing the number of required arithmetic operations.

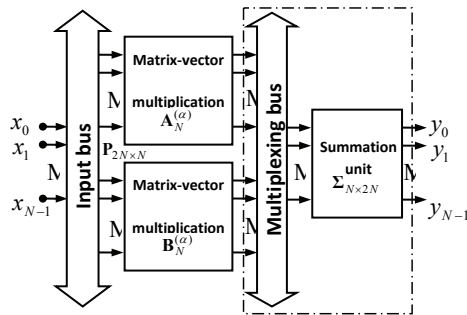


Fig. 2. General structure of DFrFT processing system for odd length N

In our previous work [12], we presented solutions leading to a reduction in the number of arithmetic operations in the calculation of the matrix-vector products under discussion. The corresponding results are presented in Table 1 and Table 2.

Tab. 1. Computation complexity of the proposed solution for even N

Operation type	$A_N^{(\alpha)} X_{N \times 1}$	$B_N^{(\alpha)} X_{N \times 1}$	$C_N^{(\alpha)} X_{N \times 1}$	Summing
additions	$N-1$	$N(N-2)/2$	$N-2$	$2N-3$
multiplications	$N+1$	$N(N-2)^2/2$	$N-1$	

Tab. 2. Computation complexity of the proposed solution for odd N

No.	$A_N^{(\alpha)} X_{N \times 1}$	$B_N^{(\alpha)} X_{N \times 1}$	Summing
additions	$N-1$	$(N-1)(N+1)/2$	$N-1$
multiplications	N	$(N-2)^2/2$	

4. Conclusions

In the paper, some aspects of the algorithmic and structural organization of the processor for computing of the fractional discrete Fourier transform were considered. It is shown that for processing even-length sequences, three matrix-vector multiplication units, two data buses, and one summing unit are necessary. To process sequences of odd length, only two three matrix-vector multiplication units, two data buses and one summing block are needed. The specific implementation of such a processor will depend on the chosen microelectronic platform. It can be a many-core VLSI, where the cores will calculate the corresponding vector-matrix products, or FPGA with embedded PC processor blocks which will be used as matrix-vector multipliers.

5. References

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