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Selection of 5 kW Converter Leg for Power Electronic System

Abstract

Three converter leg variants are analyzed for low power converter used for power electronic system for residential buildings. The two-level Si-IGBT and SiC-MOSFET converters are compared with Si-IGBT three-level T-type converter. Power losses generated in each of these converters over a predicted period of 20 years of operation are contrasted with the cost of converter options. The detailed selection procedure for output inductor is presented in this paper. This procedure shows the influence of the inductor parameters like number of turns, air gap length on its losses, cost and size. Theoretical approach is verified with simulations and experimental results.

Keywords: IGBT, Silicon Carbide (SiC), MOSFET, Inverter, Microgrid.

1. Introduction

With the increased usage of electrical energy from renewable energy sources there is a growing need to utilize that energy in the most effective way [1]. Among the main solutions, which fulfill such requirement, there are decentralized local microgrids which are part of more general concept of the smart grid [2]. These microgrids can be divided into smaller electrical systems e.g. in residential buildings which are called nanogrids [3]. They can be either ac or dc systems, but due to the focus on effectiveness of such systems the dc nanogrids are more preferable options [4]. The dc nanogrid distribution system can be build from many converters connected into a common dc-link or, as is presented Fig. 1, the whole dc nanogrid system can be a part of the power electronic converter which is referred here as power electronic system.

This paper deals with the selection procedure for converter leg which can be used in all component converters of the power electronic system. The paper focuses on the converter with the dc voltage equal to 380 V, which is suitable for single-phase power electronic system and future dc microgrids.

2. Selection of the converter topology

In this paragraph three different variants of converter legs are investigated, among them there are:

- Si-IGBT two-level converter leg (referred as Si-IGBT 2L converter),
- Si-IGBT three-level NPC type T converter leg (referred as Si-IGBT T-type converter),
- SiC-MOSFET two level converter leg (referred as SiC-MOSFET 2L converter).

Schematics of these converter leg variants are shown in Fig. 2. These topologies are chosen because they are among the most promising for their use in the power electronic system (Fig. 1).

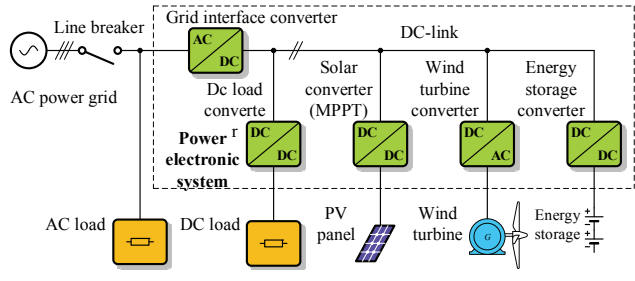

Fig. 1. General structure of the power electronic system for residential buildings

The first variant has the topology of a classical two-level converter. This topology is the most mature and Si-IGBT modules, due to their widespread use, are among the cheapest switching devices. The second variant (with SiC MOSFETs) allows operating with a high switching frequency, which can lead to the significant size reduction of the output inductor. The third variant, the T-type converter, allows reducing the ac output filter size due to a better output voltage waveform compared to both two-level converters together with offering a better efficiency compared to the Si-IGBT 2L converter.

It is assumed that all converters are constructed with switching devices with blocking voltage ratings of 1200 V (or 600 V for RB IGBT in T-type converter). It is due to the fact that the proposed converter leg can be used in three-phase converters with the dc voltage up to 800 V. In the paper the following modules are chosen:

- Infineon Si-IGBT two-level two-leg module F4-75R12KS4;
- Cree SiC MOSFETs C2M0080120D with antiparallel diodes C4D20120D;
- Fuji Electric Si-IGBT three-level three-leg T-type module 12MBI75VN-120-50.

All converter variants are analyzed in the paper in the topology of H-bridge converter supplied from a dc voltage source $V_{dc} = 380$ V operating with resistive-inductive load with the output power of 5 kW.

3. Power loss analysis

In this paragraph power loss analysis of all three converter variants is presented. This analysis include conduction and switching power losses basing on the analytical expressions and simulation models developed in GeckoCIRCUITS simulator. This analysis is also verified experimentally.

Many papers deal with the issue of power losses generated in switching devices of the two-level [5] and T-type converters [6], [7]. Basing on analytical expressions provided for such converters power losses are established for all three variants with different types of IGBT and MOSFET modules. Due to space limitation the analytical expressions are presented here only for both two-level converters as in (1)-(4). The analytical equations describing power losses in T-type converter are given in [8].

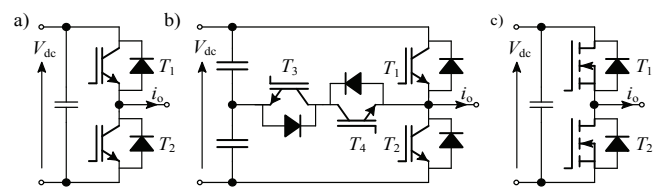

Fig. 2. General structure of the power electronic system for residential buildings

Equations (1) express the conduction power losses in all four transistors PTcon and diodes PDcon of the H-bridge converter with two-level converter legs:

$$P_{\mathrm{Tcon}} = 4\left(\frac{1}{2}I_{\mathrm{m}}V_{\mathrm{T0}}\left(\frac{1}{\pi}+\frac{m_{\mathrm{a}}}{4}\cos(\varphi)\right)+I_{\mathrm{m}}^{2}r_{\mathrm{T}}\left(\frac{1}{8}+\frac{m_{\mathrm{a}}}{3\pi}\cos(\varphi)\right)\right)$$
$$P_{\mathrm{Dcon}} = 4\left(\frac{1}{2}I_{\mathrm{m}}V_{\mathrm{D0}}\left(\frac{1}{\pi}-\frac{m_{\mathrm{a}}}{4}\cos(\varphi)\right)+I_{\mathrm{m}}^{2}r_{\mathrm{D}}\left(\frac{1}{8}-\frac{m_{\mathrm{a}}}{3\pi}\cos(\varphi)\right)\right), \quad (1)$$

Equations (1) are based on piece-wise linear approximation of the switch on-state characteristics, where V_{T0}, V_{D0}, r_T, r_D are parameters obtained from such characteristics given in Table 1, I_m is the amplitude of the output current fundamental component, φ is the phase angle between the fundamental component of the output voltage and the current. The switching losses, representing the losses occurring during the turn-on, turn-off and a diode reverse recovery process, are obtained similarly to this method. The switching energy characteristics are approximated by parabolic functions in a form of $P_{loss} = A_x I^2 + B_x I + C_x$, where A, B, and C coefficients are achieved by using the least squares approximation algorithm together with characteristics taken from device datasheets. These coefficients are collected in Table 1 and are used in (2) for calculating switching power losses.

$$P_{sw} = \frac{4V_{dc}}{V_{CE}} f_s \left((A_{on} + A_{off} + A_{rec}) \frac{I_m^2}{2} + \right.$$
$$\left. + (B_{on} + B_{off} + B_{rec}) \frac{I_m}{\pi} + \frac{1}{2}(C_{on} + C_{off} + C_{rec}) \right), \quad (2)$$

Power loss calculations with using equations (1) and (2) are done with the assumption that the output current is pure sinusoidal with no ripple component. In Table 1 parameters required for power loss calculation in Si-IGBT T-type converter and SiC-MOSFET two level converter are presented. As an example, in Fig. 3, on-state characteristics of three different transistor types are depicted.

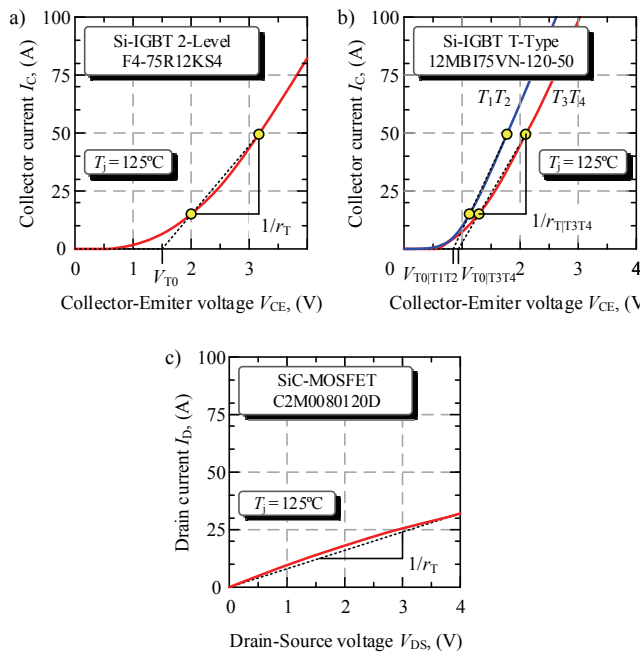

Fig. 3. On state characteristics of: a) IGBT – F4-75R12KS4, b) two IGBTs of T-type module 12MBI75VN-120-50, c) SiC MOSFET - C2M0080120D

It is clear from Fig. 3 that the highest voltage drop occurs across SiC-MOSFETs and the smallest are across IGBTs of T-type module. Fig 4 shows power losses divided into conduction and switching losses of three investigated converters arranged in a H-bridge converter supplying the RL load. The fundamental frequency of the generated output voltage is f_m = 50 Hz and the output power P_o = 5 kW, for this parameters the load resistance is set to R = 10 Ω and the inductance is L = 500 µH, giving the phase angle φ = 0.9 deg and impedance magnitude |Z| = 10 Ω. In this example the modulation index m_a = 0.85, and the output current amplitude is $I_{mn} = m_a V_{dc}/|Z| \approx 32$ A. Power losses in Fig. 4 are presented as functions of the switching frequency f_S, therefore the conduction losses are constant. In fact, due to the output ripple current, the converter conduction losses are varying with f_S.

Tab. 1. Parameters for power loss calculations (at T_j = 125ºC)

Parameter	F4-75R12KS4	12MBI75VN -120-50	C2M0080120D 2×C4D20120D
Transistor threshold voltage V_{T0}	1.50 V	T_1T_2: 0.86 V T_3T_4: 0.95 V	0 V
Transistor on-state resistance r_T	22 mΩ	T_1T_2: 17 mΩ; T_3T_4: 23 mΩ	120 mΩ
Diode threshold voltage V_{D0}	0.85 V	T_1T_2: 0.95 V; T_3T_4: 0 V	0.81 V
Diode on-state resistance r_D	10 mΩ	T_1T_2: 17 mΩ; T_3T_4: 0 mΩ	97 mΩ
Turn-on energy loss per pulse $E_{on}(i_T) = A_{Ton}i_T^2 + B_{Ton}i_T + C_{Ton}$ [A_{ton}, B_{Ton}, C_{Ton}]	[0.75, 50.4, 1.35] (µJ/A^2, µJ/A, mJ)	[0.24, 11.5, 0.13] [0.24, 11.6, 0.16] (µJ/A^2, µJ/A, mJ)	[0.42, -12.3, 6.70] (µJ/A^2, nJ/A, µJ)
Turn-off energy loss per pulse $E_{off}(i_T) = A_{Toff}i_T^2 + B_{Toff}i_T + C_{Toff}$ [A_{toff}, B_{Toff}, C_{Toff}]	[0.08, 39.3, 0.42] (µJ/A^2, µJ/A, mJ)	[-4.6, 35.9, 0.25] [141, 10.3, 0.18] (nJ/A^2, µJ/A, mJ)	[156, 1.36, 13.9] (nJ/A^2, µJ/A, µJ)
Diode reverse rec. energy loss per pulse $E_{rec}(i_T) = A_{Trec}i_T^2 + B_{Trec}i_T + C_{Trec}$ [A_{trec}, B_{Trec}, C_{Trec}]	[-0.32, 71.7, 1.21] (µJ/A^2, µJ/A, mJ)	[-0.70, 56.0, 0.03] [-0.80, 77.5, -0.01] (µJ/A^2, µJ/A, mJ)	0
Blocking voltage V_{CC}	600 V	300 V	600 V

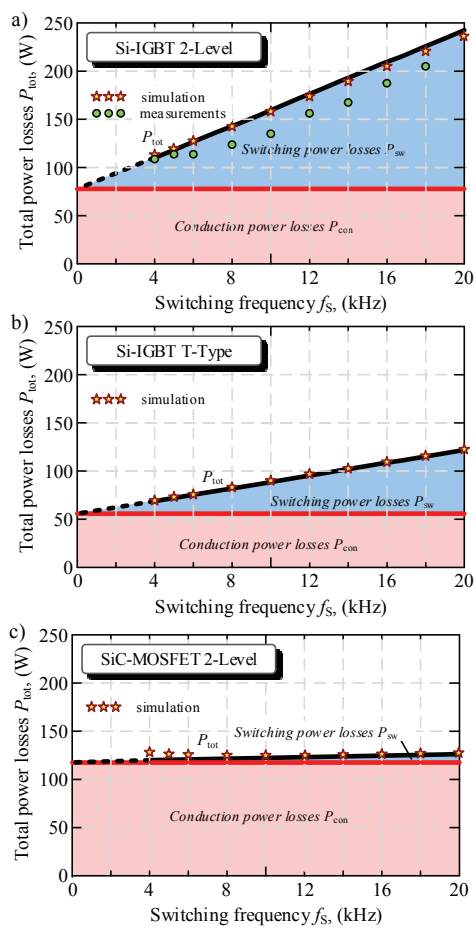

Fig. 4. Power losses P_{sw}, P_{con} as functions of switching frequency for three converter variants at the output power 5 kW: a) Si-IGBT two level b) Si-IGBT T-type, c) SiC MOSFET two-level

From Fig. 4 one can see that SiC MOSFET 2L converter has the highest conduction losses. It should be noted that the analyzed SiC-MOSFETs C2M0080120D are in much smaller package TO247 than analyzed IGBT modules. Such semiconductors are taken into consideration in this paper due to their availability and the comparable cost to other devices. The highest power losses

occur in Si-IGBT two level converter, e.g. for f_S = 10 kHz, P_{tot} = P_{con}+P_{sw} = 77.1 W+82.7 W = 159.8 W whilst for f_S = 20 kHz, P_{tot} = 242.5 W. Both conduction and switching losses in T-type converter are smaller than such losses in IGBT 2L converter, this losses are 72% and 40% of respective losses of two-level converter. In the third converter, SiC MOSFET 2L variant, the conduction power losses constitute 153% of conduction losses of Si-IGBT variant, but switching losses are only 5.3%. From Fig. 4 it is clear that SiC MOSFETs can be switched with very high frequency contributing to small increase of total losses.

The power loss analysis is verified by simulation models of H-bridge converters with three different converter legs, which are developed in GeckoCIRCUITS simulator. In Fig. 5.a the model of Si-IGBT H-bridge converter is presented as an example. The converter is feeding 5 kW of output power to the RL load, where L models the output filter inductor L = 500 μH and R = 10 Ω. The supply dc voltage is V_{dc} = 380 V. In all models it is possible to compute power losses of each switching device. The inductor current and voltage simulation waveforms are used in GeckoMAGNETICS software for the inductor geometry optimization. The exemplary waveforms are given in Fig. 5.b.

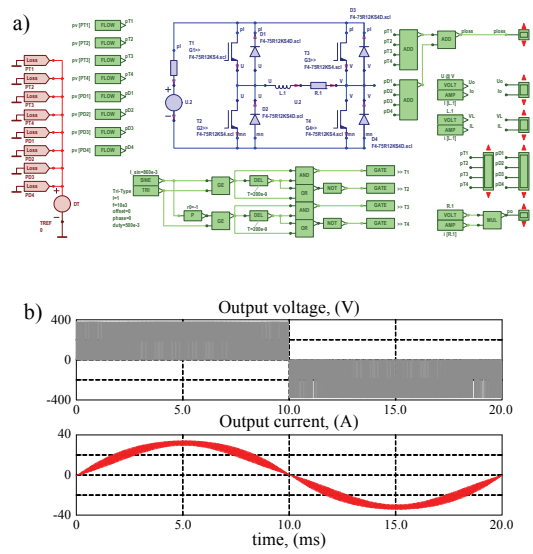

Fig. 5. Simulation model of Si-IGBT H-bridge converter developed in GeckoCIRCUITS simulator with output voltage and current waveforms at switching frequency f_S = 10 kHz

The power loss results can be used for comparing the cost of the converter utilization. The costs of all converters' components are comparable and estimated to be 200 € for Si-IGBT 2L, 230 € for Si-IGBT T-type and 250 € SiC-MOSFET 2L converter. This estimation is based on authors own experience during the construction of all converter prototypes. Higher cost of T-type compared to the cost of IGBT two-level converter is resulted from the higher number of driver circuits. The higher cost of SiC MOSFET converter is due to the higher cost of switching devices. Assuming that the converter operates during 20 years with a portion of the rated output power, power losses increase the total cost of the converter utilization. It is assumed that the cost of 1 kWh of energy loss is 0.12 €. In Fig. 6 the total cost of converter utilization is depicted as a sum of converter component cost and the cost of power losses generated during 20 years of an operation. These costs are given as a function of f_S.

As is seen from Fig. 6 the cost of utilization is the highest for the Si-IGBT 2L converter. The T-type converter has lower cost than the Si-IGBT 2L and it seems to be the best choice for switching frequencies between 4 and 20 kHz. For higher switching frequencies the lowest cost of utilization can be achieved by using SiC MOSFET 2L converter. These tendencies are observed for both operational condition with 10% and 50% of the rated power.

4. Converter prototypes

For evaluating the performance of three analyzed converter variants, two converter prototypes has been designed and built. The prototype of the Si-IGBT two-level H-bridge converter, which is based on Infineon IGBT module F4-75R12KS4, is shown in Fig. 7.a. The T-type converter prototype is designed as three-phase version due to the availability of a compact IGBT module 12 MBi75VN-120-50 (Fig. 7.b). The experimental prototype of SiC-MOSFET two level converter is arranged as two evaluation kits from Cree under the symbol KIT8020CRD8FF1217P-1 (Fig. 7.c). In this system C2M0080120D MOSFETs are with antiparallel SiC diodes C4D20120D. All converter prototypes are controlled by TMDSCNCD28335 control board, which allows operation with different switching frequencies f_S and modulation indices ma. Verification of power loss analysis is done for all converter prototypes by using measurements of input power (at dc power supply) and fundamental component of the output current. It is assumed that load resistance is constant. The test results are shown in Fig. 4.

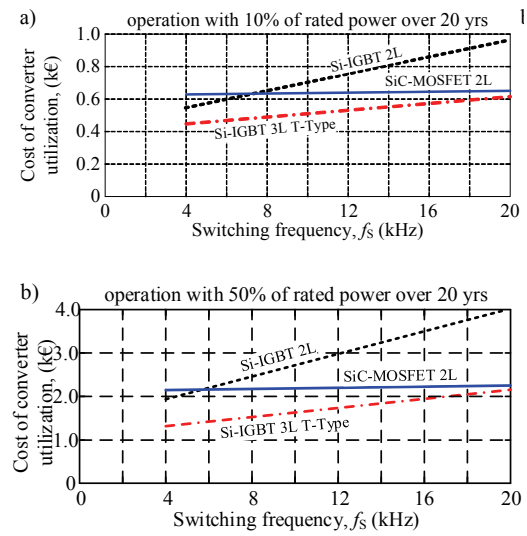

Fig. 6. Power losses P_{sw}, P_{con} as functions of switching frequency for three converter variants at the output power 5 kW: a) Si-IGBT two level b) Si-IGBT T-type, c) SiC MOSFET two-level

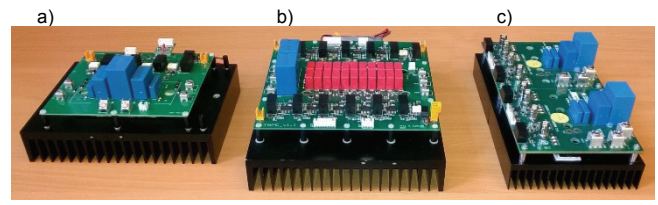

Fig. 7. Converter prototypes: a) Si-IGBT two level b) Si-IGBT T-type, c) SiC MOSFET two-level

5. Inductor design procedure

The major portion of power losses, which are generated in the power electronic converters, occur in semiconductor devices. Compare to this losses, power losses generated in inductors are typically smaller. This paragraph proposes the inductor design procedure, in which the main focus is put on the inductor size and cost. The presented design procedure is verified here by simulation models constructed in GeckoMAGNETICS software tool.

It is assumed that the designed inductor operates with the current which the rated amplitude is I_{mn} = 32 A (50 Hz). This value should not saturate the core of the inductor. To determine

the core material, three economical materials are investigated: a) ferrite 3C90, b) silicon electrical steel M165-35S and c) iron powder -26. In this example all inductors are supplied from the two-level H-bridge converter generating the sinusoidal output voltage waveform with fundamental frequency of 50 Hz, an amplitude of fundamental component 325 V ($m_a \times V_{dc} \approx 0.85 \times 380$ V) with the switching frequency f_S = 10 kHz. The required inductance of all inductors is L = 500 µH with the maximum current, above which core saturation occurs, set at the value I_{Lmax} = 35 A.

To compare core materials the same core geometry is assumed in each case. This geometry is based on the E cores of the size 65. Due to the temperature limitation or inductance constraint all three core materials have the same core thickness, which in case of laminated silicon steel is equal to the product of the number of steel sheets and their thickness 0.35 mm. The core thickness of ferrite and iron powder inductors is the product of the core thickness l = 27.4 mm and the number of stacked cores N_{stack} = 4.

The inductor core made from iron powder is gapless. Power losses obtained in GeckoMAGNETICS are presented for a comparison of core materials. The main conclusion from this analysis is that 3C90 ferrite, if compared with the other chosen materials, allows designing inductors with the smallest power losses. Power losses in inductors made from silicon steel sheets and iron powder cores are close to 50 W. Power losses in ferrite inductors are 4 times smaller. Moreover, it should be noted that the cost of the 3C90 ferrite cores is competitive to costs of other core materials. The following selection procedure given in this paragraph is based on the chosen 3C90 ferrite material.

The following parameters require to be determined, there are the inductor volume V_L, air gap length l_g, number of turns N, and relative cost. Here in this analysis the air gap length l_g is calculated as if the two E shaped cores form a single round core with single air gap which is $l'_g = 2l_g$. This is because the analyzed inductor core is composed of two E core halves with one major air gap in the central core leg and two minor air gaps in outer. The maximum volume of the selected inductor should not exceed 1 dm3 but it must be noted that the volume and the cost of the inductor are desirable to be minimized. The core sizes E65, E71, E80 and E100 are considered. For such core sizes the winding area Aw and core cross-sectional area Ac are given in Table 2.

The Ampere's Law expresses the relation between the core flux density B_c and inductor current I as

$$NI = B_c A_c N_{stack}\left(R_c + R_g\right), \tag{3}$$

where N_{stack} is the number of stacked cores, R_c and R_g represent the core and air-gap reluctances as (4),

$$R_c = \frac{l_c}{\mu_c \mu_0 A_c N_{stack}}, \qquad R_g = \frac{l'_g}{\mu_0\left(w_m l N_{stack} + \left(\frac{4}{\pi}\right) l N_{stack} l'_g \ln(1+2\pi)\right)}, \tag{4}$$

where l_c is the average core magnetic length, w_m and l are width and the depth of the core central leg, the core cross-sectional $A_c \approx w_m l$, μ_c is the core relative permeability, which for the 3C90 is μ_c = 2300. In the denominator of R_g the increase of the equivalent air-gap cross-sectional area due to the flux fringing effect is modeled as in reference [9].

By substituting (4) into (3) it is possible to find the number of turns N as a function of the air-gap, thus

$$N(l'_g) = \frac{B_{max}}{I_{max}} \frac{A_c}{\mu_0}\left(\frac{l_c}{\mu_c A_c} + \frac{l'_g}{A_c + \left(\frac{4}{\pi}\right) l l'_g \ln(1+2\pi)}\right) < N_{max} \tag{5}$$

$$N_{max} = k_{Cu}\left(\frac{A_w}{I_{max}}\right) J_{max} \tag{6}$$

The number of turns $N(l'_g)$, in the winding area A_w, are given as a function of the air gap in Fig. 9 for different core sizes. This number should not exceed the maximum number of turns N_{max}, which is determined with the assumption that the minimum fill factor is k_{Cu} = 0.3 and the maximum current density J_{max} = 6 A/mm2 according to (6). For each core size N_{max} is given in Table 2. From (5) it is known that the number of turns $N(l'_g)$ is independent on the number of stacked cores. For example, the maximum air gap length in E65 core is l'_g = 5.4 mm, for which the number of turns N(5.4 mm) = N_{max} = 27. By applying (5), the inductor guarantees the maximum flux density B_{max} at maximum current I_{max}, but for achieving the required inductance value L it is needed to determine the number of stacked cores N_{stack} according to (7). In Table 2 the boxed core and winding volume with core mass are given.

Tab. 2. Ferrite core parameters (for two E core halves)

Core size	A_w, (mm^2)	A_c, (mm^2)	l_c, (mm)	w_m, (mm)	l, (mm)
E65	537	568	147	20.0	27.4
E71	569	717	149	22.0	32.0
E80	1108	399	184	19.8	19.8
E100	2139	756	274	27.5	27.5
Core size	**w, (mm)**	**$V_{corebox}$, (cm^3)**	**$V_{windbox}$, (cm^3)**	**mass, (g)**	**N_{max}**
E65	65	116.8	47.5	410	27
E71	70.5	149.8	54.7	520	29
E80	80	120.7	131.0	360	56
E100	100.3	327.7	312.9	986	110

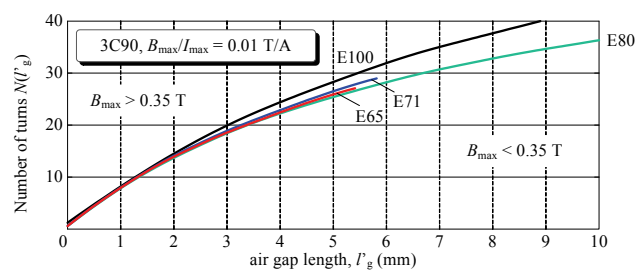

Fig. 8. Number of turns N as a function of the air gap length l'_g for cores E65, E71, E80 and E100

$$L(N, N_{stack}) = \frac{\left(N(l'_g)\right)^2}{R_c + R_g} = \frac{\left(N(l'_g)\right)^2 \mu_0 A_c}{\frac{l_c}{\mu_c} + \frac{l_g}{\left(1 + \frac{4 l l'_g \ln(1+2\pi)}{\pi A_c}\right)}} N_{stack}, \tag{7}$$

In Fig. 9 the possible inductor solutions are presented as the regions on the number of turns – air gap plane for different number of stacked cores and core sizes. The constant inductance curves are taken from (7). In all regions presented in Fig. 10, 14 possible solutions have been indicated. Their details are presented in Table 3.

Table 3. gathers the parameters of 14 possible inductors (as in Fig. 10) with the number of turns calculated from (5), the selected air gap l'_g, and number of stacked cores N_{stack} from (7) for the reference inductance L = 500 µH. The number of presented solutions is limited by the total volume of 1 dm3 and the maximum number of turns N_{max} as in (6). It should be noted that each of these inductor variants has the maximum field density B_{max} = 0.35 T at maximum current I_{max} = 35 A.

The resulted values of the inductances L are close to the reference value 500 µH, because in each case the air gap l'_g has the tolerance of 0.1 mm and N is an integer number. Calculated and computed results from GeckoMAGNETICS simulator, referred here as L_{GECKO}, are in good agreement.

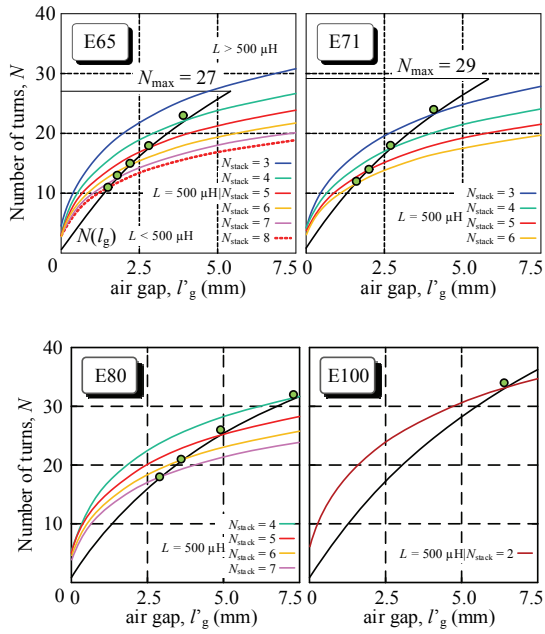

Fig. 9. Number of turns N as a function of the air gap length l'_g for cores E65, E71, E80 and E100

Tab. 3. Parameters of selected inductors made from 3C90 E shaped cores

Core size	N_{stack}	N	l'_g, (mm)	L, (µH)	L_{GECKO}, (µH)	Litz wire Nr. of strands × strand diameter/ total diameter	Winding length (m)
E65	4	23	3.9	544.9	530.6	200×0.2/3.94 mm	8.18
	5	18	2.8	523.8	519.7	250×0.2/4.22 mm	6.95
	6	15	2.2	521.4	522.4	300×0.2/4.52 mm	6.65
	7	13	1.8	533.1	537.5	360×0.2/5.30 mm	6.68
	8	11	1.5	504.0	510.3	360×0.2/5.30 mm	6.27
E71	3	24	4.1	531.6	523.6	200×0.2/3.94 mm	7.93
	4	18	2.7	533.5	536.6	250×0.2/4.22 mm	6.68
	5	14	2.0	505.6	514.4	300×0.2/4.52 mm	6.13
	6	12	1.6	530.8	543.7	360×0.2/5.30 mm	6.21
E80	4	32	7.3	520.9	493.1	300×0.2/4.52 mm	9.24
	5	26	4.9	535.4	524.1	360×0.2/5.30 mm	8.97
	6	21	3.6	508.8	508.6	360×0.2/5.30 mm	8.08
	7	18	2.9	505.1	510.7	360×0.2/5.30 mm	7.16
E100	2	34	6.4	528.2	559.0	600×0.2/7.10 mm	9.98

Keeping the maximum fill factor k_{Cu} is one of the inductor design objective. This maximization is achieved by using different litz wires, as in Table 3. For such inductors with defined cores and winding it is possible to compute in GeckoMAGNETICS both core and winding power losses referred as ΔP_{core} and ΔP_{Cu}. Inductor power losses and the total volume of the inductor V_{ind} are presented in Table 4 and Fig. 10.a. The inductor volume V_{ind} is equal to the sum of the core boxed volume $N_{stack}V_{corebox}$, the winding volume $V_{windbox}$, which protrudes the core boxed volume and the volume increased by the air gap. This sum is expressed as (8).

$$V_{ind} = N_{stack}V_{corebox} + V_{windbox} + \frac{wlN_{stack}l'_g}{2}, \qquad (8)$$

Inductor power losses are summed and illustrated in Fig. 10.a as the loss-volume diagram. It is evident from this figure that power losses are higher for inductors having a smaller volume. For all core sizes the volume strongly depends on the number of stacked cores N_{stack}. Knowing the winding mass, which is mainly the mass of the copper, and the mass of cores, which are given in Table 4, it is possible to calculate the total cost of the designed inductor. These costs are shown for each inductor in Fig. 10.b as a relative cost to the cost of the first inductor made from 4 stacked E65 cores. In this analysis it is assumed that the cost of 1 kg of litz wire is 2.6 times the cost of 1 kg of 3C90 ferrite.

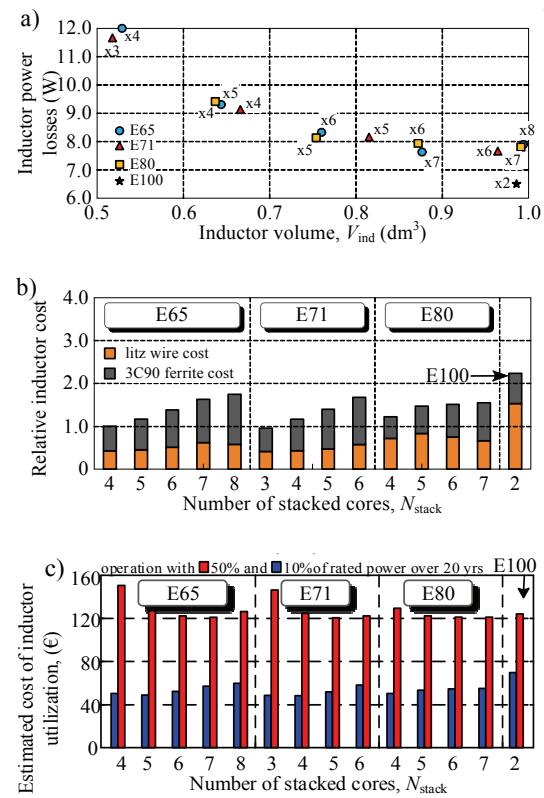

Fig. 10. Number of turns N as a function of the air gap length l'_g for cores E65, E71, E80 and E100

Tab. 4. Parameters of selected inductors

Core size	E65					E100
N_{stack}	4	5	6	7	8	2
V_{ind}, (cm^3)	529	644	760	876	993	986
ΔP_{core}, (W)	1.06	1.88	2.39	2.68	3.22	2.06
ΔP_{Cu}, (W)	10.95	7.43	5.93	4.96	4.66	4.45
Wind. mass, (kg)	0.46	0.49	0.56	0.67	0.63	1.68
Core mass, (kg)	1.64	2.05	2.46	2.87	3.28	1.97

Core size	E71				E80			
N_{stack}	3	4	5	6	4	5	6	7
V_{ind}, (cm^3)	518	666	815	964	637	754	872	992
ΔP_{core}, (W)	1.04	1.95	2.67	3.04	1.18	1.47	1.93	2.50
ΔP_{Cu}, (W)	10.61	7.15	5.47	4.61	8.24	6.67	6.01	5.32
Wind. mass, (kg)	0.44	0.47	0.52	0.63	0.78	0.91	0.82	0.72
Core mass, (kg)	1.56	2.08	2.60	3.12	1.44	1.80	2.16	2.52

The inductor with 4 E65 cores has been build and tested with H-bridge 2L converter. The measurements showed 12 W of inductor losses, which is in good agreement with computed losses from Table 4. The inductor relative cost is not critical when the total cost of utilization is taken into account. For presentation of such cost it is assumed that the inductor operates during the period of 20 years with 10% and 50% of maximum power losses, as given in Table 4. The estimation of utilization costs (Fig. 10.c) is done with assuming that the cost of 4xE65 inductor is 25 € and the cost of 1 kWh of energy is 0.12 €. When the designed inductor

operates with relatively small power, here 10% of maximum power over 20 years, the estimated cost of utilization of larger variants are higher than the cost of smaller variants. This is no longer necessarily true when the power utilization increases e.g. to 50% of the maximum power. In such a case, inductors having lower power losses are more expensive, but they are more competitive to less expensive counterparts. This is particularly interesting conclusion for power electronic converters used in microgrids where power utilization over the long period of time is relatively high.

As is seen from the analysis presented in this paragraph power losses generated in inductors are low. It is mainly due to the utilization of efficient and not expensive material 3C90. The analysis presented in this paragraph was carried out in case of the operation of two-level H-bridge converter with switching frequency of 10 kHz. In case of using three level converter topology e.g. by using T-type converter, it is possible to reduce the inductance of the inductor by 50%. In case of using two-level converter with SiC-MOSFETs with higher switching frequency it is possible to reduce the inductance further.

6. Conclusions

Three topologies of converter legs have been analyzed in terms of utilizing them in the power electronic system for residential buildings. This utilization requires a detailed recognition of the costs due to power losses and cost of converter components. The paper presents power losses analysis of all three converter leg variants together with the detailed inductor selection procedure. Relatively small power losses are generated in T-type coverter which operation is justified with the switching frequency up to 20 kHz. SiC MOSFET based converters offer power losses almost not dependent on the switching frequency, which allows reducing the inductor size and its cost without increasing the cost of power losses. Si-IGBT 2L converter utilizes switching devices which are commonly used in many applications and therefore are less expensive than other devices. Due to small losses generated in inductors with ferrite cores, these materials seem to be the most preferable choices for output inductors of converters operating with low frequency AC currents with high frequency ripple.

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7. References

[1] Boroyevich D., Cvetkovic I., Burgos R., Dong D.: Intergrid: A future electronic energy network?, IEEE J. Emerging Sel. Topics Power Electron., Vol. 1, no 3, pp. 127-138, Sep. 2013

[2] Kouro S., Leon J. I., Vinnikov D., Franquelo L. G.: Grid-Connected Photovoltaic Systems: An Overview of Recent Research and Emerging PV Converter Technology, IEEE Industrial Electronics Magazine, Vol. 9, no 1, pp. 47-61, 2015

[3] Dong D., Cvetkovic I., Boroyevich D., Zhang W., Wang R., Mattavelli P.: Grid-interface bidirectional converter for residential DC distribution systems - Part 1: High-density two-stage topology, IEEE Trans. Power Electron., Vol. 28, no 4, pp. 1655-1666, Apr. 2013

[4] Patterson B.: DC, come home: DC microgrids and the birth of the "Ener-net" IEEE Power Energy Magazine, vol. 10, no 6, pp. 60-69, Nov. 2012.

[5] Bierhoff M. H., Fuchs F. W.: Semiconductor losses in voltage source and current source IGBT converters based on analytical derivation. IEEE 35th Annual Power Electronics Specialists Conference PESC, 2004.

[6] Schweizer M. Kolar J. W.: Design and implementation of a highly efficient three-level T-type converter for low-voltage applications, IEEE Trans. Power Electron., Vol. 28, no. 2, pp. 899-907, Feb. 2013

[7] Zhe Zhang, Anthon A., Andersen M.A.E.: Comprehensive Loss Evaluation of Neutral-Point-Clamped (NPC) and T-Type Three-Level Inverters based on a Circuit Level Decoupling Modulation. Power Electronics and Application Conference PEAC, 2014.

[8] Staudt I.: Comprehensive 3L NPC & TNPC Topology. Semikron Application Note AN-11001, 2015.

[9] Hanselman D.: Brushless Permanent-Magnet Motor Design. McGraw-Hill, New York, 1994.

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