INTL JOURNAL OF ELECTRONICS AND TELECOMMUNICATIONS, 2021, VOL. 67, NO. 4, PP. 699-704
Manuscript received July 9, 2021; revised November, 2021 DOI:10.24425/ijet.2021.137865

Logarithmic ADC with Accumulation of Charge and Impulse Feedback – Construction, Principle of Operation and Dynamic Properties

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***Abstract*—This article is a presentation of the analysis of new class of logarithmic analog-to-digital converter (LADC) with accumulation of charge and impulse feedback. LADC construction, principle of operation and dynamic properties were presented. They can also be part of more complex converters and systems based on LADC. LADC of this class is perspective for implementation in the form of integrated circuit, as the number of switched capacitors needed to conversion is minimized to one capacitor. (Logarithmic ADC with accumulation of charge and impulse feedback – construction, principle of operation and dynamic properties)**

***Keywords*—Analog-to-digital converter, analysis, construction, charge accumulation, logarithm, modeling, impulse feedback**

I. Introduction

ANALOG-to-digital converters (ADC) are the most important link in the modern digital systems used in the various areas of human activity, because they link these systems with real objects whose information from sensors is almost always (more than 90 %) given in analog form. The accuracy and speed of these systems depend in the first place on the characteristics and parameters used in ADC. From many ADC special attention is paid to ADC with logarithmic characteristic of conversion [1-20].

Logarithmic converters are indispensable for systems working in a wide range of input signals of 80 dB or more.

Use of logarithmic conversion provides for an effective solution to a number of important tasks, such as: compression of dynamic range of input signals, ensuring constant relative error of conversion, linearization of conversion characteristics and carrying out logarithmic arithmetic operation, in which multiplication, division or raising to a power is reduced to the basic operations of addition, subtraction, multiplication and division by constant factors. The last of these advantages is probably the most important, because it causes a significant increase in the speed of computerized systems, which is the most important for control systems of real-time such as control systems of manufacturing process and robot motion, telecommunications, aero navigations, cosmic and others in which delay in processing must be minimized.

A. Objective and scope of work

The aim of this article is principles of construction, the analysis of dynamic properties.

II. Physical Model of LADC with Accumulation of Charge and Impulse Feedback

In fig. 1 functional block diagram of LADC with accumulation of charge and impulse feedback has been presented. Authors improved described converter by adding switch (SW2). This eliminates the influence of no-load running on the output of voltage-current converter and increase of accuracy and decrease of time needed for transitional processes. LADC (fig.1) contains: CLK - clock, AND - and gate, CNT - counter, RM - register of memory, N - output code, Cmp - comparator, MM – monostable multivibrator, IN1 and IN2 - logic inverter 1 and 2, ED – element of delay, SBEF – scaling block of exponential function, RVS - reference voltage source, SW0 to SW2 - analog switches, C – accumulative capacitor, VF – voltage follower, VCT - voltage-current transducer, IN - input.

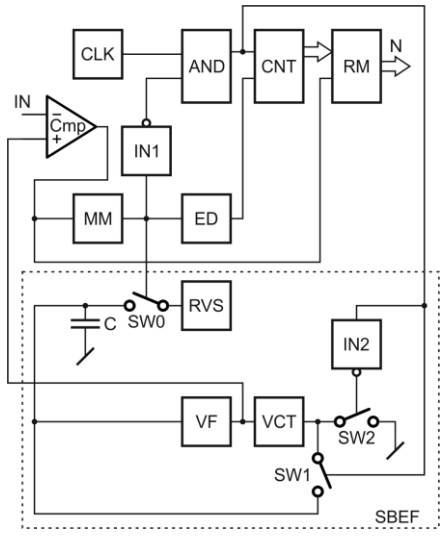

Fig. 1. Functional block diagram of LADC with accumulation of charge and impulse feedback

This article was developed as part of the international cooperation concluded between the University of Technology in Kielce and the University of Technology in Lviv.

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After switching power supply on, comparator Cmp turns on and activates monostable multivibrator MM. Output impulse of MM turns on switch SW0 trough which capacitor C charges to a reference voltage U_0. Simultaneously impulse of MM inverts itself by inverter N1 and prohibits impulses of the clock CLK on the input of the counter CNT. Delayed MM impulse by ED resets counter L.

After finishing of MM impulse switch SW0 turns off and on output of the inverter N1 appears logic one, which allows for course of clock impulses on the counter L and control input of switch SW1. With each clock impulse, switch SW1 turns on and connects output of the VCT to the accumulative capacitor C. The capacitor C discharges by output VCT current during the clock impulse. During pause between clock impulses, switch SW1 is turned off and capacitor C keeps its charge. In this way, with each clock impulse, which course trough AND gate, voltage on capacitor C reduces itself.

Let us note that during the pause between clock impulses, when the switch SW1 is turned off and switch SW2 turned on, output of VCT is connected to the ground, what is the ideal working mode of VCT.

Voltage from the capacitor C transfers itself on comparator Cmp through VF with transfer coefficient equal to one. When the voltage on capacitor C becomes equal to input voltage, Cmp starts. Output impulse of Cmp saves the result of the count impulses on the output of AND gate from counter CNT to register of memory RM and starts MM, then this process is repeated.

Let us note that in RM data is stored until the appearance of the next output impulse of comparator Cmp.

Let us define the characteristic of LADC conversion. In order to do this, we examine change in voltage on the accumulative capacitor C.

Impulse from the output of MM causes an initial installation of LADC and the process of conversion begins from the moment of the end of MM impulse. At this moment, the voltage on accumulative capacitor C is equal to reference voltage U_0, which is on the output of reference voltage source RVS, and AND gate receives permission for course of clock impulses CLK on counter CNT.

With the first impulse on output of AND gate switch SW1 turns on and output current of VCT flows through SW1 on capacitor C and discharges it. As a result of great value of output resistance of VCT, which has the same value as output resistance of current source, voltage on capacitor C changes linearly causing linear change of output current of VCT.

Using average value of VCT output current, we define voltage on capacitor C after first impulse on output of AND gate as

$$U_1 = U_o - \frac{Yt}{2C}\left(U_1 + U_o\right)$$

that is

$$U_1 = \xi U_o \tag{1}$$

$$\xi = \frac{1 - Yt/2C}{1 + Yt/2C} \tag{2}$$

where: Y – conversion factor of VCT, t – lasting time of clock impulse CLK, C – capacitance of an accumulative capacitor.

Change of voltage on capacitor C at the time of the duration of the first impulse on the output of AND gate

$$\Delta U_1 = U_o - U_1 = U_o\left(1 - \xi\right) \tag{3}$$

At the time of the duration of the second clock impulse on the output of AND gate switch SW1 again turns on, voltage on capacitor C reduces and becomes equal to

$$U_2 = U_1 - \frac{Yt}{2C}\left(U_2 + U_1\right)$$

that is

$$U_2 = \xi^2 U_0$$

Change of voltage on capacitor C at the time of the duration of the second impulse on the output of AND gate

$$\Delta U_2 = U_1 - U_2 = \xi\left(1 - \xi\right)U_o$$

Analogically voltage changes on capacitor C at the time of the duration of each next impulse on the output of AND gate and after passing N impulses it becomes equal to

$$U_N = \xi^N U_o \tag{4}$$

And its change

$$\Delta U_N = \xi^{N-1}\left(1 - \xi\right)U_o \tag{5}$$

When the voltage on capacitor C after passing N-th impulse it becomes equal to input voltage U_{in}, i.e.

$$U_{in} = \xi^N U_o$$

then number of impulses stored in counter L becomes equal to

$$N = \frac{1}{\ln \xi} \ln \frac{Uin}{Uo} \tag{6}$$

This means, that the result of LADC conversion equals the number of clock impulses CLK, which are entered in the counter L in the time from the moment of disappearing of impulse of monostable multivibrator MM to running comparator Cmp. Let us notice that coefficient ξ in the formula (6) is a database of logarithm.

Let us examine accuracy of LADC.

Relative error of quantization on any step of conversion has value

$$\delta = \frac{\Delta U_i}{U_i} = \frac{1 - \xi}{\xi} \tag{7}$$

If a base of logarithm $\xi = const$, then $\delta = const$.

The relative error of quantization δ does not depend on the size of input value, but only from a base of logarithm.

From the formula (2) we can see that the logarithm base is dependent on conversion coefficient of VCT, time of duration of clock impulses CLK and capacitance of accumulative capacitor C. Relative error of logarithm base may be defined by the formula (2) as double sum of relative errors of multiplied coefficients because products in numerator and denominator are equal to absolute value and have different signs

$$\delta_\xi = 2\left(\delta_Y + \delta_t + \delta_C\right) \tag{8}$$

So, in order to improve the accuracy of LADC essential is stabilization of component parameters, which define logarithm base.

The easiest way is to stabilize duration of clock impulses. In the case of using as a clock source the simplest quartz oscillator relative error of time duration of clock impulses does not exceed 0.001 - 0.0001 %.

As an accumulative capacitor, it is suitable to use precise capacitors made of styroflex, polystyrene or mica. Temperature coefficient of better ones does not exceed 0.003%/degree of Celsius. Due to this, the relative rror of capacitance is lower than 0.006% in room temperatures.

Special attention in the structure of LADC should be paid to realization of voltage – current transducer VCT.

Simple circuits based on PNP transistors have low accuracy.

The highest accuracy and easy realization have compensation VCT based on operational amplifiers OA and field-effect transistors FET [13]. Among them, the most promising is compensation VCT (fig. 2).

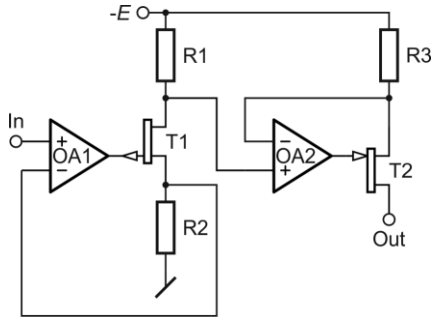

Figure 2. Schematic diagram of compensation voltage-current transducer realized with OAs and FETs

Coefficient of conversion of this VCT

$$Y = \frac{R_1}{R_2 R_3} \tag{9}$$

where R_1, R_2, R_3 are resistances of resistors by which output current of VCT is set. Target is to select $R_1 = R_2$.

Input Impedance of VCT is equal to nodifferential impedance of OA

$$R_{in} = r_n$$

i.e. it exceeds 100 $M\Omega$.

Output impedance of VCT

$$R_{out} = KSr_{ds}R_3 \tag{10}$$

where K - own coefficient of voltage gain of OA (without feedback from output to input); r_{ds} and S - drain-source resistance and transconductance of FET on the oputput of VCT.

For large output resistance values it is necessary to consider shunting effect of output resistance according to formula (10) with gate-source resistance (r_{bs}) of FET on VCT output. Practically, taking into account parameters of modern OAs and FETs, output impedance of VCT equals:

$$R_{out} = r_{gd}$$

where r_{gd} - gate-drain resistance of FET, which usually exceeds 100 $M\Omega$.

Output current of VCT linearly depends on input voltage, and does not depend on parameters of OAs and FETs

$$I_{out} = YU_{in}$$

or

$$I_{out} = \frac{R_1}{R_2 R_3} U_{in} \tag{11}$$

We define relative error of VCT on the basis of above formula as a

$$\delta_{VCT} = \delta_{R_1} + \delta_{R_2} + \delta_{R_3} \tag{12}$$

where $\delta_{R_1}, \delta_{R_2}, \delta_{R_3}$ - relative errors of resistors R_1, R_2, R_3

If resistors R_1, R_2, R_3 are of one type (with equal instability factors), then there will be a compensation of their errors and relative error of conversion of VCT becomes equal to error of one resistor for example resistor R_3:

$$\delta_{VCT} = \delta_{R_3}$$

For precise resistors, temperature coefficient does not exceed 0.001% per degree of Celsius and relative error of VCT does not exceed 0.002% at room temperatures.

Let us note that for the correct working of VCT voltage value on the output of VCT (U_{out}) should not exceed the value:

$$U_{out} = E - U_{in} - U_{ds} \tag{13}$$

where E – voltage supply of VCT; U_{ds} - voltage drain-source of saturated FET ($U_{ds} \geq 1V$).

Therefore relative error of base of logarithm will not exceed 0.02% and on the same value will change relative error of LADC quantization. Effects of this error can be compensated relatively easily alike for additive errors in linear ADC.

III. Assessment of Dynamic Properties of LADC with Accumulation of Charge and Impulse Feedback

In physical modeling of LADC with accumulation of charge and impulse feedback we should be aware that their dynamic properties are practically completely defined by the charge and discharge time of accumulative capacitor C.

Charging circuit of accumulative capacitor C can be represented as a first-order aperiodic term (fig. 3), and therefore voltage changes on it in time according to a formula

$$U_C(t) = U_0(1 - e^{-\frac{t_t}{\tau_l}})$$

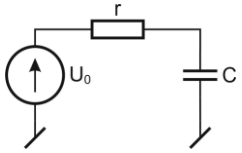

Figure 3. Circuit diagram of charging accumulative capacitor

Time-constant of charging accumulative capacitor C is defined as

$$\tau_l = rC$$

where r - resistance of turned on switch.

For capacitance of the accumulative capacitor C 1μF and resistance of turned on switch 70Ω charging time-constant of accumulative capacitor $\tau_l = 70\mu s$. For reduction of error from undercharging (δ_n) on the level not higher than 0.005% charging time should be set no lower than $12\tau_l$, that is 840 μs.

To reduce charging time of accumulative capacitor target is to use improved switches [13], whose resistance in the turned on state does not exceed 0.01 Ω. Then for the above mentioned conditions $\tau_l \le 10ns$ and for reduction of $\delta_n \le 0{,}005\%$ charging time of accumulative capacitor should not be less than 120 ns.

An accumulative capacitor discharges by feedback impulses from the output of VCT which can be shown on schematic diagram as a current source with internal conductance G (fig.4). Since output current of VCT converts itself in voltage on the accumulative capacitor, it is necessary to determine impedance of transformation (Z_t) from node 1 to node 2 and in this case load is accumulative capacitor C.

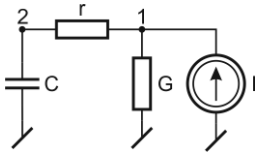

Figure 4. Circuit diagram of discharging accumulative capacitor.

Voltage on accumulative capacitor C is defined as

$$U_C = Z_t I$$

where Z_t - transformation impedance according to [20] is

$$Z_t = \frac{\Delta_{12}}{\Delta + Y_L \Delta_{22}}$$

where $\Delta_{12}; \Delta_{22}$ and Δ - algebraic complements and admittance matrix determinant [Y] of discharge circuit of accumulative capacitor C (fig. 4).

Matrix admittance [Y] of the circuit has form

where y – conductance of turned on switch; $y=1/r$.

Algebraic complement and admittance matrix determinant [Y] are respectively equal to

$$\Delta_{12} = y \;;\quad \Delta_{22} = y + G \;;\quad \Delta = yG$$

Taking into account above formula we define transformation impedance as

$$Z_t = \frac{R}{1 + sC(r+R)}$$

where $R = \frac{1}{G}$

Thus, voltage on the accumulative capacitor in operational form equals

$$U_{C_a} = \frac{R}{1 + sC(r+R)} I$$

Above formula can be written in a more convenient form

$$\big(C(r+R)s + 1\big)U_C = RI$$

what indicates that this is heterogeneous differential equation in operational form.

As readers knows, the solution of heterogeneous differential equation is a sum of partial solution of heterogeneous differential equation $\left(U_C^{'}\right)$ and general solution of heterogeneous differential equation $\left(U_C^{''}\right)$, i.e. voltage on accumulative capacitor

$$U_C = U_C^{'} + U_C^{''}$$

In our case,

$$U_C^{'} = RI \quad \text{and} \quad U_C^{''} = Ae^{\alpha t} \;.$$

To define a general solution of homogeneous differential equation

$$C(r+R)s + 1 = 0$$

let us find root of equation

$$\alpha = -\frac{1}{C(r+R)} \,.$$

Constant A will be equal to

$$A = -RI$$

and general solution of a homogeneous differential equation is

$$U_C^{''} = -RIe^{-\frac{t}{C(r+R)}}$$

Thus, the voltage on accumulative capacitor is equal to

$$U_C(t) = (1 - e^{-\frac{t}{C(r+R)}})RI.$$

Above formula can be written in Maclaurin series

$$U_C(t) = RI\left(\frac{t}{RC} - \frac{1}{2}\cdot\frac{t^2}{R^2C^2} + \ldots + \ldots + \frac{(-1)^{n-1}}{n!}\cdot\frac{t^n}{R^nC^n}\right)$$

Here one should take into consideration that internal resistance R of current generator (it is output resistance of VCT) is equal to gate-drain resistance (r_{bd}) of FET on VCT output and since $r_{gd} \ge 10^8 \div 10^9 \Omega$, i.e. $R >> r = 70\Omega$, time constant of accumulative capacitor discharge current

$$\tau_r = (r+R)C \approx RC$$

[Y] =

	1	2
1	$y+G$	$-y$
2	$-y$	y

The above series of variable mark – is fast convergent because $RC >> 1$.

Absolute error of sum of terms of variable sign of convergent series does not exceed value of first rejected term of this series. As a result voltage on accumulative capacitor is equal

$$U_C(t) = I\frac{t}{C} \qquad (14)$$

with absolute error

$$|\Delta_n| \le \frac{1}{2}\cdot\frac{t^2}{R^2C^2}\cdot RI$$

or with relative error

$$\delta_n \le \frac{\Delta_n}{U_C(t)}, \quad \text{i.e.}$$

$$0 \ge \delta_n \ge -\frac{1}{2}\cdot\frac{t}{RC}\cdot 100\% \qquad (15)$$

In the last formula, it can be seen that absolute value of relative error δ_n increases with increase of discharge time t. For the set value of error δ_n one can determine acceptable value of discharging time

$$t \le \frac{2RC\delta_n}{100\%}$$

Accumulation of error with each step of conversion must be taken into consideration. Then the last formula takes form

$$t \le \frac{2RC\delta_n}{100\% \cdot N} \quad (16)$$

where N - number of conversion steps.

Let us point here that for quantization error 0.1% in whole range of input signals one needs to set N=10000.

Establishing δ_n = 0.01% for N = 10000 and taking into account $R = 10^9 \Omega$ and $C = 1\mu F$, we get maximally allowed time of one step of conversion $t \le 20\mu s$, and for $R = 10^8 \Omega$ and remaining above data $t \le 2\mu s$.

IV. Modeling Impact of Leakage Currents in LADC with Charge Accumulations and Impulse Feedback.

We have carried out analysis of leakage currents for the above diagram of LADC taking two phases of the converter:

first phase - discharging of accumulative capacitor C (switches SW0, SW2 are opened and switch SW1 is closed).

second phase - pause (switches SW0, SW1 are opened and switch SW2 is closed).

In order to carry out mathematical analysis of LADC, taking into account leakage currents, equivalent circuit diagrams (fig.5, fig.6) for the particular phase taking into account only these elements which have impact on leakage currents were made.

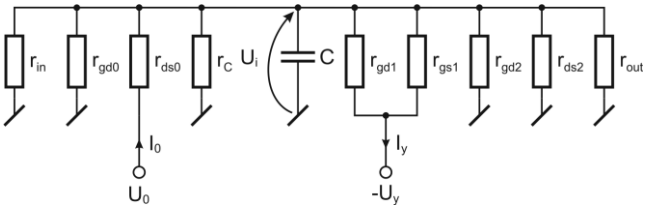

Figure 5. Equivalent circuit diagram of LADC for the first phase (Φ1)

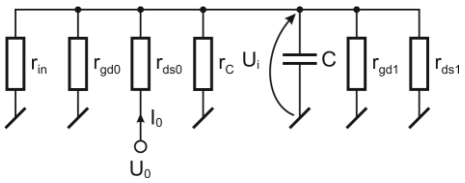

Figure 6. Equivalent circuit diagram of LADC for the second phase (Φ2)

Mathematical analysis of LADC was carried out for the following parameters:

r_c = 100 TΩ, r_{gd} = 1 GΩ , r_{gs}= 1GΩ , r_{ds} = 1GΩ, r_{SW1} = 0.1 G Ω , r_{SW2} = 0.1 GΩ , r_{vf} = 0.1 G Ω , U_0 = 10 V, U_y = 15 V

Analysis of leakage currents for first phase (Φ1)

Absolute error of voltage on accumulative capacitor from leakage currents can be determined from the formula:

$$\Delta U_{Ni} = \frac{1}{C}\sum_{\kappa=1}^{\kappa=2} I_{\Phi\kappa} \cdot t_{\Phi\kappa} \cdot N \quad (17)$$

where: N - number of tacts of the converter, $t_{\Phi1}$, $t_{\Phi2}$ and $I_{\Phi1}$, $I_{\Phi2}$ - respectively times and leakage currents for the particular work phases of the converter.

Total leakage current for the first phase we determine on the basis of formula:

$$I_{\Phi1} = I_0 - I_1 - I_y$$

where: I_0 - leakage current from the reference voltage source U_0 expressed as:

$$I_0 = \frac{U_0 - U_i}{r_{ds}}$$

I_1 - leakage current from capacitor C_n expressed as:

$$I_1 = \left(\frac{2}{r_{gd}} + \frac{1}{r_{ds}} + \frac{1}{r_{gs}} + \frac{1}{r_{in}}\right)$$

I_y - leakage current from control voltage which controls analog switch, expressed as:

$$I_y = (U_i + U_y) \cdot \left(\frac{1}{r_{gs}} + \frac{1}{r_{gd}}\right)$$

Analysis of leakage currents for second phase (Φ2)

Total leakage current for the second phase we determine on the basis of formula:

$$I_{\Phi2} = I_0 - I_2$$

where: I_2 - leakage current from capacitor C_n expressed as:

$$I_2 = U_i \cdot \left(\frac{1}{r_{gd}} + \frac{1}{r_{ds}} + \frac{1}{r_{gs}} + \frac{1}{r_{in}}\right)$$

in which: U_i - voltage on accumulative capacitor in i-th phase of conversion.

In the case of the analyzed converter N =10000, while times for individual phases are: $t_{\Phi1}$ = 2 μs and $t_{\Phi2}$ = 0.5 μs.

In fig.7 absolute error on LADC accumulative capacitor was presented.

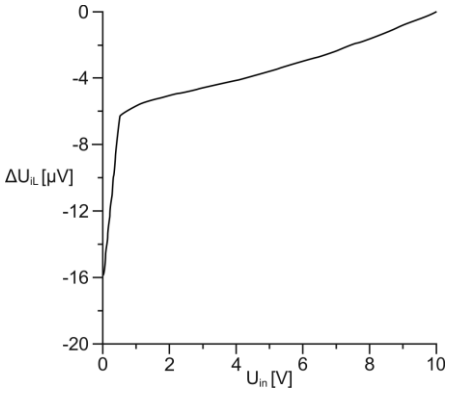

Figure 7. Absolute error of voltage on LADC accumulative capacitor from the impact of leakage currents

V. Conclusions

On the basis of conducted research of LADC with charge accumulation and impulse feedback, it can be concluded that:

1. When designing above LADC, main attention should be paid to VCT because accuracy of the other functional nodes is much easier obtainable.
2. The highest accuracy of above LADC is obtained when

VCT is realized as compensation system on OAs and FETs. On the output of such VCT, should be put FET with increased value of gate-drain resistance, intentionally above $10^9\,\Omega$.

3. For quantization error of 0.1% over the entire range of input signals, time of conversion of above LADC should be set intentionally from 10 to 20 ms. Together with an increase of quantization error, time of conversion may be reduced.
4. Error from the impact of leakage currents increase with increase of time of conversion and is much smaller than error from the influence of interelectrode parasitic capacitances of the components and does not exceed 0.0002% at time of conversion not higher than 50 ms .

REFERENCES

[1] S. Purighalla, B. Maundy, "84-dB Range Logarithmic Digital-to-Analog Converter in CMOS 0.18-µm Technology", *IEEE Transactions on Circuits and Systems II: Express Briefs*, 58 (2011), no.5, pp. 279-283

[2] J. Lee, J. Kang, S. Park, J. Seo, J. Anders, J. Guilherme, M. P. Flynn, "A 2.5 mW 80 dB DR 36 dB SNDR 22 MS/s Logarithmic Pipeline ADC," *IEEE Journal Of Solid-State Circuits*, 44 (2009), no.10, pp. 2755-2765

[3] B. Maundy, D. Westwick, S. Gift, "On a class of pseudo-logarithmic amplifiers suitable for use with digitally switched resistors," *Int. J. of Circuit Theory and Applications*, vol. 36 (2008), no.1, pp. 81–108

[4] B. Maundy, D. Westwick, S. Gift, (2007) "A useful pseudo-logarithmic circuit," *Microelectronics International*, Vol. 24 Iss: 2, pp.35 - 45

[5] M. Alirieza, L. Jing and J. Dileepan, "Digital Pixel Sensor Array with Logarithmic Delta-Sigma Architecture," *Sensors*, 13(8), pp. 10765-10782, August 2013

[6] J. Guilherme, J. Vital, Jose Franca, "A True Logarithmic Analog-to-Digital Pipeline Convener with 1.5bitistage and Digital Correction," *Proc. IEEE International Conference on Electronics Circuits and Systems*, pp. 393-396, Malta 2001

[7] G. Bucci, M. Faccio, C. Landi, "The performance test of a piece-linear A/D converter," *IEEE Instrumentation and Measurement Technology Conference*, St. Paul USA May 1998, pp.1223.1228

[8] J. Guilherme, J. Vital, J. Franca, "A CMOS Logarithmic Pipeline *A/D* Converter with a Dynamic Range of 80 dB," *IEEE Electronics, Circuits and Systems, 2002. 9th International Conference on,* (2002), no.3/02, pp. 193-196

[9] J. Sit and R. Sarpeshkar, "A Micropower Logarithmic A/D With Offset and Temperature Compensation," *IEEE J. Solid-State Circuits*, 39 (2004), nr. 2, pp. 308-319

[10] J. Mahattanakul, "Logarithmic data converter suitable for hearing aid applications," *Electronic Letters*, 41 (2005), no.7, pp. 31-32

[11] S. Sirimasakul, A. Thanachayanont, W. Jeamsaksiri, "Low-Power Current-Mode Logarithmic Pipeline Analog-to-Digital Converter for ISFET based pH Sensor," *IEEE ISCIT*, 2009, no.6/09, pp. 1340-1343

[12] M. Santosa, N. Hortaa, J. Guilherme, "A survey on nonlinear analog-to-digital converters," *Integration, the VLSI Journal*, Volume 47, Issue 1, pp. 12–22, January 2014

[13] Z.R. Mychuda, "Logarithmic Analog-To-Digital Converters – ADC of the Future," Prostir, Lviv, Ukraine 2002, pp. 242

[14] A. Szcześniak, Z Myczuda, "A method of charge accumulation in the logarithmic analog-to-digital converter with a successive approximation," *Electrical Review*, 86 (2010), no.10, pp. 336-340

[15] A. Szcześniak, U. Antoniw, Ł. Myczuda, Z. Myczuda, „Logarytmiczne przetworniki analogowo-cyfrowe z nagromadzeniem ładunku i impulsowym sprzężeniem zwrotnym," *Electrical Review*, R. 89 no. 8/2013, pp. 277 – 281

[16] A. Szcześniak, Z. Myczuda, „Analiza prądów upływu logarytmicznego przetwornika analogowo-cyfrowego z sukcesywną aproksymacją," *Electrical Review,* 88 (2012), no. 5a, pp. 247-250

[17] J.H. Moon, D. Y. Kim, M. K. Song, Patent No. KR20110064514A, "Logarithmic Single-Slope Analog Digital Convertor, Image Sensor Device And Thermometer Using The Same, And Method For Logarithmic Single-Slope Analog Digital Converting,"

[18] J. Gorisse, F. A. Cathelin, A. Kaiser, E. Kerherve Patent No. EP2360838A1, "Method for logarithmic analog-to-digital conversion of an analog input signal and corresponding apparatus,"

[19] R. Offen Patent No. DE102008007207A1 "Logarithmierender Analog-Digital Wandler,"

[20] H. Suzunaga Patent No. US20080054163A1, "Logarithmic-compression analog-digital conversion circuit and semiconductor photosensor device,"