

Qucs Equation-Defined and Verilog-A Higher Order Behavioral Device Models for Harmonic Balance Circuit Simulation

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Abstract—This paper is concerned with the development and evaluation of a number of modeling techniques which improve Qucs Harmonic Balance simulation performance of RF compact device models. Although Qucs supports conventional SPICE semiconductor device models, whose static current/voltage and dynamic charge characteristics exhibit second and higher order derivatives may not be continuous, there is no guarantee that these will function without Harmonic Balance simulation convergence problems. The same comment also applies to a number of legacy compact semiconductor device models. The modeling of semiconductor devices centered on non-linear Equation-Defined Devices and blocks of Verilog-A code, combined with linear components, is introduced. These form a class of compact macromodel that has improved Harmonic Balance simulation performance. To illustrate the presented modeling techniques RF diode, BJT and MESFET macromodels are described and their Harmonic Balance performance simulated with Qucs and Xyce©.

Index Terms—Qucs, Xyce, Harmonic Balance RF simulation, compact semiconductor device modelling, equation-defined devices, macromodels.

I. INTRODUCTION

SINCE the adoption by the Qucs circuit simulation community of Equation-Defined Devices (EDD) [1] and Verilog-A analogue modules for compact device modeling [2] they have become amongst the most widely used forms of non-linear device model for established and emerging technologies [3]. The release of the open source General Public License (GPL) “Automatic Device Model Synthesizer” (ADMS) [4], has ensured that Verilog-A will remain one of the dominant compact modeling languages for the foreseeable future. Although ADMS only handles a sub-set of Verilog-A it includes a number of language statements which simplify compact semiconductor device model design [5]. Verilog-A modules and EDD models are now established as important Qucs modeling features. Qucs treats EDD models and Verilog-A modules as non-linear entities, including those with interface ports linked to internal model nodes via resistors implemented with EDD two terminal branches or Verilog-A code. This structure implies that only non-linear components are connected to internal model nodes. In general, such models function correctly in the DC, AC and Transient simulation domains.

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However, they often do fail during Harmonic Balance (HB) simulation, mainly due to problems occurring when circuits are partitioned into a frequency domain linear subcircuit and a time domain non-linear subcircuit or because of large changes in device bias points between circuit equation iterative solution steps [6]. Nodes with only non-linear components connected can make partitioning especially difficult, often resulting in HB simulation non-convergence [6]. A reevaluation of the role of EDD and Verilog-A modules suggests that reserving either for the non-linear sections of an HB model reduces partition failure, provided the remaining model components are linear and at least one linear component is connected to each macromodel node. Moreover, this structure naturally builds into a compact macromodel. Non-linear EDD and Verilog-A modules with current or charge characteristics that have discontinuous differential terms can also be a source of HB simulation non-convergence. This paper introduces EDD and Verilog-A macromodeling techniques which attempt to eliminate the problems found with Qucs HB circuit partitioning and device model discontinuities. Semiconductor diode, BJT and MESFET HB macromodels are described and their performance simulated with the Qucs and Xyce ©[7] circuit simulators. The Xyce circuit simulator includes multi-tone signal HB simulation features that are not available with the current release of Qucs while simultaneously providing a very stable form of single tone HB simulation, making the package useful for cross checking Qucs HB simulation data.

II. OVERVIEW OF THE QUCS/SPICE4QUCS SUBSYSTEM FOR CIRCUIT SIMULATOR

Qucs is distributed with a built-in simulation kernel called Qucsator. Qucs software spice4qucs series snapshots released since stable release-0.0.18 include an experimental subsystem called spice4qucs [8]. This subsystem allows simulation of Qucs schematics with external SPICE-compatible GPL simulation engines. Currently, the Qucs/spice4qucs software package supports both the ngspice [9] and Xyce (serial and parallel versions) circuit simulators. The spice4qucs extension is enabled by default for Qucs development snapshots and stable software releases after Qucs-0.0.19. The spice4qucs extension interfaces directly with Qucs schematic capture at the Qucs graphical user interface (GUI) level, extending the Qucs legacy simulation and modelling features by adding more simulation routines and extra component models that were only previously available with SPICE simulators. The spice4qucs extension consists of the following major parts:

- 1) A SPICE netlist builder: this converts Qucs schematic generated netlists into SPICE style netlists.
- 2) A SPICE raw ASCII output file parser: this generates a Qucs XML output dataset and passes it to the Qucs visualization system for post-simulation data processing, tabulation and graphical display.

The block diagram given in Figure 1 illustrates the interface and interaction between the Qucs schematic capture process and Qucs simulation data visualization. The data flow implied by Figure 1 indicates how Qucs builds a SPICE netlist (from a circuit schematic), passes it to the selected simulation engine, undertakes circuit simulation and finally parses the resulting XML output data to either the Qucs internal post-simulation numerical processing routines or to external Octave©[10] numerical analysis and visualization software. In general, legacy Qucs schematics constructed from basic circuit simulation components only require minimal or no manual tweaking for error free simulation with Ngspice or Xyce. The following features are currently implemented by the Qucs/spice4qucs circuit simulation package:

- 1) Ngspice, Xyce (both serial and parallel) supported: Use Xyce-parallel with the “OpenMPI” protocol for best simulation performance.
- 2) Basic SPICE support for .DC, .AC, .TRAN simulation.
- 3) Advanced SPICE simulation support: including .FOUR, .DISTO, .NOISE, and .HB simulation types.
- 4) All legacy Qucs circuit simulation features are fully supported and are unaffected by the spice4qucs subsystem extensions.
- 5) Semiconductor devices with full SPICE .MODEL format are implemented, allowing directly embedded SPICE-models, taken from manufactures device data-sheets, in Qucs schematics.
- 6) The spice4qucs extensions fully support Qucs equations, SPICE parametrization (.PARAM) statements, and ngntumeg scripts, including the use of ngntumeg equations for post-simulation data processing purposes.
- 7) Custom controlled ngspice simulation via ngntumeg scripts: this extended circuit simulation capability uses embedded user-defined ngntumeg scripts, listed on a Qucs schematic, for the control of simulation sequences and the processing of simulation output data. This feature is especially useful for non-standard SPICE circuit simulation such as statistical analysis of circuit performance.
- 8) Full support for Qucs EDD and SPICE B non-linear sources: this feature allows compact modeling of existing and emerging technology devices. It is particularly useful for interactive development and testing of new compact device models.

Although the Qucsator, ngspice and Xyce circuit simulators are designed for analog circuit simulation they are not fully compatible with each other in that they offer different simulation facilities, for example Qucsator and Xyce implement HB while ngspice does not. Similarly, all three simulators have some form of built-in algebraic/numerical features for evaluating component values, and other quantities like device

parameters, the set of implemented mathematical operators and functions are again not fully compatible. One example of this form of incompatibility is the commonly used “if” statement. Qucsator and Ngspice implement the “if” statement as a C style ternary operator $x?y : z$. However, with Xyce the C style ternary operator is replaced by a Heaviside step function $\sigma(x)$, for example in each of these cases implementing a current-voltage statement $I=f(V)$, yields:

- 1) For Qucsator and ngspice:

$$I = (V > V(th)) ? f(V) : g(V), \text{ where } V(th) \text{ is a threshold voltage such that}$$

$$I = f(V) \text{ for } V > V(th) \text{ else } I = g(V).$$

- 2) For Xyce:

$$I = f(V) \cdot \sigma(V - V(th)) + g(V) \cdot \sigma(V(th) - V),$$

where $\sigma(V - Vth) = 1$ when $V > V(th)$, and $\sigma(V - Vth) = 0$ when $V < V(th)$.
Similarly, $\sigma(Vth - V) = 0$ when $V > V(th)$, and $\sigma(Vth - V) = 1$ when $V < V(th)$.

Ngspice and Xyce represent the Heaviside step function $\sigma(x)$ with functions named $step(x)$ and $stp(x)$, respectively. Unfortunately, Xyce is not equipped with scripting language like Qucsator and ngspice which limits its post-simulation data precessing capabilities. When constructing compact models, for use with more than one circuit simulator, any differences in simulator functionality and in the specification of implemented scripting mathematical functions must be carefully considered, otherwise simulation failure may occur.

III. MODELING A DIODE NON-LINEAR STATIC CURRENT-VOLTAGE CHARACTERISTIC

A basic compact device model for a semiconductor diode is shown in Fig. 2. To prevent HB floating point numerical overflow in the diode forward bias region of operation the Verilog-A function $limexp$ is often used to calculate diode current, rather than the standard exponential function exp . When computed diode voltages have a value such that $\delta \cdot Vd > 80$ function $limexp$ linearizes the diode current characteristic equation in an attempt to prevent numerical overflow. At the crossover point between the diode exponential and linear regions of operation the Id and dId/dVd curves are continuous. Qucs C++ code represents real numbers using IEEE binary 64 bit real numbers. These have a decimal range of roughly $\pm 2.23 \cdot 10^{-308}$ to $\pm 1.80 \cdot 10^{308}$. Writing the diode equation given in Fig. 2 in terms of a critical voltage $Vcrit$, which represents the value of Vd where Id changes from the exponential to the linear region of operation, yields equations (1) and (2) respectively.

$$Id = Is \cdot (exp(\delta \cdot Vd) - 1), \quad \forall (Vd \leq Vcrit) \quad (1)$$

$$Id = Is \cdot exp(\delta \cdot Vcrit) \cdot [1 + \delta \cdot (Vd - Vcrit)], \quad \forall (Vd > Vcrit) \quad (2)$$

where $exp(\delta \cdot Vcrit) \gg 1.0$ and $Vcrit = 308/\delta$ volts. For $N = 1$ and $T = 300$ Kelvin, $Vcrit(max) \approx 7.7$ volts. Hence with $N = 1$, adopting a value of $Vcrit$ near to, but below 7.7 volts, will ensure that values of Vd below $Vcrit$ do not cause floating point overflow when calculation Id [6]. In the exponential region of operation the first and higher

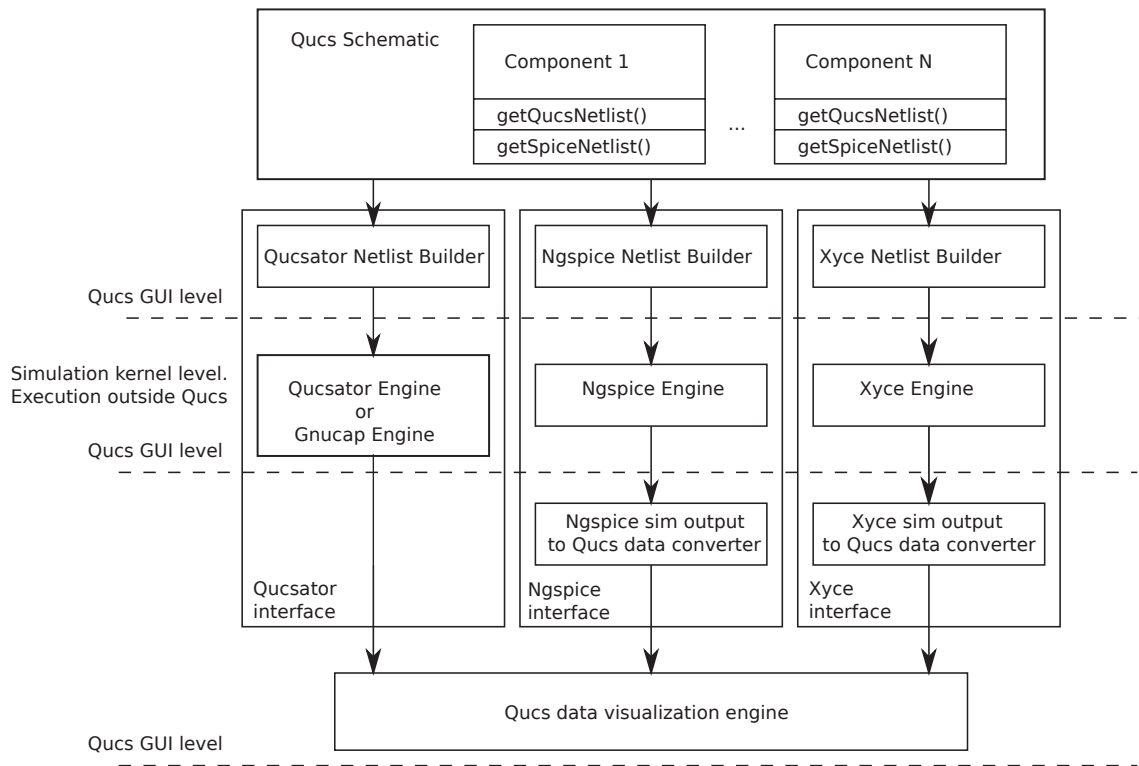
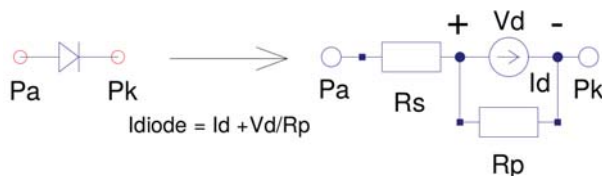


Fig. 1. Spice4qucs subsystem block diagram.

order current derivatives are continuous which is ideal for HB simulation. However, in the linear region of operation ($V_d > V_{crit}$) only the first order derivative is continuous. Figures 3 and 4 introduce a non-linear EDD model and a Verilog-A module which, when either are combined with linear resistors R_s and R_p , form a compact diode macromodel. Typical simulated DC data for a diode macromodel under test are given in Fig. 5. The test circuit has $V_{crit} = 0.6$ volts. This value is set artificially low in order to demonstrate the change from the exponential to the linear region of operation in the diode I_d characteristic. In Fig. 5 the plot of $\frac{d^2 I_d}{dV d^2}$ against V_d clearly illustrates a discontinuity at $V_d = 0.6$ volts



where $I_d = I_s \cdot (\text{limexp}(\delta \cdot V_d) - 1)$, $\delta = e / (N \cdot K \cdot T)$
 and $\text{limexp}(X) = (X < 80) ? \exp(X) : \exp(80) \cdot (1 - (X - 80))$

Fig. 2. A semiconductor diode static I/V model: N is the diode emission coefficient, e is the electron charge, K is the Boltzmann constant, T is the diode temperature in Kelvin, R_s is the series bulk and contact resistance and R_p a diode junction parallel leakage resistance.

A more general equation for the diode model current I_d , when $V_d > V_{crit}$, is given by equation 3.

$$I_d = I_s \cdot \exp(\delta \cdot V_{crit}) \cdot \sum_{i=0}^p \frac{\delta^i}{i!} (V_d - V_{crit})^i \quad \forall (V_d > V_{crit}) \quad (3)$$

where $0 \leq p \leq 5$. Illustrated in Fig. 6 are a typical set of DC simulation data obtained from the test circuit shown in Fig.5 and a diode model based on the extended macromodel defined by equation 3. In this example both $Diff1$ and $Diff2$ are continuous, making the model more suitable for HB simulation.

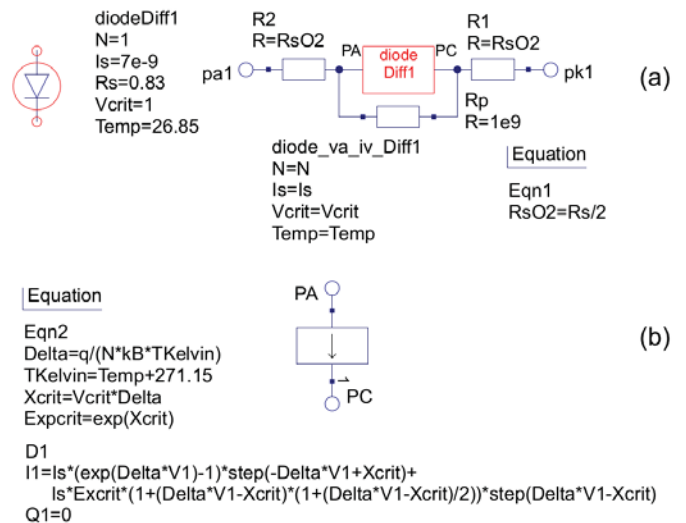


Fig. 3. A diode compact macromodel: (a) Qucs schematic symbol and macromodel circuit, (b) Qucs EDD diode current $I1$ selected with function $\text{step}()$. For clarity $D1 : I1$ is displayed on more than one line.

```

// Diode I/V HB model diode_va_iv_Diff1.va
`include "disciplines.vams"
`include "constants.vams"
module diode_va_iv_Diff1(pa,pk);
inout pa, pk; electrical pa, pk;
parameter integer N = 1 from [1 : inf];
parameter real Is = 1e-14 from [1e-20 : inf];
parameter real Vcrit = 0.6 from [0.4 : 5];
parameter real Temp = 26.85 from [-100 : 200];
parameter real Tnom = 26.85 from [-100 : 200];
real TKelvin, Delta, Xcrit, Expcrit, X;
analog begin
@ (initial_model)
begin
TKelvin = Temp+271.15; Delta = `P_Q/(N*`P_K*TKelvin);
Xcrit = Vcrit*Delta; Expcrit = exp(Xcrit);
end
X = Delta*V(pa, pk);
I(pa,pk) <+ (X <= Xcrit) ? Is*(exp(X)-1) : Is*Expcrit*(1+(X-Xcrit));
end
endmodule

```

Fig. 4. Qucs diode Verilog-A code: diode current $I(pa, pk)$ selected with ternary operator $x?y : z$.

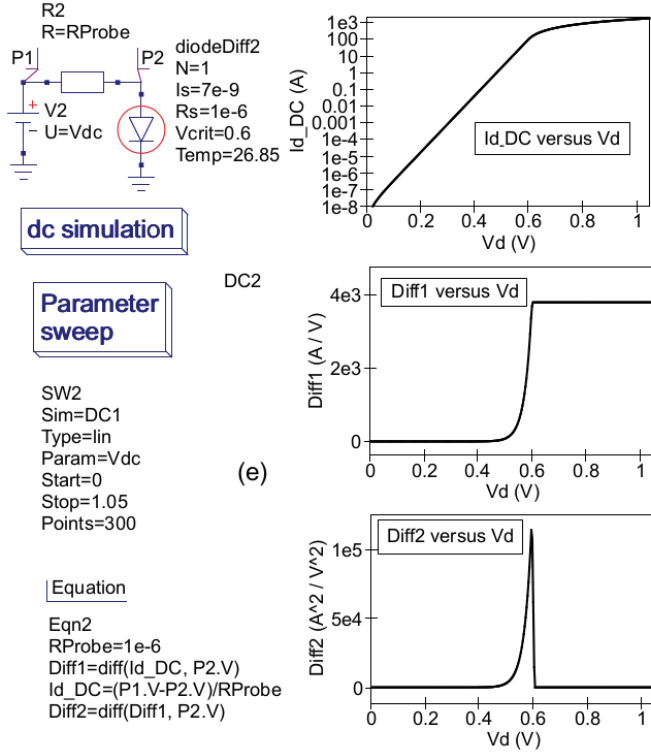


Fig. 5. QuCS compact diode macromodel test circuit and simulated DC current characteristics: $I_{d_DC} = Id$, $Diff1 = \frac{dId}{dVd}$, and $Diff2 = \frac{d^2Id}{dVd^2}$.

IV. MODELING DIODE NON-LINEAR DYNAMIC CHARGE CHARACTERISTICS

Semiconductor diode diffusion and depletion capacitance are given by equations 4, 5 and 6 [11].

$$C_{diff} = \frac{dQ_{diff}}{dVd} = Tt \cdot \frac{dId}{dVd} \quad (4)$$

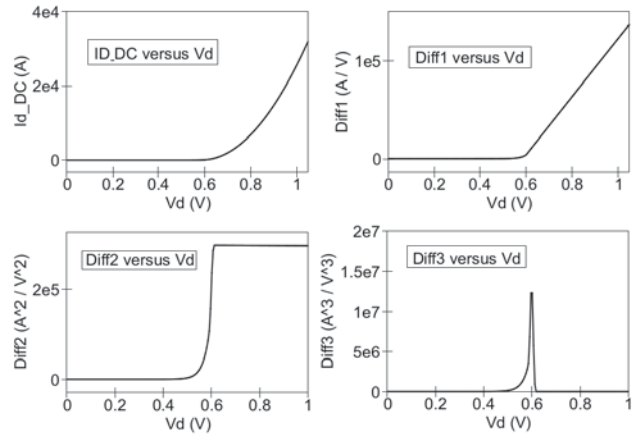


Fig. 6. Extended diode compact macromodel simulated DC current characteristics for $p = 2$, $V_{crit} = 0.6$ V, $Is = 7e-9$ A, $Rs = 1e-6$ Ω and $T = 300$ Kelvin: $I_{d_DC} = Id$, $Diff1 = \frac{dId}{dVd}$, $Diff2 = \frac{d^2Id}{dVd^2}$ and $Diff3 = \frac{d^3Id}{dVd^3}$.

where Tt is the diode transit time in seconds.

$$C_{dep} = \frac{dQ_{dep}}{dVd} = Cj0 \cdot \left[1 - \frac{Vd}{Vj}\right]^{-M} \forall \left(Vd < \frac{Vj}{2}\right) \quad (5)$$

$$C_{dep} = 2^M \cdot Cj0 \cdot [2 \cdot M \cdot \frac{Vd}{Vj} + (1 - M)] \forall \left(Vd \geq \frac{Vj}{2}\right) \quad (6)$$

where $Cj0$ is the zero bias junction capacitance in Farads, M is a pn junction grading coefficient, Vj is the junction potential voltage in Volts, and Q_{diff} and Q_{dep} are stored diffusion and depletion charges in Coulombs respectively. To reduce the effect of the discontinuity in equation 5 at $Vd = Vj$ the depletion capacitance can be represented by equations 5 and 7.

$$C_{dep} = 2^M \cdot Cj0 \cdot \sum_{i=0}^p \frac{(Vd - Vmax)^i}{i!}, \forall \left(Vd \geq \frac{Vj}{2}\right) \quad (7)$$

where $0 < p \leq 5$. Although equation 7 gives an approximate value for C_{dep} at $Vd > Vj/2$ it is normally acceptable because C_{diff} is the dominant capacitive component in this region of diode operation. Setting $p = 2$ and integrating equations 4, 5 and 7 gives

$$Q_{diff} = Tt \cdot Id \quad (8)$$

$$Q_{dep} = Cj0 \cdot \left(\frac{Vj}{(1-M)}\right) \cdot \left[1 - \left(1 - \frac{Vd}{Vj}\right)^{1-M}\right], \forall \left(Vd < \frac{Vj}{2}\right) \quad (9)$$

$$Q_{dep} = 2^M \cdot Cj0 \left[Vdiff + \frac{Vdiff^2}{2} + \frac{Vdiff^3}{6}\right], \forall \left(Vd \geq \frac{Vj}{2}\right) \quad (10)$$

where $Vdiff = Vd - Vmax$ and $Vmax = Vj/2$. A modified EDD macromodel which includes Q_{diff} and Q_{dep} is shown in Fig. 7. The Verilog-A code for this model is similar to the module code listed in Fig. 4 with $I(Pa, Pk) <+ ddt(Q1)$ added, where $Q1 = Q_{diff} + Q_{dep}$. Shown

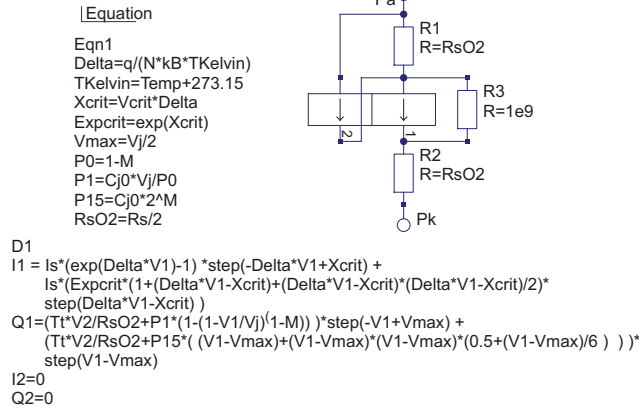


Fig. 7. A semiconductor diode EDD macromodel including dynamic charge characteristics. For clarity EDD $D1$ current $I1$ and charge $Q1$ are displayed on more than one line.

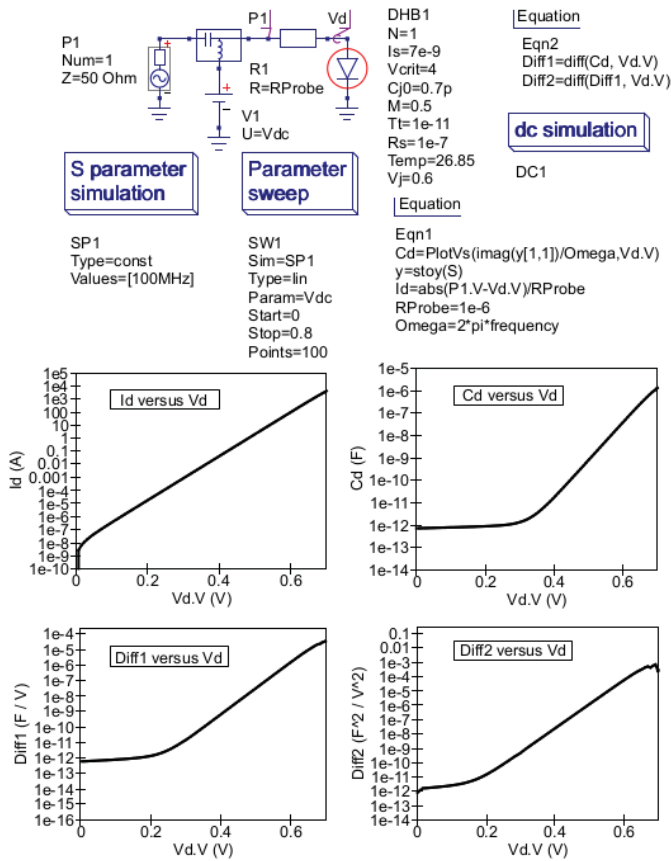


Fig. 8. Diode compact macromodel S parameter simulation: test circuit and Equation scripts for extracting diode capacitance from Qucs S parameter simulated values.

in Fig. 8 is a test circuit for extracting semiconductor diode capacitance from S parameter simulated data. In this circuit the diode under test has series resistance R_s set at $0.1\mu\Omega$ to ensure that R_s does not affect the accuracy of the extracted values of C_d . The diode under test has DC bias voltage V_{dc} swept over the range 0 to 0.8 volts and, at each bias

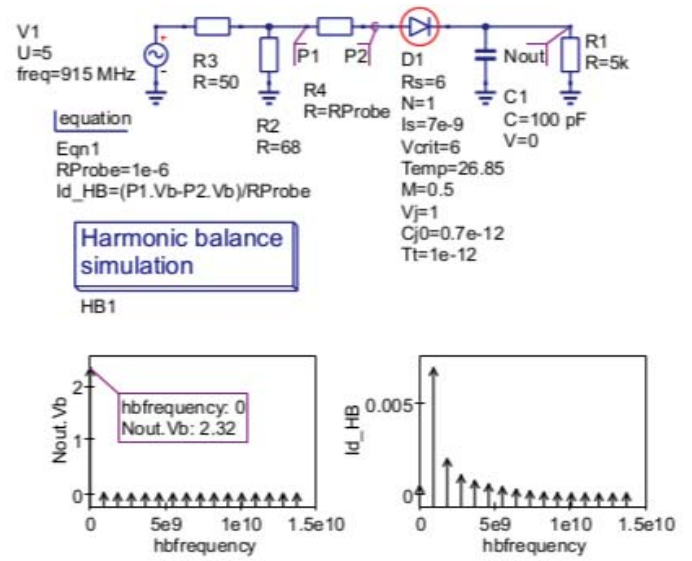


Fig. 9. RF diode detector test set and HB simulation data plots: $I_s = 7e-9A$, $N = 1$, $V_j = 1.0V$, $R_s = 6\Omega$, $C_{j0} = 0.7pF$ and $T_t = 1e-12s$.

point, $S[1, 1]$ determined with Qucs S parameter simulation. Conversion of $S[1, 1]$ to $y[1, 1]$ allows diode capacitance values to be extracted from the imaginary component of the $y[1, 1]$ data; $C_d = \text{imag}(y[1, 1]) / (2 \cdot \pi \cdot \text{frequency})$. Diode parameter V_j is set at 0.6 volts to be able to observe any discontinuities in the diode capacitance characteristics. Fig. 8 presents plots of C_d , and its first two derivatives, with respect to diode bias voltage V_d . These suggest that the change in depletion capacitance given by equations 5 and 7 is smooth and does not introduce any significant discontinuities in the diode capacitance characteristic.

V. HARMONIC BALANCE AND TRANSIENT SIMULATION OF AN RF DIODE DETECTOR

The diagram in Fig. 9 shows an unbiased RF diode detector circuit and a set of Qucs HB simulation output voltage and diode current spectral plots for a 915 MHz five volt peak AC input signal. The detector diode model parameters are similar

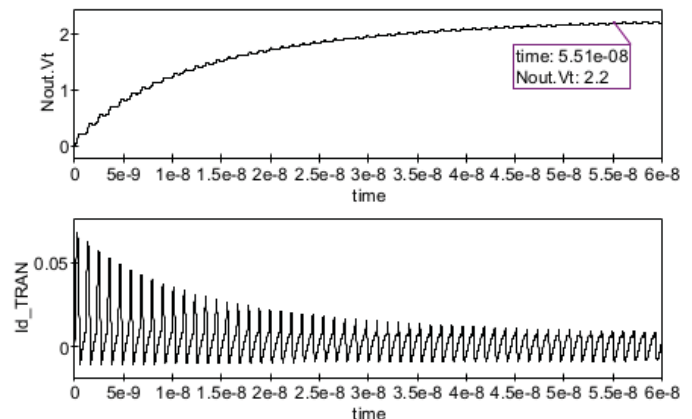


Fig. 10. RF diode detector transient simulation data plots: $N_{out.Vt}$ and I_{d_TRAN} against time.

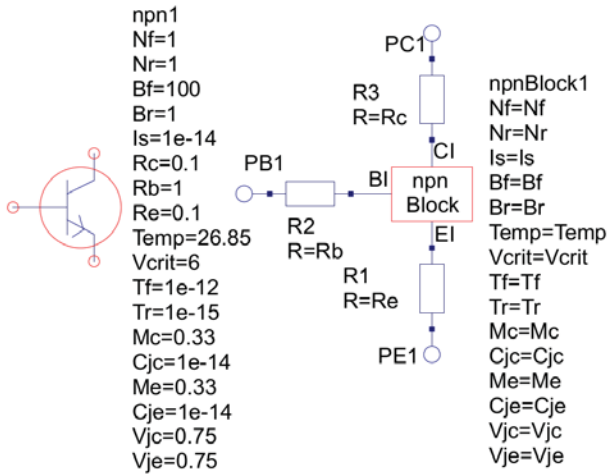


Fig. 11. An npn BJT compact macromodel: symbol and circuit.

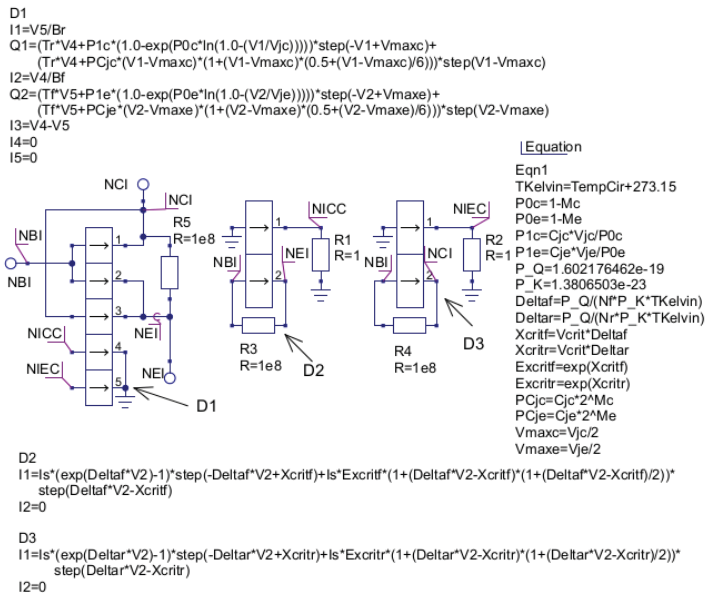


Fig. 12. A Qucs npn BJT EDD macromodel block *npnBlock*: For clarity EDD *D2* and *D3* currents (*I1*) and charge *Q1* are displayed on more than one line, BJT current and charge equations are selected with function *step()*.

to the AVAGO HSMS-2820 published SPICE parameters [12]. This particular circuit illustrates the performance of the diode HB compact macromodel and how effective HB simulation is in determining the AC steady state response of RF circuits, particularly when compared to number of AC input signal cycles needed before the transient simulation output voltage *Nout.Vt* approaches a steady state response, see Fig.10.

VI. A BJT COMPACT MACROMODEL FOR HARMONIC BALANCE SIMULATION

A Qucs compact macromodel for an npn BJT modeled by a large signal Ebers-Moll I/V characteristic and non-linear stored charge is given in Fig. 11. This macromodel is constructed from a nonlinear block called *npnBlock* and three linear resistors connecting port terminals *PC1*, *PB1* and *PE1* to *npnBlock*. Figures 12 and 13 present details of the npn BJT

```

`include "disciplines.vams"
`include "constants.vams"
module npnBlock(CI, BI, EI);
inout CI, BI, EI; electrical CI, BI, EI;
parameter integer Nf = 1 from [1 : inf];
parameter integer Nr = 1 from [1 : inf];
parameter real Is = 1e-14 from [1e-20 : inf];
parameter real Bf = 100 from [1 : inf];
parameter real Br = 1 from [0.1 : inf];
parameter real Vcrit = 6 from [0.5 : inf];
parameter real Tf = 1e-12 from [1e-20 : inf];
parameter real Tr = 1e-11 from [1e-20 : inf];
parameter real Mc = 0.33 from [0.05 : 5];
parameter real Cjc=1.0e-14 from [1.0e-20 : inf];
parameter real Vjc=0.75 from [0.1 : inf];
parameter real Me = 0.33 from [0.05 : 5];
parameter real Cje=1.0e-14 from [1.0e-20 : inf];
parameter real Vje=0.75 from [0.1 : inf];
parameter real Temp = 26.85 from [-100 : 200];
parameter real Tnom = 26.85 from [-100 : 200];
real TKelvin, Deltaf, Deltar, Xcritf;
real Xcritr, Expcritf; Expcritr, PCjc;
real PCje, Vmaxc, Vmaxe, ICC, IEC, Xr;
real Xf,Vdiffr,Qtc, P0c, P1c, Vdiff;
real Qte, P0e, P1e;
analog begin
@ (initial_model)
begin
TKelvin = Temp+273.15;
Deltaf = `P_Q/(Nf*`P_K*TKelvin);
Deltar = `P_Q/(Nr*`P_K*TKelvin);
Xcritf = Vcrit*Deltaf;
Xcritr = Vcrit*Deltar;
Expcritf = exp(Xcritf);
Expcritr = exp(Xcritr);
PCjc = Cjc*exp(Mc*ln(2));
PCje = Cje*exp(Me*ln(2));
Vmaxc = Vjc/2; Vmaxe = Vje/2;
P0c = 1-Mc; P1c=Cjc*Vjc/P0c;
P0e=1-Me; P1e=Cje*Vje/P0e;
end
Xr=Deltar*V(BI,CI);
IEC=(Xr-Xcritr) ? Is*(exp(Xr-1)
: Is*Expcritr*(1+(Xr-Xcritr)*
(1+(Xr-Xcritr)/2));
I(BI,CI) <+ IEC/Br; Vdiffr = V(BI,CI)-Vmaxc;
Qtc = (V(BI,CI) < Vmaxc
? Tr*ICC+PCjc*(1.0-exp(P0c*ln(1.0-V(BI,CI)/Vjc)))
: Tr*ICC+PCjc*(Vdiffr +Vdiffr*Vdiffr/2 +
Vdiffr*Vdiffr*Vdiffr/6);
I(BI,CI) <+ ddt(Qtc); Xf=Deltaf*V(BI,EI);
ICC=(Xf-Xcritf) ? Is*(exp(Xf)-1)
: Is*Expcritf*(1+(Xf-Xcritf)*
(1+(Xf-Xcritf)/2));
I(BI,EI) <+ ICC/Bf; Vdiff = V(BI,EI)-Vmaxe;
Qte = (V(BI,EI) < Vmaxe)
? Tf*IEC+PCje*(1.0-exp(P0e*ln(1.0-V(BI,EI)/Vje)))
: Tf*IEC+PCje*(Vdiff +Vdiff*Vdiff/2 +
Vdiff*Vdiff*Vdiff/6);
I(BI,EI) <+ ddt(Qte); I(CI,EI) <+ ICC-IEC;
end
endmodule
  
```

Fig. 13. A Qucs npn BJT Verilog-A code block *npnBlock* : BJT current and charge equations are selected with ternary operator *x?y : z*.

nonlinear static current and dynamic charge properties derived from the semiconductor diode model introduced previously. Figure 14 introduces a basic BJT test bench and a set of Qucs HB and transient simulation derived frequency domain spectral plots for the voltage at output node Pc . The latter being obtained with FFT techniques, see Qucs equation *Eqn5* Fig. 14. DC voltage sources $V3$ and $VinDC$ were set at 15V and 0.65V to bias the BJT output node Pc at a quiescent DC voltage of approximately 10V at a collector current of 2mA. Comparison of the HB and transient voltage spectral data for node Pc , with $VinAC$ a single tone AC test signal of 1MHz frequency and 20mV peak amplitude, indicates good agreement between both sets of data. The latest development version of Qucs/spice4qucs [13] includes routines for generating Xyce netlists from Qucs schematics. A Xyce netlist for the *nnpBlock* macromodel is given in Fig. 15. This netlist has a similar structure to both the Qucs EDD *nnpBlock* model, Fig. 12, and the Verilog-A *nnpBlock* module, Fig. 13, introduced previously. However, some minor adjustments were required to the Xyce netlist due to incompatibilities in some parameter and function names, for example Qucs *Temp* is replaced by *TempCir* and Qucs function *step()* is replaced by Xyce function *stp()*. Shown in Fig. 16 is the Xyce HB simulation spectral data for the magnitude of the voltage at test circuit node Pc . The data illustrated in Fig. 16 confirm the values obtained with Qucs HB simulation. Figure 17 gives a circuit for a single stage RF BJT amplifier and set of typical simulation output data. This amplifier is designed to give a 20 dB voltage gain at midband frequencies. The theoretical value of the amplifier midband voltage gain is given by equation 11 and is mainly determined by the negative feedback introduced by resistor $R9$. The Qucs plots of small signal AC and HB simulation data show very similar values for the output voltage at node $Nout$.

$$V_{gain} \approx 20 \cdot \log(R1/R9) \quad (11)$$

VII. A MESFET COMPACT DEVICE MODEL FOR HB RF CIRCUIT SIMULATION

A Xyce Curtice level 1 MESFET EDD model with fixed linear interelectrode capacitances is shown in Figure 19. This macromodel consists of two EDD blocks: $D1$ and $D2$, where block $D2$ models non-linear drain to source current characteristics and linear capacitances CGS and CDS and block $D1$ models linear capacitance CGD . Inductances L_d , L_g , and L_s are also assumed to be linear and external to the main body of the Xyce Curtice model. In an attempt to ensure that this model converges to an acceptable electrical solution during HB simulation each of the model nodes has at least one linear component attached. The model shown in Figure 19 exhibits the following noteworthy features: (1) the drain and source terminals may be interchanged, (2) multiple Xyce *stp()* functions act as an *if-then-else* statement and (3) resistor $R1$ (Figure 19), added to the MESFET source lead, introduces a DC current sensing function via EDD $D1$ voltages $V2$ and $V3$, allowing device diffusion capacitance to be easily calculated.

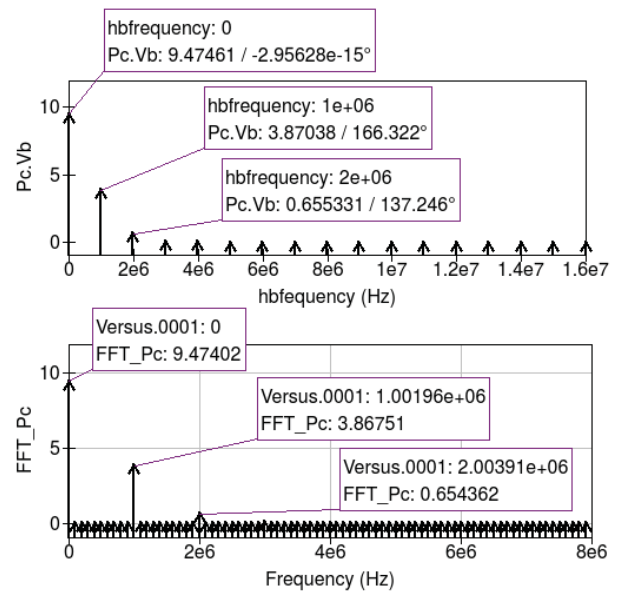
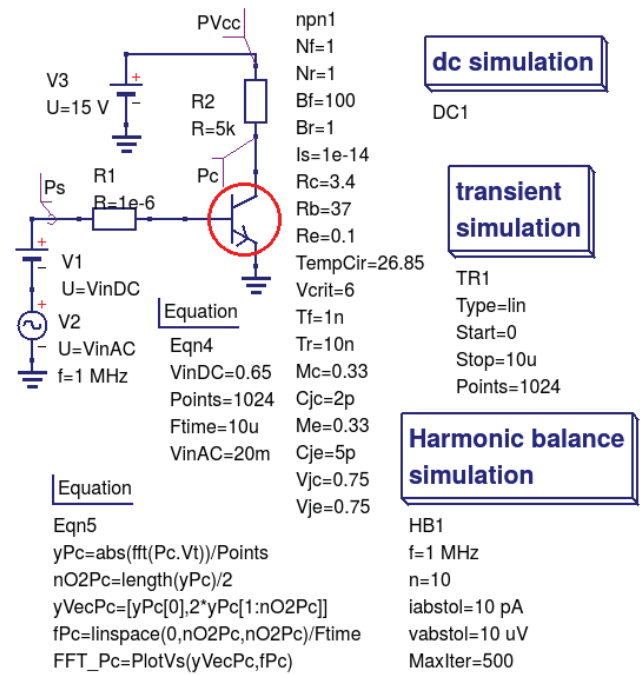


Fig. 14. A BJT HB and transient simulation test bench: Circuit, node Pc HB simulation data and frequency domain spectral plot of transient simulation data.

The SPICE code of the Xyce Curtice Level 1 MESFET macromodel is shown in the Figure 18. This was obtained automatically using the spice4qucs SPICE netlist builder.

VIII. A COMPARISON OF QUCS AND XYCE MESFET AMPLIFIER HB SIMULATION

The final example simulation in this paper introduces a single stage MESFET amplifier test circuit and a set of typical comparison data for the Qucs and Xyce HB simulations. Illustrated in Figure 20 is a basic single stage MESFET RF amplifier with a $5k\Omega$ resistive load and high impedance DC gate biasing network. In Figure 20 a single tone sine wave

```
.SUBCKT npnBlock NCI NBI NEI Nf=1 Nr=1 Is=1e-14 Bf=100 Br=1
+ TempCir=26.85 Vcrit=6 Tf=1e-12 Tr=1e-11 Mc=0.33 Cjc=1e-12
+ Me=0.33 Cje=1e-12 Vjc=0.75 Vje=0.75 Rc=1e-3 Rb=1e-3 Re=1e-3
.PARAM TKelvin=(TempCir+271.15)
.PARAM P0c={1-Mc}
.PARAM P0e={1-Me}
.PARAM P1c={Cjc*Vjc/P0c}
.PARAM P1e={Cje*Vje/P0e}
.PARAM P_Q=1.602176462e-19
.PARAM P_K=1.3806503e-23
.PARAM Deltaf={P_Q/(Nf*P_K*TKelvin)}
.PARAM Deltar={P_Q/(Nr*P_K*TKelvin)}
.PARAM Xcritf={Vcrit*Deltaf}
.PARAM Xcritr={Vcrit*Deltar}
.PARAM Excritf={exp(Xcritf)}
.PARAM Excritr={exp(Xcritr)}
.PARAM PCjc={Cjc*2**Mc}
.PARAM PCje={Cje*2**Me}
.PARAM Vmaxc={Vjc/2}
.PARAM Vmaxe={Vje/2}
R2 0 NIEC 1
R1 0 NICC 1
BD2I0 0 NICC I=Is*(exp(Deltaf*V(NBI,NEI))-1)*
+ stp(-Deltaf*V(NBI,NEI)+Xcritf)+Is*Excritf*
+ (1+(Deltaf*V(NBI,NEI)-Xcritf)*(1+(Deltaf*V(NBI,NEI)-Xcritf)/2))*
+ stp(Deltaf*V(NBI,NEI)-Xcritf)
BD2I1 NBI NEI I=0
BD3I0 0 NIEC I=Is*(exp(Deltar*V(NBI,NCI))-1)*
+ stp(-Deltar*V(NBI,NCI)+Xcritr)+Is*Excritr*
+ (1+(Deltar*V(NBI,NCI)-Xcritr)*(1+(Deltar*V(NBI,NCI)-Xcritr)/2))*
+ stp(Deltar*V(NBI,NCI)-Xcritr)
BD3I1 NBI NCI I=0
R3 NEI NBI 1E8
R4 NCI NBI 1E8
R5 NEI NCI 1E8
BD1I0 NBI NCI I=V(NIEC)/Br
GD1Q0 NBI NCI nD1Q0 NCI 1.0
LD1Q0 nD1Q0 NCI 1.0
BD1Q0 nD1Q0 NCI I=-((Tr*V(NICC)+P1c*
+ (1.0-exp(P0c*ln(1.0-(V(NBI,NCI)/Vjc)))))*
+ stp(-V(NBI,NCI)+Vmaxc)+(Tr*V(NICC)+PCjc*(V(NBI,NCI)-Vmaxc)*
+ (1+(V(NBI,NCI)-Vmaxc)*(0.5+(V(NBI,NCI)-Vmaxc)/6))))*
+ stp(V(NBI,NCI)-Vmaxc))
BD1I1 NBI NEI I=V(NICC)/Bf
GD1Q1 NBI NEI nD1Q1 NEI 1.0
LD1Q1 nD1Q1 NEI 1.0
BD1Q1 nD1Q1 NEI I=-((Tr*V(NIEC)+P1e*
+ (1.0-exp(P0e*ln(1.0-(V(NBI,NEI)/Vje)))))*
+ stp(-V(NBI,NEI)+Vmaxe)+(Tr*V(NIEC)+PCje*(V(NBI,NEI)-Vmaxe)*
+ (1+(V(NBI,NEI)-Vmaxe)*(0.5+(V(NBI,NEI)-Vmaxe)/6))))*
+ stp(V(NBI,NEI)-Vmaxe))
BD1I2 NCI NEI I=(V(NICC)-V(NIEC))
BD1I3 NICC 0 I=0
BD1I4 NIEC 0 I=0
.ENDS
```

Fig. 15. A Xyce npn BJT SPICE subcircuit *npnBlock* : BJT current and charge equations are selected with function *stp()*.

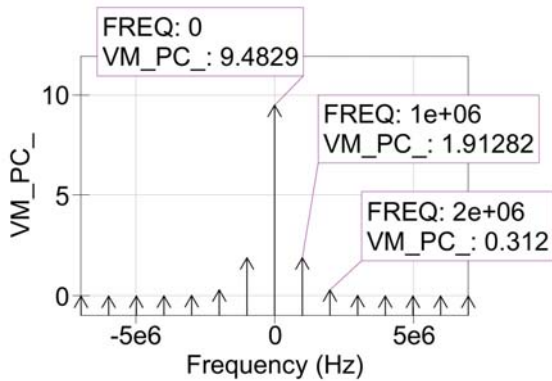
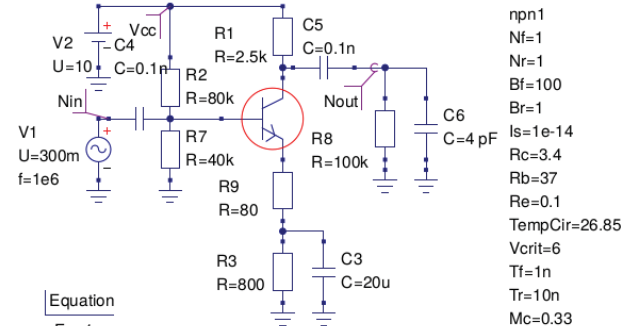
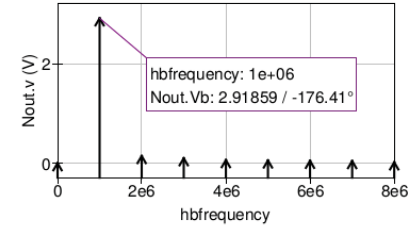
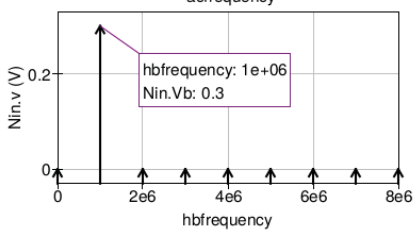
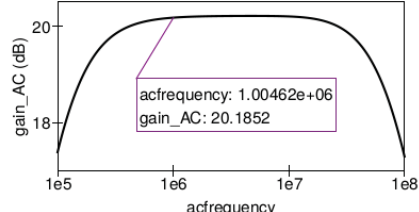


Fig. 16. Xyce HB simulation data for the magnitude of node *Pc* voltage: Test configuration identical to Fig. 14.



Equation
Eqn1
gain_AC=dB(Nout.v/Nin.v)



- npn1
- Nf=1
- Nr=1
- Bf=100
- Br=1
- Is=1e-14
- Rc=3.4
- Rb=37
- Re=0.1
- TempCir=26.85
- Vcrit=6
- Tf=1n
- Tr=10n
- Mc=0.33
- Cjc=2p
- Me=0.33
- Cje=5p
- Vjc=0.75
- Vje=0.75

dc simulation

DC1

ac simulation

AC1
Type=log
Start=1e5
Stop=1e8
Points=1001

Harmonic balance simulation

HB1
f=1 MHz
n=8
iabstol=10 uA
vabstol=10 uV
retol=0.01
MaxIter=500

Fig. 17. A 20dB single stage npn transistor RF amplifier: circuit, small signal AC voltage gain and HB simulation data obtained with *R9* adjusted to give a gain of 20dB at 1MHz.

signal is applied to the gate of the MESFET device via AC coupling capacitor *C1*. Qucs and Xyce plotted HB simulation data are given in Figure 21.

Qucs HB simulation data is output as a plot of frequency domain spectral amplitude components $|H|$,

$$|H| = U_0(0), U(f_1), U(f_2), U(f_3), \dots \quad (12)$$

where $U(f_n)$ is the magnitude of a harmonic component at frequency f_n and $n = 1, 2, 3, \dots$. In contrast to the Qucs circuit simulator Xyce outputs HB data as a plot of complex conjugated spectral amplitude components H in the negative ($-f$) and positive (f) frequency domains, where

$$|H| = U_0(0), 2 \cdot \sqrt{U(-f_1) \cdot \overline{U(f_1)}}, 2 \cdot \sqrt{U(-f_2) \cdot \overline{U(f_2)}} \dots \quad (13)$$

Figure 21 illustrates a set of HB data plots for the MESFET single stage test amplifier. These results are summarized in Table I.


```
.SUBCKT curtige_2 Source Drain Gate RG=1e-3 RD=1e-3 RS=1e-3
+ VBR=0 LG=0 LD=0 LS=0 IS=10e-15 N=1 XTI=0 EG=1.11
+ Beta=3e-3 Lambda=40e-3 VT0=-6 PTemp=27
+ Alpha=0.8 CDS=300e-15 TAU=10e-12 RIN=1m
+ CGS=300e-15 CGD=300e-15 Vbi=1.0 PTnom=27
.PARAM PGMIN=1e-12
.PARAM TK={PTemp+273.15}
.PARAM TnK={PTnom+273.15}
.PARAM PVt={1.38065e-23/1.6021765e-19*TK}
.PARAM TR={TK/TnK}
.PARAM IsT={IS*exp(XTI/N*ln(TR)-EG/N/PVt*(1-TR))}
RIN n6 n7 {RIN}
Rd n1 n2 {RG}
Ld Gate n1 {LG}
Lg n3 Drain {LD}
Rg n4 n3 {RD}
Rs n8 n6 {RS}
Ls Source n8 {LS}
R1 n6 n5 1M
BD2I0 n4 n2 I=0
GD2Q0 n4 n2 nD2Q0 n2 1.0
LD2Q0 nD2Q0 n2 1.0
BD2Q0 nD2Q0 n2 I=-((CGD*(V(n4)-V(n2)))
BD1I0 n4 n5 I=stp((V(n2)-V(n6))-VT0>0)*stp((V(n4)-V(n5))>=0)*
+ (Beta*((V(n2)-V(n6))-VT0)**2)*
+ (1+Lambda*(V(n4)-V(n5)))*tanh(Alpha*(V(n4)-V(n5))))+
+ stp(-(V(n2)-V(n6))+VT0>0)*
+ stp(-(V(n4)-V(n5))>=0)*(-Beta*((V(n2)-V(n6))-VT0)**2)*
+ (1-Lambda*(V(n4)-V(n5)))*tanh(-Alpha*(V(n4)-V(n5))))
GD1Q0 n4 n5 nD1Q0 n5 1.0
LD1Q0 nD1Q0 n5 1.0
BD1Q0 nD1Q0 n5 I=-((CDS*(V(n4)-V(n5)))+
+ (TAU*(V(n5)-V(n6))*1e3))
BD1I1 n5 n6 I=0
BD1I2 n2 n6 I=stp((V(n2)-V(n6))>Vbi)*
+ (IsT*(exp((V(n2)-V(n6))/(N*PVt)-1.0)))+
+ PGMIN*(V(n2)-V(n6))+
+ stp(-(V(n2)-V(n6))>Vbi)*(-IsT+PGMIN*(V(n2)-V(n6)))
BD1I3 n2 n7 I=0
GD1Q3 n2 n7 nD1Q3 n7 1.0
LD1Q3 nD1Q3 n7 1.0
BD1Q3 nD1Q3 n7 I=-((CGS*(V(n2)-V(n7)))
.ENDS
```

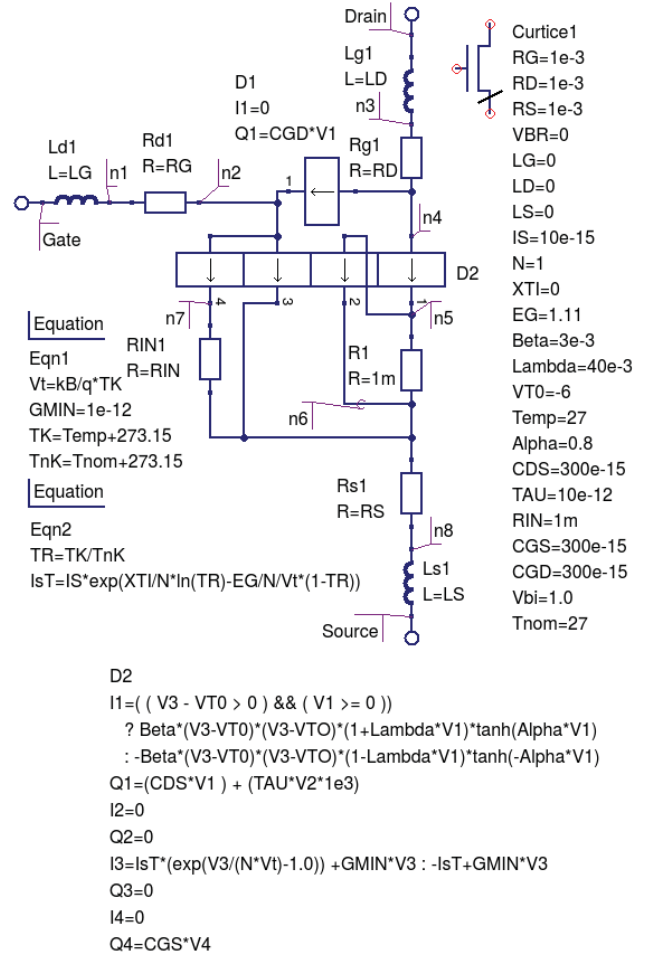


Fig. 18. Auto-generated Xyce SPICE netlist for the Curtige level 1 MESFET model. For clarity long text lines are shown on more than one line.

Fig. 19. Curtige level 1 Xyce MESFET EDD macromodel: model body, component symbol and device parameter list. Qucs EDD diode current I1 selected with function step(). For clarity D2 is displayed on more than one line.

TABLE I
HB SIMULATION DATA FOR THE SINGLE STAGE MESFET AMPLIFIER GIVEN IN FIGURE 21

Node Pc	Qucs			Xyce		
	H_0	H_1	H_2	H_0	H_1	H_2
Volts	7.81624	3.59243	0.07711	7.82522	3.58553	0.07720
% Diff.				+0.115	-0.192	+0.1297

IX. CONCLUSIONS

Harmonic Balance simulation of RF circuits is rarely implemented in GPL circuit simulators derived from Berkeley SPICE 2g6 or 3f5 [14], [15]. Currently, Qucs includes single tone HB simulation. This paper introduces a compact macromodeling approach to Qucs HB simulation which is suitable for simulating RF discrete and integrated circuit steady state AC performance. The proposed modeling technique introduces a compact macromodeling structure which reduces HB linear and non-linear circuit partitioning problems and helps reduce the effects of discontinuities in model current and charge differential characteristics on HB solution convergence. Experience with the proposed Qucs HB compact macromodeling method has shown that it is suitable for any general purpose circuit simulator provided it implements HB simulation and

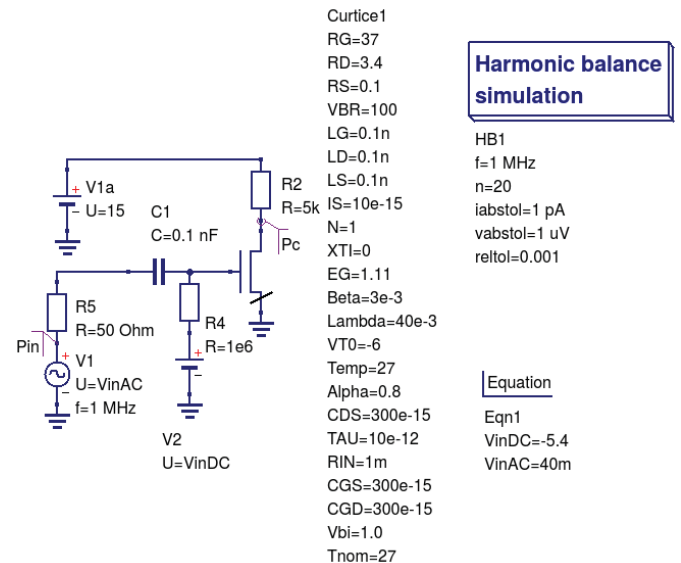


Fig. 20. The Qucs and Xyce single stage MESFET amplifier test bench.

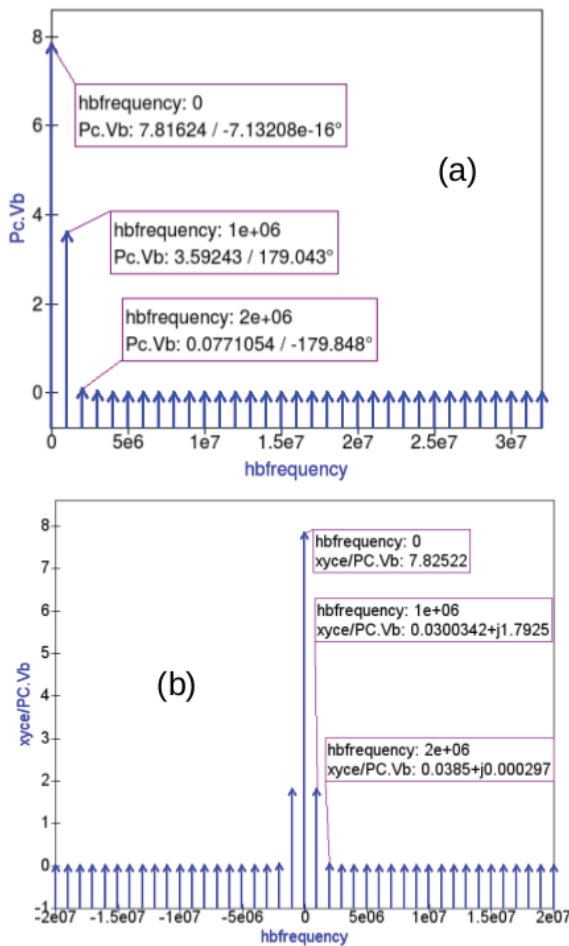


Fig. 21. Qucs and Xyce single stage MESFET amplifier HB simulation data: (a) Qucs node Pc spectral voltage amplitude plot against frequency and (b) Xyce node Pc spectral complex voltage plot against frequency.

can handle Equation-Defined Devices or Verilog-A analogue modules. HB simulation data for a semiconductor diode, an npn BJT and a MESFET are reported. This data was obtained from test simulations using both the Qucs and Xyce GPL simulators. Good agreement was found between the steady state AC simulation results obtained from Qucs HB simulation and transient time domain simulation and between Qucs and Xyce single tone HB simulation.

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Mike Brinson received a first class honours BSc degree in the Physics and Technology of Electronics from the United Kingdom Council for National Academic Awards in 1965, and a PhD in Solid State Physics from London University in 1968. Since 1968 Dr. Brinson has held academic posts in Electronics and Computer Science. From 1997 till 2000 he was a visiting Professor of Analogue Microelectronics at Hochschule, Bremen, Germany. Currently, he is a visiting Professor at the Centre for Communication Technology Research, London Metropolitan University, UK. He is a Chartered Engineer (CEng) and a Fellow of the Institution of Engineering and Technology (FIET), a Chartered Physicist (CPhys), and a member of the Institute of Physics (MInstP). Prof. Brinson joined the Qucs project development team in 2006, specializing in device and circuit modeling, testing and document preparation.



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