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SIMULATION OF HIGH-EFFICIENCY INTERLEAVED STEP-UP DC-DC BOOST-FLYBACK CONVERTER TO USE IN PHOTOVOLTAIC SYSTEM

In low-voltage photovoltaic (PV) systems high-efficiency high voltage gain step-up DC-DC converters are required as the interface between the PV panel and the load. Therefore overall performance of the PV system is essentially affected by the efficiency of step-up DC-DC converter itself. This paper presents the results of PSpice simulation of high-efficiency interleaved step-up DC-DC converter. The converter integrates boost and flyback topologies. Interleaved approach minimizes the current stress on the switches as well as allows reducing a sizes of the inductors but also decreases input current ripples. The other advantage of interleaving structure is flexibility of number of working phases extension. The number of working phases can be dynamically determined depending on the power requirements of the load. High efficiency assured by boost-flyback topology is achieved by the means of recycling the energy from input leakage inductance and relatively low voltage stress across the transistor switches which enables low drain-to-source resistance transistors application. The simulation carried out will present transient and performance characteristics of interleaved step-up DC-DC boost-flyback converter.

KEYWORDS: Step-up DC-DC Converters, High Efficiency, Photovoltaic Systems

1. INTRODUCTION

The PV panel comprising PV modules connected in parallel delivers the power at the voltage range of 20 V_{DC} to 50 V_{DC} (V_i) depending on PV module type. Step-up DC-DC converter is the next stage in a PV system. Simplified renewable energy system is shown in Fig. 1.

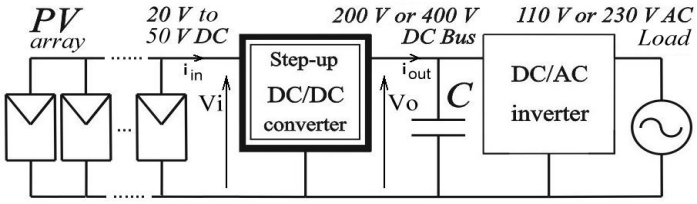

Fig. 1. Simplified low-voltage PV energy system diagram

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The role of the converter is to step up its input voltage to the level accepted by DC-AC inverters which is around 200 V_{DC} or 400 V_{DC} depending on the grid standards[1]. The other goal is to achieve highest energy conversion efficiency possible [2]. In this paper the performance of three-phase boost-flyback topology of interleaved step-up DC-DC converter with coupled inductors will be characterized basing on PSpice computer simulations.

2. INTERLEAVED STEP-UP BOOST-FLYBACK DC-DC CONVERTER WITH COUPLED INDUCTORS TOPOLOGY

Step-up DC-DC converter input current is shared between a number of phases allowing reduction of inductor and semiconductor peak currents which benefits with overall power loss reduction [3]. The other advantages of an interleaved topology are possibility to use smaller and cheaper passive components, applying lower power rating semiconductor components as well as efficient input and output current ripples rejection [4].

2.1. Electrical Scheme

Single phase of boost-flyback step-up DC-DC converter is shown in Fig. 2. It is derived from boost (S_1, L_{T1}, D_{11} and C_1) topology associated with flyback converter (S_1, L_{T1}, L_{T2}, D_1 and C_0-C_1) [5]. The converter proposed here consists of 3 phases connected in parallel.

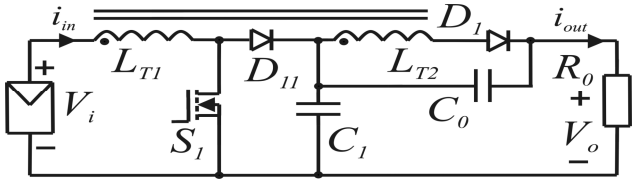

Fig. 2. Single phase of interleaved boost-flyback step-up DC-DC converter

In proposed topology the leakage energy from primary inductance L_{T1} is directly recycled through input diode D_{11} at transistor turn off transient preventing voltage overshoots at transistor S_1 drain. V_i represents low voltage PV array and R_0 is a load resistance of PV system DC-bus.

2.2. Principle of operation

There are three modes of operation in one switching cycle (T) of interleaved step-up DC-DC converter with assumption of continuous conduction mode. The model presented here does not include any parasitic parameters such as leakage inductances (i.e. ideal coupling between L_{T1} and L_{T2}), winding resistances and

capacitor's ESRs. Moreover neglected are transistor's on resistances and diode voltage drops. Fig. 3 explains the work of 3-phase converter where gate driving signals of transistors S_1, S_2 and S_3 are switched at duty cycle of D = 66.6% and phase shifted by $2\pi/3$ electrical angle (Fig. 3a, 3b and 3c).

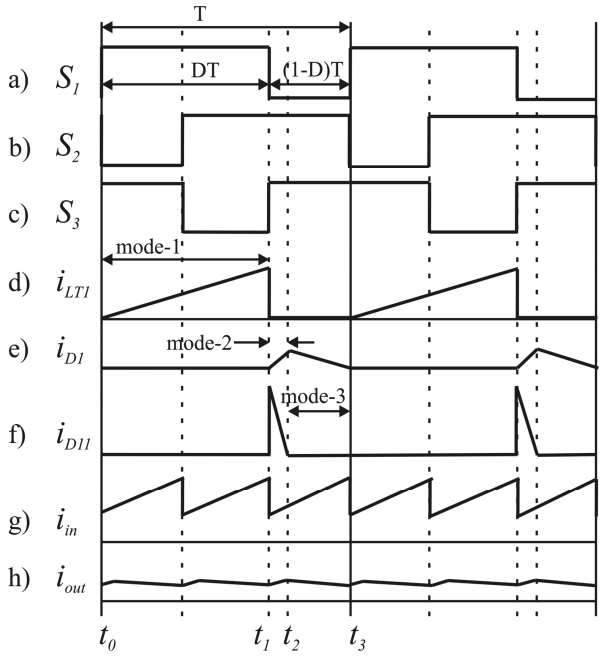

Fig. 3. Key waveforms of interleaved step-up DC-DC converter during operation modes 1 to 3

At the example of single phase in mode-1 when transistor S_1 is switched on and output rectifier D_1 is reverse-biased the energy is transferred from the input to primary inductance L_{T1}.

The capacitor C_1 is charged through forward forward-biased primary rectifier diode D_{11} in mode-2.

In mode-3 when D_{11} current reaches zero and transistor S_1 is turned off and the output diode D_1 is on capacitor C_0 is charged through output rectifier diode D_1.

Aggregate output current (i_0) (Fig. 3h) is composed of each individual phase currents and is further filtered by C_0.

In steady state the voltage gain of boost converter itself is:

$$\frac{V_0}{V_{i\ |boost}} = \frac{1}{1-D} \tag{1}$$

whereas the voltage gain of overall boost-flyback converter is:

$$\frac{V_0}{V_{i\ |boost-flyback}} = 1 + \frac{D(1+N)}{1-D} \tag{2}$$

3. PSPICE SIMULATION MODEL OF INTERLEAVED BOOST-FLYBACK STEP-UP DC-DC CONVERTER WITH COUPLED INDUCTORS

Fig. 4 presents PSpice model of n = 3-phase boost-flyback interleaved step-up DC-DC converter. Fast power MOSFET transistors (IRFP4568, R_{DSon_typ} = 4.8 mΩ, V_{DS_max} = 150 V) are driven by phase shifted square waves generated by V_{gk} voltage sources (k = 1,2,...,n). Gate driving circuit comprises C_{gk} (10 nF), D_{gk} and R_{gk} (10 Ω) chosen to optimize turn-off time of the transistors. The switching frequency f_S is 20 kHz.

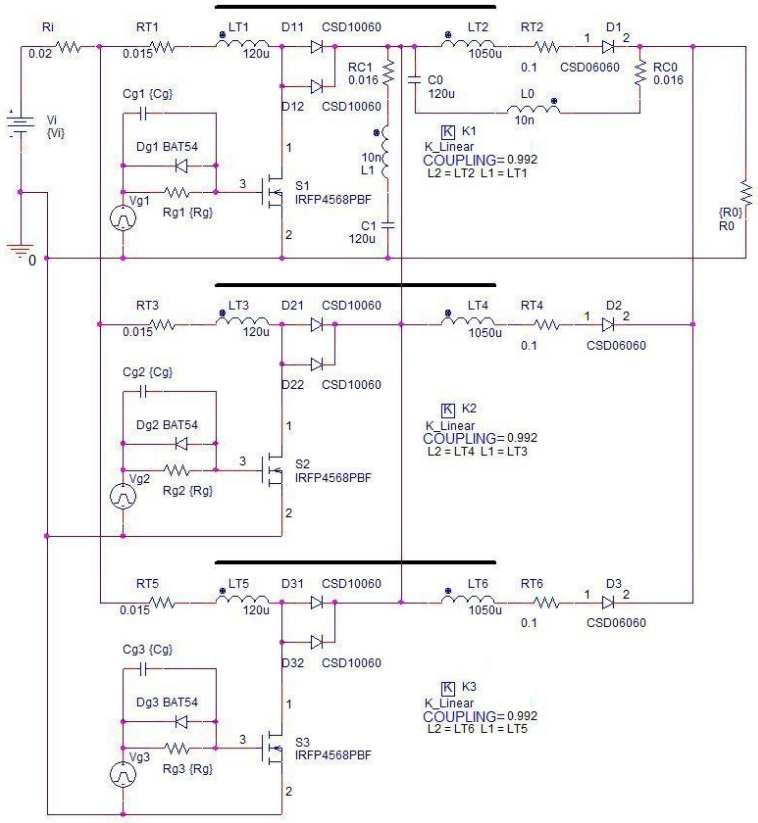

Fig. 4. Pspice model of 3-phase boost-flyback interleaved step-up DC-DC converter

The Silicon Carbide (SiC) diodes can be paralleled as they do not suffer with thermal runaway effect. The output diodes D_{11} to D_{32} (two diodes CSD12060 for the purpose of simulation, instead of dual device in one package) and input diodes D_1 to D_3 (CSD06060) are 600 V rated.

In the simulation the parasitic components such as $R_{C0,}$ R_{C1} and $L_{0,}$ L_1 representing real capacitor parasitic resistances and inductances respectively are considered.

L_{T1} together with L_{T2} are primary and secondary windings of coupled inductor together with R_{L1k} and R_{L2k} which are primary and secondary winding resistances create a model of the coupled inductors with turns ratio of $N = 3$ and inductance coupling coefficient $K = 0.992$.

4. TRANSIENT CHARACTERISTICS

Fig. 5 presents simulation waveforms of 3-phase interleaved boost-flyback step-up DC-DC converter. For given conditions the voltage gain is 10.3 producing output voltage V_0 of 413 V. Fig 5a) shows the voltage at anode of D_1 and output voltage V_0. Fig. 5b) depicts transistors S_1 drain to source voltage effectively clamped to 133 V according to (1). Input and output currents together with the currents of single phase transistor and input and output rectifiers are depicted on (Fig. 5c). The influence of parasitic parameters can be seen on transient plots as output rectifier diode voltage ringing at transistor turn-off and slanted slopes of transistor voltage caused by input leakage inductance.

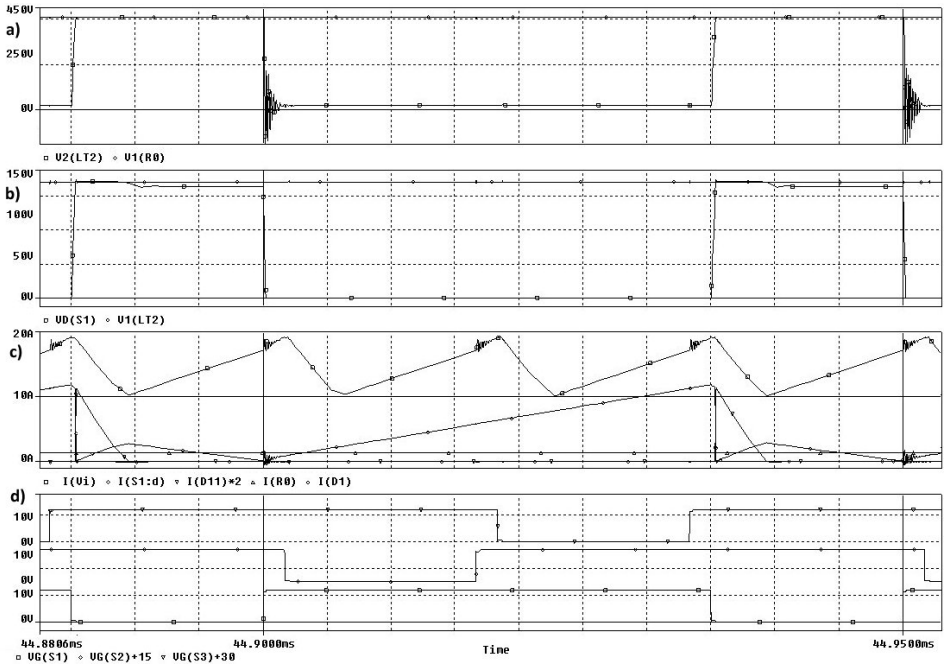

Fig. 5. Transient waveforms of key boost-flyback DC-DC converter currents and node voltages at $f_S = 20$ kHz, $V_{in} = 40$ V, $D = 0.7$ and load resistance $R_0 = 300\ \Omega$

5. PARAMETRIC CHARACTERISTICS

Parametric characteristics present the dependency of interleaved step-up DC-DC converter parameters on duty cycle D and output resistance R_0 variations. Simulation was carried out at following conditions: input voltage V_i = 40 V and switching frequency f_S = 20 kHz. Load resistance was changed within the range R_0 = 65 Ω to 1000 Ω, and duty cycle D within 60% up to 80%.

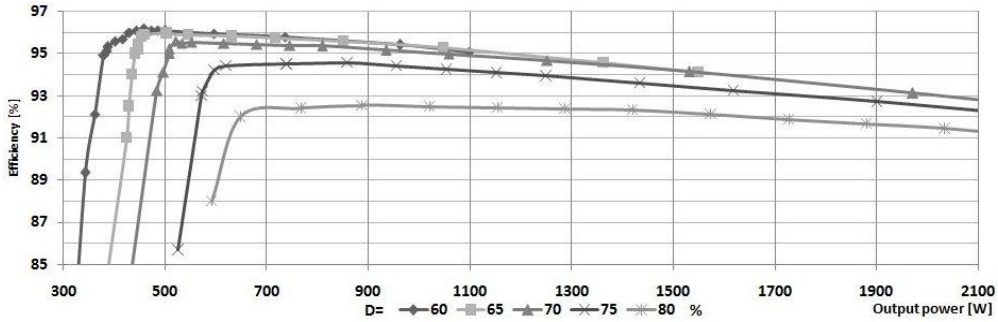

Fig. 6. Parametric characteristics of efficiency η vs. duty cycle D

Fig. 6 shows that efficiency over 92% can be achieved within wide output power the range for lower duty cycle values (except of 80%). The efficiency gets higher as duty cycle decrease. It is caused by lower power losses at input stage (i.e. boost converter) when high current flows through primary windings and through transistor during DT period (Fig. 3). On the other hand in order to produce high enough voltage level at the output it is necessary to drive the converter with duty cycle higher than 65%, which according to (2) gives the voltage above 340 V at the output.

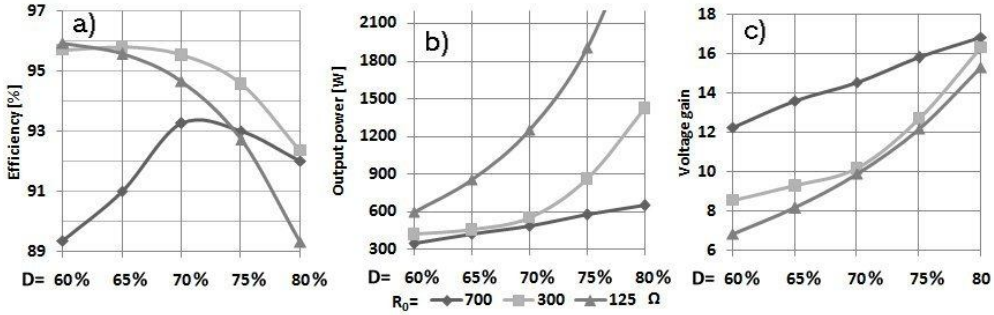

Fig. 7. Parametric characteristics of a) efficiency η, b) output voltage V_0, and b) voltage gain B vs. duty cycle D at three different load resistances R_0

For heavier loads (i.e. R_0 = 300 Ω and R_0 = 125 Ω) it is possible to achieve the efficiency above 92%, Fig. 7a) within examined duty cycle range. On Fig 7b) and 7c) it can be seen that the output power P_0 (and output voltage V_0) regulation is not linear except of light load (i.e. R_0 = 700 Ω) where it can be treated as linear one. Remarkable is that the voltage gain curves are different at three different load resistances. That is caused by parasitic component influences not considered in ideal formula (2).

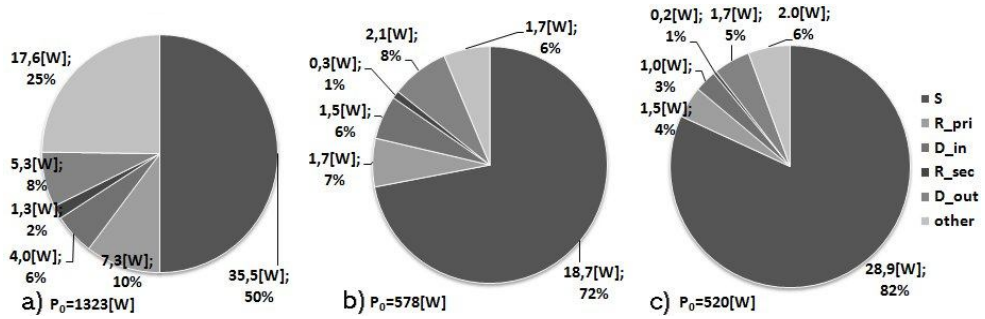

Fig. 8. Power loss budget of the converter at D = 70% and different load resistances a) R_0 = 125 Ω, b) R_0 = 300 Ω, c) R_0 = 700 Ω

Fig. 8 collates power losses of step-up boost-flyback DC-DC converter components at three different load resistances. R_pri and R_sec represent a sum of three inductor primary and secondary winding resistance power losses respectively, S is total power loss of transistors, D_in and D_out are the power losses in all input rectifiers and output rectifiers respectively. Other power losses represent wire resistance losses and transistor gate driving losses (Ri at Fig. 4). Transistor power losses are major component of total converter power loss budget.

6. CONCLUSION

PSpice computer based simulation tests confirmed high efficiency of interleaved step-up boost-flyback DC-DC converter with coupled inductors. Simulation results show that despite hard switching the converter demonstrate high efficiency within wide output power range. Therefore proposed topology can be effectively applied in low-voltage PV systems. However simulation results look consistent real laboratory measurement results may vary with respect to inaccuracies of whole converter model and individual component models.

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