ARCHIVES OF ELECTRICAL ENGINEERING VOL. 65(3), pp. 437-448 (2016)

DOI 10.1515/aee-2016-0032

Modeling and simulation of novel stepped DC coupled quasi Z-Multilevel Inverter for single phase systems

T. MEENAKSHI[1], N. SUTHANTHIRA VANITHA[2]

[1]*Department of EEE, Jansons Institute of Technology, Coimbatore, India*
[2]*Department of EEE, Knowledge Institute of Technology, Salem, India*
e-mail: mechand22@gmail.com

(Received: 31.08.2014, revised: 02.11.2015)

Abstract: This paper presents the modeling and simulation of a novel topology of quasi Z-Multilevel Inverter with stepped DC input. The proposed inverter incorporates a simple switching technique with reduced component count and is aimed at producing boosted multilevel output AC voltage. The inverter consists of two stages and the buck /boost operation is obtained by varying the shoot through period of the pulses obtained by maximum constant boost control with third harmonic injection. With all the advantages of the quasi Z-network, the proposed inverter eliminates the fly back diodes and capacitors present in a conventional Z-Multilevel Inverter. Further the stress on the devices is less which leads to reduction in component value and hence the cost. The novel stepped DC coupled Single Phase quasi Z-Multilevel Inverter is modeled and simulated in the MATLAB – SIMULINK environment and its performance is analyzed for varying input and switching conditions. The voltage and current waveforms across each stage of the inverter is analyzed and the results are presented for different levels of input.

Key words: multilevel inverter, shoot through, quasi Z-Source, modulation index

1. Introduction

Since its advent, the Z-Source Inverter [1] is gaining popularity among researchers because of its advantages like a single stage buck/boost operation, higher efficiency and inclusion of shoot through states in switching pulses. Continuous research is being performed on various areas of the Z-Source Inverter like topological changes, advancements in control schemes and promoting to different applications. Topological renovation is one area where fast developments are being encountered to improvise the performance from its predecessor and to reduce the stress on the device. The quasi Z-Source Inverter and Extended Boost quasi Z-Source Inverter are one of its types that reduce the stress on the *LC* component and have a high boost value which was described in [2-3]. The soft start capability is obtained by the Improved Z-Source Inverter which was proposed in [4]. Trans Z-Source Inverter is a modular structure that uses coupled inductors and center tapped capacitors for power conversion which was discussed in [5]. Reference [6] shows different types of *LC* combinations in the T-Source

Inverter and it also highlights the manipulation of output voltage for different transformer turns ratio. Frequency changes in the output voltage along with the buck-boost operation are brought by the Z-Source buck-boost matrix converter as given in [7]. Reference [8] discusses the topology to produce multilevel output with the Z-Source Inverter that used modified phase disposition pulse width modulation and modified phase shifted carrier scheme for pulse generation. The structure of the three phase neutral point clamped Multilevel Z-Inverter proposed in [9] is shown in Fig. 1.

It uses 12 switches, 6 fly back diodes and needs two Z-network or single Z-network depending on the type of the modulation technology. Further expanding the number of levels in the output voltage is difficult as far as this topology is concerned. The modulation scheme proposed for this inverter was modified phase disposition pulse width modulation and modified phase shifted carrier scheme which is more complicated than that used for the primitive Z-Inverter.

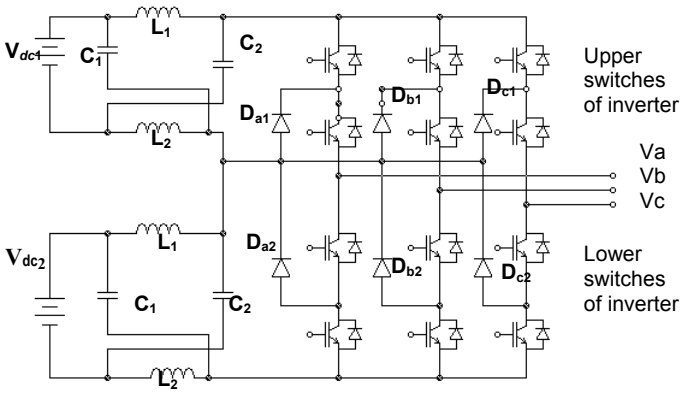

Fig. 1. Neutral point clamped Multilevel Z Source Inverter

To overcome the drawback of the NPC Multilevel Z-Inverter and to fill the gap of Z-Multilevel Inverters with expandable levels, the novel stepped DC coupled quasi Z-Multilevel Inverter (SDQZMLI) is devised. The SDQZMLI Inverter produces stepped DC voltage at the front end that is buck/boosted and inverted by the quasi Z-Inverter. The system uses the same control strategy that is used for Z-Source Inverter [10, 11] and could be used for isolated energy sources like PV, fuel cells and its applications as its primitive type [12, 14].The inverter system is simulated with different DC voltage sources in the MATLAB/Simulink environment and the discussion is made on various results obtained.

2. Modeling of the proposed Z-Multilevel Inverter

2.1. Structure of the proposed inverter

The Z-Source Inverter is an emerging area in the field of power electronics. Topological modifications are being carried out in this area to improvise its performance and to reduce the

losses. The proposed inverter is also another topological exploration of its type which produces boosted multilevel AC voltage that could be utilized for renewable energy sources. The structure of the proposed inverter is shown in Fig. 2.

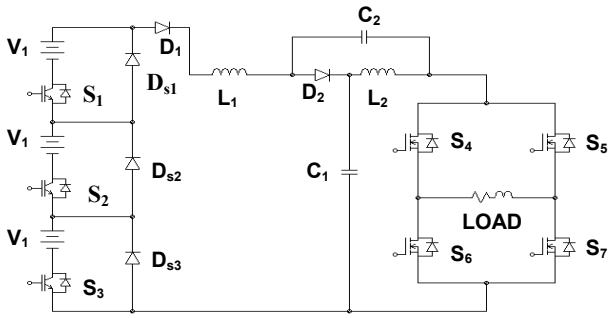

Fig. 2. Structure of proposed stepped DC link Z MLI

Multilevel DC link voltage can be produced with different circuit arrangements as given in [15] and this is one of its kinds. This configuration comprises a simple structure that utilizes isolated DC voltage sources connected through switches (S_1, S_2 and S_3) and bypass diodes (DS_1, DS_2 and DS_3) with quasi Z-Inverter. The switches of the DC link side are unidirectional and of low rating because they are subjected to low input voltage. The switching ON and OFF of the switches S_1, S_2, S_3 produces stepped DC link voltage (V_{sdc}). The number of levels of the DC link voltage is decided by the number of DC sources and switches used. This topology claims the advantage of using minimum number of switches for higher level in out-put voltage. The stepped DC link voltage appearing at the input is buck/boosted and inverted by the quasi Z-Inverter. The quasi network is a unique combination of *LC* elements (L_1, L_2, C_1, and C_2) and diodes D_1 which is a reverse current protection diode and D_2 which helps to build energy in Z components during shoot through state. The inverter switches has to withstand the high voltage stress caused due to the shoot through, hence their rating are comparatively higher than DC link switches. This setup aids the buck/boost operation and its advantage includes high boost factor and less stress on the components. Both buck and boost operation is obtained by controlling the shoot through period of the inverter. The firing pulses for the DC circuit is obtained by comparing triangular wave at fundamental frequency and a constant DC line at various levels, for the inverter the pulses are generated by maximum constant boost control with third harmonic injection scheme which is same as that used for traditional Z-Source Inverters [10]. This scheme is preferred as it maintains constant shoot through and produces high boost factor. It uses two reference signals V_a and V_b and two constant lines V_p and V_n. The carrier wave is a triangular wave switched at high frequency. Whenever the value of the reference signal exceeds the carrier wave and the constant line, firing pulse is generated. The high frequency switching of the SDQZMLI does not produce any interference with the DC link voltage that acts as input to the circuit. The inductor and capacitor requirements are to fulfil the energy storage and filtering action and the requirement is far less than that used in

voltage source inverter (capacitor) or current source inverter (inductor). The switching algorithm for firing pulse generation to produce V_{sdc} is given in the Table 1.

Table 1. Switching algorithm to produce stepped DC link voltage (V_{sdc})

Voltage level	Switches to be turned ON	Diode in conduction
0	nil	DS_1,DS_2,DS_3
V_1	S_3	DS_1,DS_2
$2V_1$	S_2,S_3	DS_1
$3\ V_1$	S_1,S_2,S_3	nil

The operating principle of the proposed stepped DC coupled quasi Z-Multilevel Inverter (SDQZMLI) is explained for shoot through and non-shoot through state with the Fig. 3(1) and 3(2).

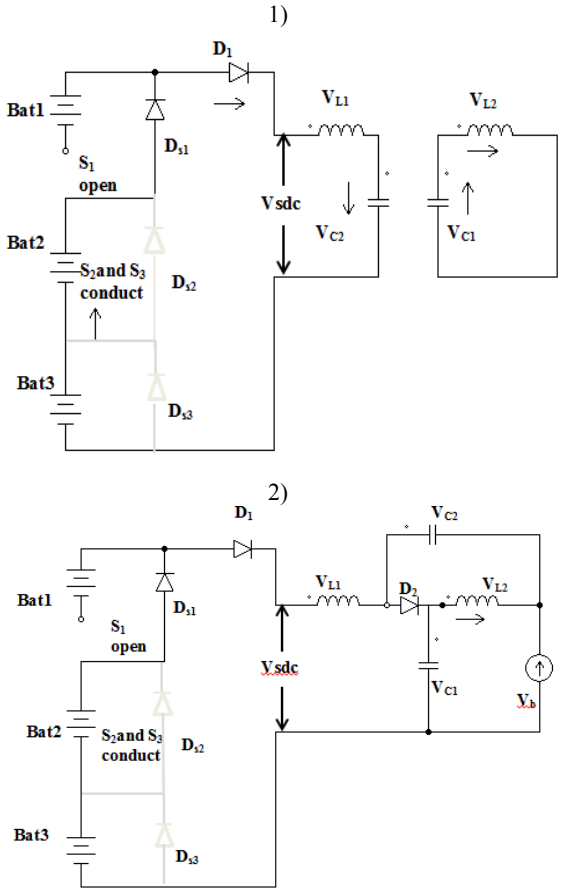

Fig. 3. Circuit operation of the proposed SDQZMLI inverter
1) shoot through state, 2) non-shoot through state

Fig. 3(1) shows the operation of the proposed SDQZMLI circuit during the shoot through state. The voltage 3*V*1 appears across the quasi Z-network where the legs of the inverter are shorted and the energy storage operation takes place in the Z components. During the non-shoot through state shown in Fig. 3(2), the sum of input voltage and that stored in Z-network appears as output. Both the inductance and the capacitance is taken identical in the Z-network for easier analysis. The shoot through state arises when switches of the same single leg are or of both the legs are shorted and produces a short circuit. During the non-shoot through state, the inverter acts as a current source when viewed from DC supply.

The same operation is carried out for different levels during shoot through states and non-shoot through states by following the switching scheme in Table 1. This operation could be extended for n levels in output voltage incorporating a simple revision in the proposed setup. The circuit arrangement to produce *n* level of boosted multilevel single phase AC voltage is shown in Fig. 4. It is noted that it requires only (*n*-1)/2 switches and diodes for stepped DC link voltage and 4 switches for inverter to produce *n* level single phase AC output voltage. Moving towards higher levels reduces the switch count drastically and the total harmonic distortion is considerably reduced in the waveform.

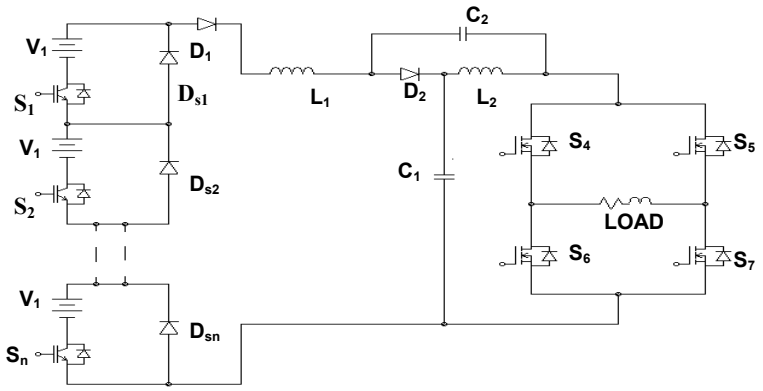

Fig. 4. Structure of proposed SDQZMLI for *n* level output

2.2. Modeling and circuit analysis

The system is modelled and the circuit analysis is carried out similar to as that of quasi Z-Inverter [2] and is extended for various levels. The following parameters are designated for the analysis; let the inductor voltage be V_{L1} and V_{L2} and capacitor voltage is V_{C1} and V_{C2}. The input DC voltage obtained from the isolated energy system is represented as V_1. The stepped DC voltage available to the Z-network is V_{sdc}. The boosted voltage across the Z-network is V_b and the inverter voltage of SDQZMLI is V_{ac}. The voltage equations of the inductor and capacitor and the AC output voltage available at the output of the inverter is given by the expressions (1) to (13)

During the shoot through state of level 1 of V_{sdc}, the inductor voltages are given as,

$$V_{L1} = V_1 + V_{C2} \quad \text{and} \quad V_{L2} = V_{C1}. \tag{1}$$

During the non-shoot through state of level 1 of V_{sdc},

$$V_{L1} = V_1 - V_{C2} \quad \text{and} \quad V_{L2} = V_{C1} - V_{sdc} \ , \tag{2}$$

$$V_{L2} + V_{C2} = 0 \, , \tag{3}$$

$$V_{L2} = -V_{C2} \, . \tag{4}$$

The average voltage in an inductor is zero. T_0 is taken as the time period of shoot through state and T_1 is the time period of non-shoot through state. The sum of T_0 and T_1 is the switching period T. Hence

$$V_{L1} = \frac{T_0(V_1 + V_{C2}) + T(V_1 + V_{C1})}{T} = 0 \, , \tag{5}$$

$$V_{L2} = \frac{T_0(V_{C1}) + T_1(-V_{C2})}{T} = 0 \, . \tag{6}$$

On simplification

$$V_{C1} = \frac{T_1}{T_1 - T_0} V_1 \quad \text{and} \quad V_{C2} = \frac{T_0}{T_1 - T_0} V_1 \, . \tag{7}$$

The expression of V_{sdc} from Eq. (2) is given as,

$$V_{sdc} = V_{C1} + V_{C2} = \frac{1}{1 - 2\frac{T_0}{T}} V_1 = BV_1 \, , \tag{8}$$

where B is the value by which the input voltage is boosted.

The same analysis is carried for different levels of V_{sdc}. For step 2.

During the shoot through state

$$V_{L1} = 2V_1 + V_{C2} \quad \text{and} \quad V_{L2} = V_{C1} \, . \tag{9}$$

During the non-shoot through state

$$V_{L1} = 2V_1 - V_{C1} \quad \text{and} \quad V_{L2} = V_{C1} - V_{sdc} \, , \tag{10}$$

$$V_{sdc} = V_{C1} + V_{C2} = \frac{1}{1 - \frac{2T_0}{T}} 2V_1 = 2BV_1 \, . \tag{11}$$

Similarly for n steps, the stepped DC voltage will be boosted by nBV_1. The boosted multilevel AC voltage available at the inverter is given by (12)

$$V_{ac} = M \frac{V_{sdc}}{2} = M \frac{BV_1}{2} \, . \tag{12}$$

The voltage gain (G) of the system is given as

$$G = \frac{V_{oc}}{V_1/2} = MB = \frac{M}{\sqrt{3}M - 1} \quad \text{where} \quad (B = \frac{1}{\sqrt{3}M - 1}). \tag{13}$$

3. Simulation and discussion

Simulations have been performed in MATLAB/ Simulink environment to demonstrate the working of the proposed SDQZMLI Inverter. The system under simulation is aimed to produce 7 level in the output and it uses 3 DC sources of 50 V each. The configuration shown in Fig. 1 is simulated with the following circuit parameters; the front end circuit producing V_{sdc} is switched at fundamental frequency. The inductor and capacitor values of the LC network is $L_1 = L_2 = 800$ µH and $C_1 = C_2 = 1$ µF. The system is designed to produce a multilevel AC voltage of 220 V rms at fundamental frequency. The switching frequency of the inverter is 10 kHz.

The waveforms depict the simulation results at various stages of the inverter. Fig. 5 shows the stepped DC voltage (V_{sdc}) obtained from the proposed inverter. The 7 steps of voltage levels are obtained by following the switching algorithm in Table 1.

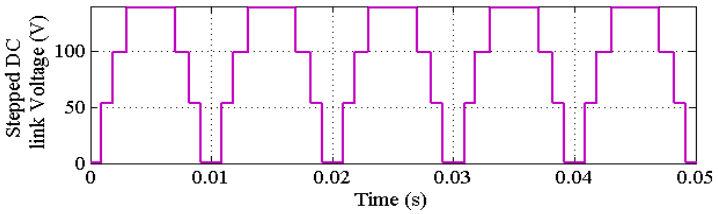

Fig. 5. Simulation result of stepped DC voltage (*Vsdc*)

This stepped DC voltage appears as DC link voltage to the quasi Z-Inverter. The firing pulse for the Z-Inverter is generated by maximum constant boost control with third harmonic injection. Simulation of the system is performed for a modulation index of 0.7, the reference lines V_p and V_n is taken as 0.62 (both positive and negative values). This difference in value is due to third harmonic injected in the reference value. By this high boost value is obtained even for high modulation index. The simulated reference waveforms of maximum constant boost control with third harmonic injection are shown in Fig. 6.

Figs. 7-9 shows the simulated waveforms of inductor current, capacitor voltage and inverter output voltage V_{ac} of the inverter. The inductor current peaks to a value of 12 A, Capacitor voltage is 300 V peak. This shows that the stress on the device is reduced compared to traditional ZSI. The DC link voltage is boosted and flipped by the inverter, the waveform reveals that it is boosted to a value of 400 V peak consisting of 7 levels.

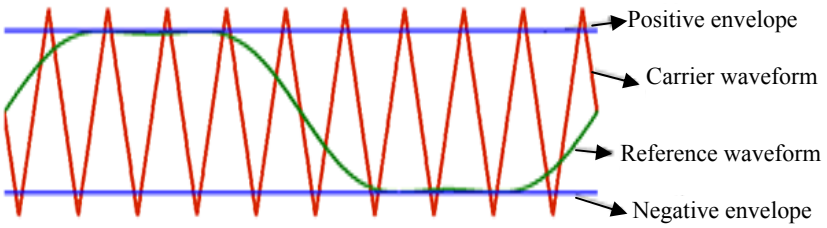

Fig. 6. Simulated reference waveforms for SDQZMLI

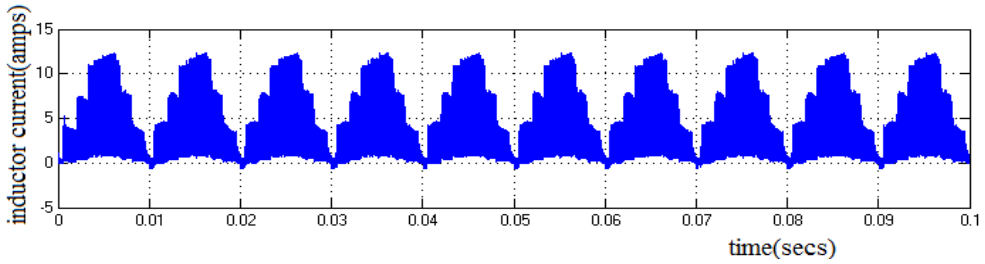

Fig. 7. Simulated waveform of Inductor current, modulation index = 0.7

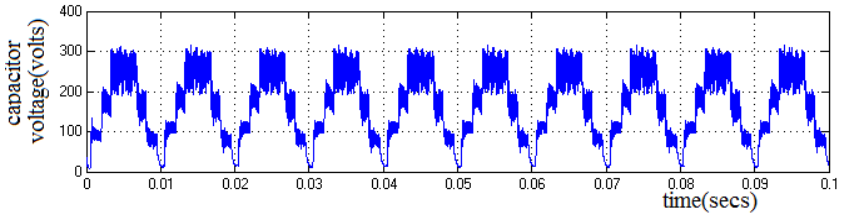

Fig. 8. Simulated capacitor voltage, modulation index = 0.7

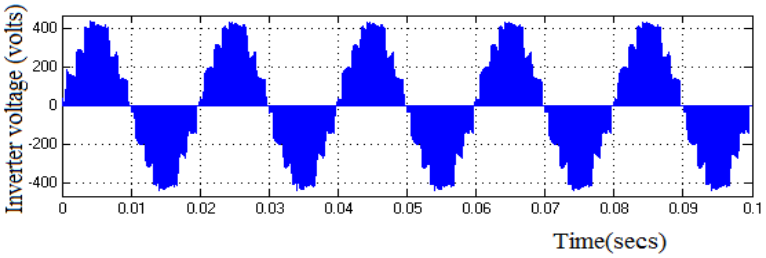

Fig. 9. Simulated multilevel AC voltage for modulation index of 0.7

Fig. 10 depicts the input current and the load current obtained by simulation for the same system. The input current drawn from the supply is 6 A and the load current is 1.85 A for a RL load of impedance 100 Ω.

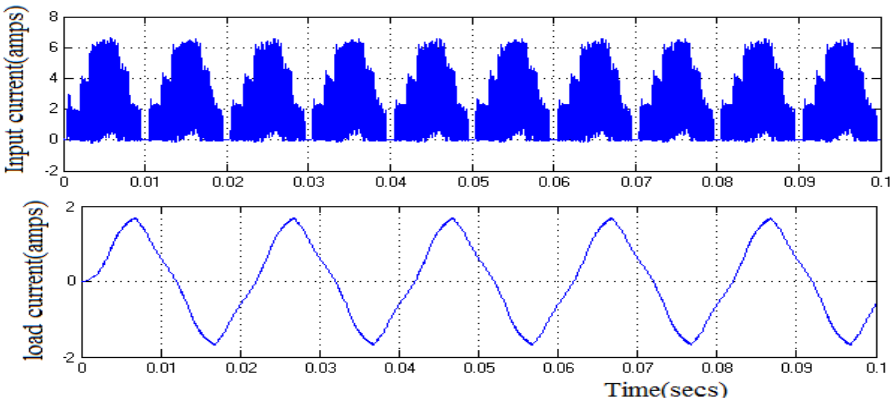

Fig. 10. Simulated current waveforms

To demonstrate the working of the inverter with higher levels in the output voltage, simulations were performed for 11 level of the proposed SDQZMLI Inverter. The simulated waveforms of boosted voltage of Z-network (V_b) and inverter voltage (V_{ac}) are shown in the Figure 11. This is performed for a modulation index of 0.7. The 500 V input is boosted to value of 1223 V peak.

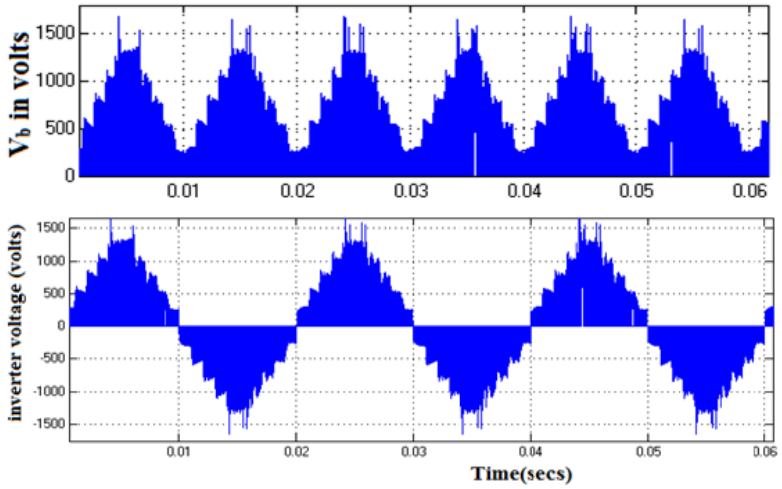

Fig. 11. Simulated waveform of 11 level proposed SDQZMLI Inverter

The variation of the output voltage of the SDQZMLI Inverter for different shoot through periods is given in Table 2.

It is seen that the shoot through increases with the decrease in modulation index and both buck and boost operation is obtained by varying the shoot through period.

A comparative evaluation is performed between SDQZMLI and quasi Z-Source Inverter based on the voltage total harmonic distortion and efficiency which is depicted in Fig. 12(1) and 12(2).

Table 2. Variation of output voltage for different shoot through period and modulation index, V_1 = 100 V with 3 isolated DC source

Modulation index	Shoot through period	Output voltage (fundamental) (volts)
0.7	0.0165 ms	437 V
0.75	0.0126 ms	380 V
0.8	0.001 ms	336 V
0.85	0.00076 ms	292 V
0.9	0.0005 ms	256 V

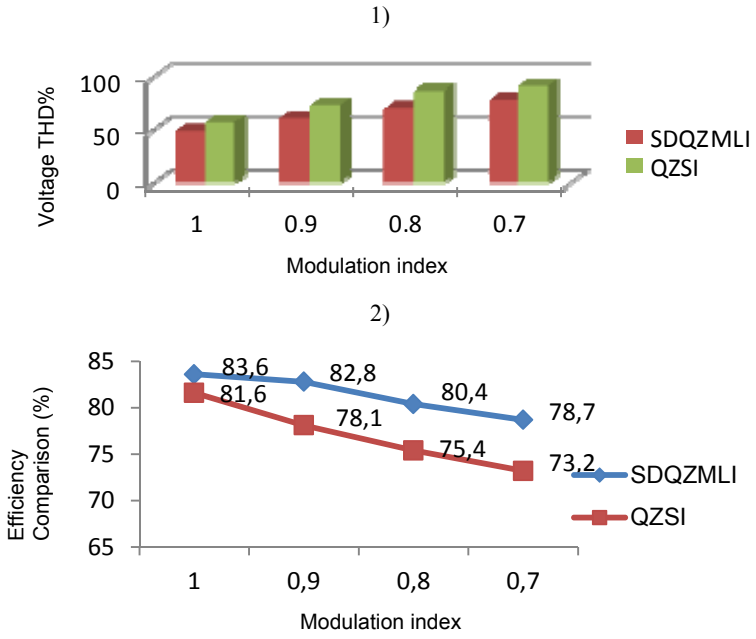

Fig. 12. Performance comparison. 1) voltage THD, 2) efficiency comparison

It is seen that the proposed SDQZMLI has comparatively lower voltage harmonic distortion compared to QZSI. This is due to the stepped nature of the output voltage that reduces the harmonic content. The efficiency of the proposed inverter is higher because of the reduced stress on the devices that reduces the losses in the energy storage elements.

Table 3 depicts a comparative study between the conventional Single phase ZMLI and the proposed SDQZMLI Inverter for a 5 level stepped voltage.

It is comprehended that the proposed inverter uses simple switching technique compared to neutral point clamped ZMLI and further the number of Z-network and switches are reduced in the proposed inverter for the same output. The DC link voltage is stepped in the proposed type whereas it is constant in its counterpart. On performing a study on the simulation results it is found that the third harmonic is found to be dominant in the single phase system. Hence

selective harmonic suppression has to be implemented to reduce the effect of third harmonics in the output voltage.

Table 3. Comparison of single phase ZMLI and proposed SDQZMLI Inverter for a 5 level system

Performance feature	**Neutral point clamped Z-source MLI**	**Proposed SDQZMLI inverter**
No of switches	8	6
No of clamping diodes	6	2(parallel diodes)
PWM scheme	Phase disposition	All control schemes applicable for traditional Z-Inverter
DC link voltage	Constant	Multi-step
No of Z networks	2	1

The hardware experimentation was carried for a five level SDQZMLI. The hardware setup and the output voltage is given in Fig. 13.

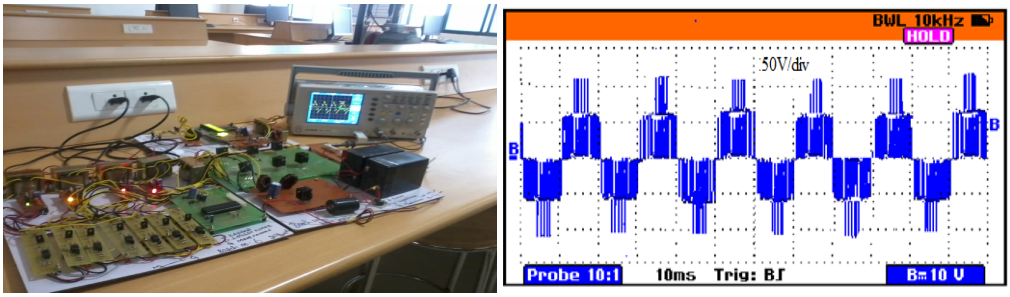

Fig. 13. 1-Hardware implementation, 2-5 level output voltage obtained from hardware

4. Conclusions

This paper has presented the theoretical analysis, modeling and simulation of new topology of Z-Multilevel Inverter which achieves buck/boosted multilevel AC operation through two stage conversion process. The analysis confirms that it uses less number of switches and single *LC* combination to produce the same output voltage as its counterpart. Moreover the stress on the *LC* components is much reduced thus lowering the voltage rating of the components. This inverter can be extended to n levels by appending circuit components in the front end. The harmonics realized in the simulation results can be reduced by introducing harmonic suppressors.

References

[1] Peng F.Z., *Z-source inverter*, IEEE Transactions on Industrial Applications (39): 504-510 (2003).
[2] Li Y., Anderson J., Peng F.Z., Liu D., *Quasi-z-source inverter for photovoltaic power generation systems*, Proceeding of Applied Power Electronics Conference and Exposition, pp. 918-924 (2009).

[3] Gajanayake C.J., Fang L.L., Hoay B.G., et al., *Extended boost Z-source inverters*, IEEE Transactions on Power Electronics (25): 2642-2652 (2010).
[4] Yu T., Shaojun X., Chaohua Z., and Zegang X., *Improved Z-Source Inverter With Reduced Z-Source Capacitor Voltage Stress and Soft-Start Capability*, IEEE Transactions on Power Electronics (24):409-415 (2009).
[5] Qian W., Peng F.Z., Cha H., *TransZsource inverters*, in Proceedings of Power Electronics Conference pp. 1874-1881 (2010).
[6] Das A., Lahiri D., Goswami A.K., *A New Inverter Topology for Adjustable Speed Drive Systems,* Proceeding of International Conference on Control, Communication and Power Engineering pp. 162-164 (2010).
[7] Nguyen M.K., Jung Y.G., Lim Y.C., Kim Y.M., *A Single-Phase Z- Source Buck-Boost Matrix Converter*, IEEE Transactions on Power Electronics (25): 453-462 (2010).
[8] Loh P.C., Lim S.W., Gao F., Blaabjerg F., *Three-level Z-source inverters using a single LC impedance network,* IEEE Transactions on Power Electronics (22):706-711 (2007).
[9] Loh P.C., Blaabjerg F., Feng S.Y., Soon K.N., *Pulse-width modulated Z-source neutral-point-clamped inverter*, IEEE Transactions on Industrial Applications (43):1295-1308 (2007).
[10] Peng F.Z., Shen M., Qian Z., *Maximum boost control of the Z-source inverter*, IEEE Transactions on Power Electronics (20): 833-838 (2005).
[11] Shen M., Wang J., Joseph A., Peng F.Z., Tolbert L.M., Adams D.J., *Constant Boost control of the Z-source inverter to minimize current ripple and voltage stress*, IEEE Transactions on Industrial Applications (42): 770-777 (2006).
[12] Peng F.Z., Shen M., Holland K., *Application of Zsource inverter for traction drive of fuel cell-battery hybrid electric vehicles,* IEEE Transactions on Power Electronics (22):10541061 (2007).
[13] Huang Y., Shen M., Peng F.Z., *A Z-source inverter for residential photovoltaic systems*, IEEE Transactions on Power Electronics (21): 1776-1782 (2006).
[14] Peng F.Z., Joseph A., Wang J., Shen M., Chen L., Pan Z., Rivera E.O., Huang Y., *Z-source inverter for motor drives*, IEEE Transactions on Power Electronics (20): 857-863 (2005).
[15] Su G.J, *Multilevel DC-Link Inverter*, IEEE Transactions on Industrial Applications (41): 848-854 (2005).