A Low-Jitter, Full-Differential PLL in 0.18μm CMOS Technology

Farzad Modarresi, Mehdi Ghasemzadeh, Mahsa Mazlumi,
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***Abstract*—This paper presents a Phase Locked Loop (PLL) which works with minimum jitter in the operation frequency range of 600MHZ to 900MHZ. Utilizing a full differential architecture that consists of several blocks of differential VCO, a differential PFD and a differential CPL leads to limiting the RMS jitter to 4.06ps, with 50mV power supply noise in the frequency range of 750MHz. Simulation results using 0.18μm CMOS TSMC standard technology demonstrate the power-consumption of 4.6mW at the supply voltage of 1.8V.**

***Index Terms*—full differential PLL, PFD, VCO, low jitter, CPL**

I. Introduction

PHASE-LOCKED loops (PLL) are the essential building blocks in high-performance applications such as: wireless or wire-line digital communication systems, where the clock frequencies are extremely needed. Therefore the performance of the PLLs is a most important issue in the mentioned applications that all designers have to put it in the center of attention.

The most common applications of PLLs are in the clock generators and frequency synthesizers [1-3]. A phase locked loop (PLL) is a negative feedback, closed loop system that compares and locks the phase of its output signal to an input reference signal. Usually a typical PLL consists of several main blocks as: phase-frequency detector (PFD), charge pump (CP), low-pass filter (LPF), voltage controlled oscillator (VCO) and a divider [4-5]. The comparison between the phase and the frequency of the reference signal with the phase and the frequency of the feedback signal can be performed by PFD. The phase-frequency detector produces an error signal which is proportional to the phase difference between its applied inputs [6]. Charge pump and the low-pass filter are the components of the CPL block which employed to improve the acquisition range of the PLL [3]. The output voltage of the low-pass filter is fed to the VCO to generate a proportional output signal. Finally, oscillation frequency divided into feedback clock, utilizing the frequency divider block [9-10].

In this work, applying new structures for voltage controlled oscillator (VCO) and charge pump (CP) leads to a high performance PLL which is described in the next section.

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The block diagram of a typical PLL is depicted in fig. 1.

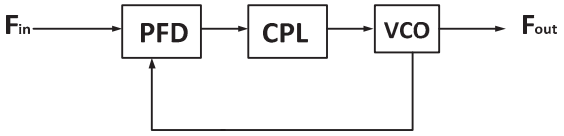

Fig. 1. The block diagram of PLL

Rest of the paper is organized in four sections. The next section includes a comprehensive discussion about the proposed PLL architecture and operation its blocks, respectively. Section. III shows the simulation results and also compares the proposed structure with some similar approaches. Finally, conclusion is given at Section. IV.

I. Proposed Structure

In this section, different building blocks of the proposed structure are described one by one.

A. Phase-Frequency Detector (PFD)

Fig. 2 shows the proposed PFD which is designed completely in symmetrical situation. The devices (M1-M4) are employed to detect the difference of the phase and frequency between the negative input (in-) and the output of the oscillator (in+). The comparison results will be held by the M5 and M6 devices and also for return the PFD circuit to its ordinary situation and starting the next comparison cycle, the devices M7 to M10 are embedded. The most important advantage of this structure is the PFD has no any feedback path. Hence the higher speeds will be achieved. Instead of the conventional PFDs which use the feedback path to reset the operation, in this structure, the reset process occurs automatically when the inputs are equal to "0". Also the other advantage of this circuit is the low power consumption because the precharge operation do not appear in this PFD. As shown in fig. 2, the proposed PFD circuit has single stage structure and consists of ten transistors which they are responsible to detect the differences of frequency and phase between the input signal and the feedback signal, as well.

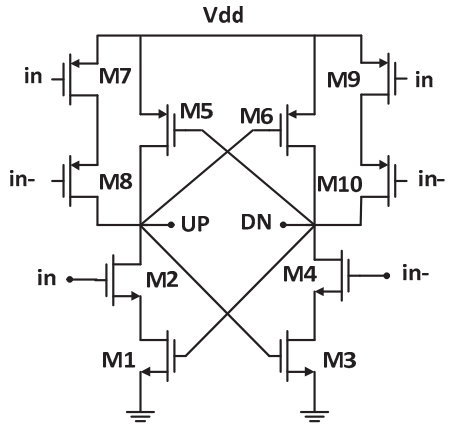

Fig. 2. The block diagram of the proposed PFD

B. Charge Pump and Low-Pass-Filter (CPL)

As shown in fig. 3, the CPL block is consists of two sub-blocks such as: a charge pump and a low pass filter which merged together. The differential input devices (M1-M4) are responsible for receive the input signals that produced by the PFD block (DN and UP), and the employment of the other transistors is necessary to guarantee the proper operation of the input P-MOS devices. In the conventional single ended charge pumps where just Vc+ produced by the circuit, the currents I1 and I2 not be equal, because of the diode-connection (M7) that is a origin of the systematic error and increases the RMS jitter of the system.

In the proposed structure, utilizing a full differential circuit as the charge pump leads to solve the systematic error and also decrement in the effect of the power supply noise on the operation of the charge pump, obviously. In order to define the closed loop frequency response of the system and also decrease the effect of the undesirable signals, a low-pass filter is employed.

This especial structure of the charge pump helps the system to have the fewer jitter and noise and also more proper response of the system will be achieved.

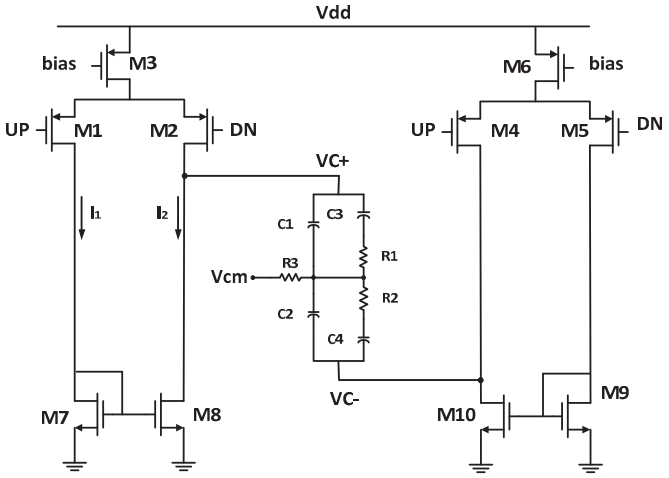

Fig. 3. The block diagram of the proposed CPL block

C. Voltage Controlled Oscillator (VCO)

Fig. 4 shows the block diagram of the differential proposed VCO. In this structure, the output frequency can be controlled by two voltages (Vc- and Vc+) and also the produced signal and its inverted version can be obtained at the output of the proposed VCO. The proposed VCO consists of three similar cells that each of which is shown in fig. 5.

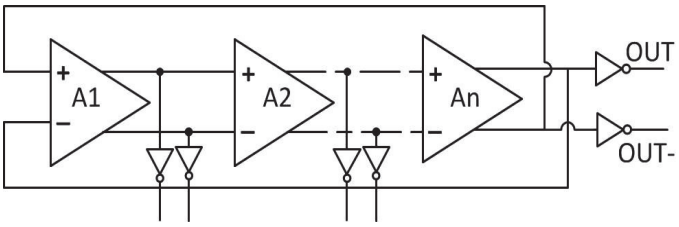

Fig. 4. The block diagram of the proposed VCO

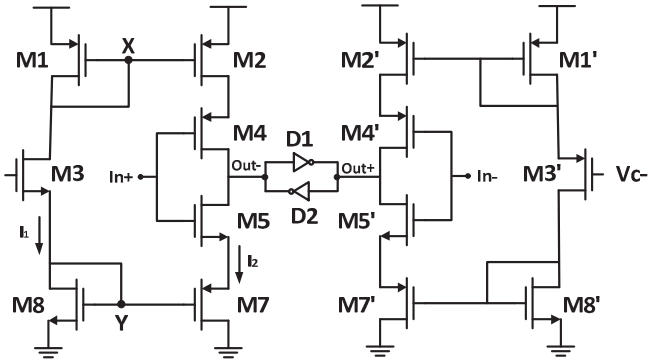

Fig. 5. One-cell of the proposed VCO

In order to synchronizing the circuit, the output of each cell is connected to the dummy inverters that are designed in minimum possible size. This idea helps to having the qualified and concurrent circuit especially when the output of the VCO is connected to the load. The transistors M4 and M5 operate as an inverter which its time constant and the output delay can be controlled by M2 and M7 devices. Hence any variation in the voltage of Vc+ will be changes the value of the I1 branch current. M1 and M8 devices are responsible to mirror the I1 current into the M2 and M7 transistors which leads to change the voltage of the X and Y nodes. Therefore, variation of Vc+ changes the value of I2 and it leads to change the time constant and out+, simultaneously. The other side of the circuit (M′ transistors) has the same operation but in this part, Vc- controls the process. In order to proportion the cell and synchronize the outputs (out+ and out-), two inverters (D1 and D2) have been employed which are implemented in minimum possible sizes.

II. Simulation Results and Comparison

This section describes the simulation results of the proposed full differential PLL which is designed in 0.18μm standard CMOS technology and works with the 1.8V power supply. Fig. 6 shows the frequency per control voltage ratio of the VCO. In order to prove our pretension, proper operation and settling behavior of the CPL is depicted in fig. 7.

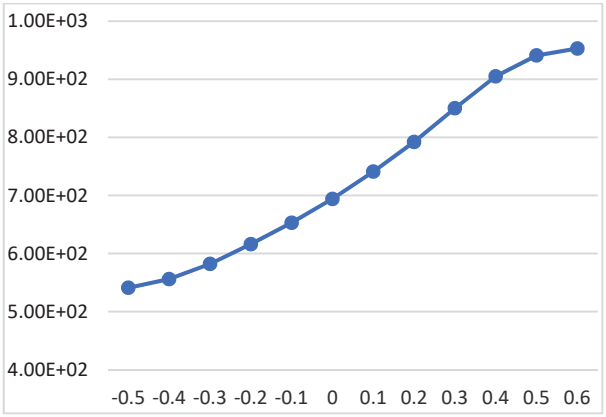

Fig. 6. Frequency per control voltage ratio of the VCO

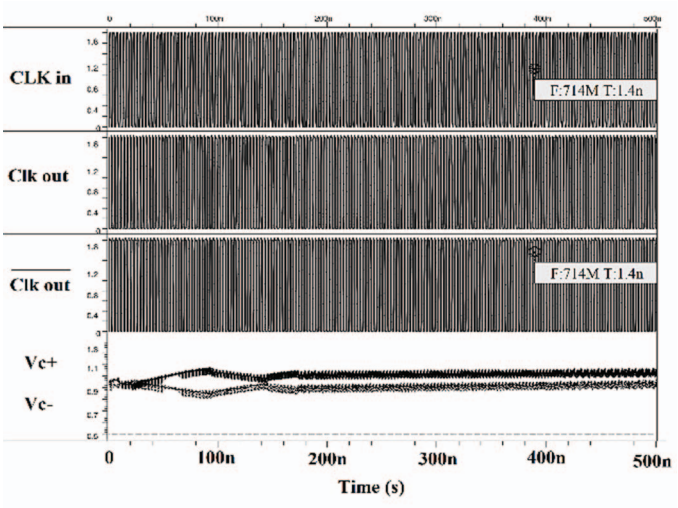

Fig. 7. Proper operation and settling behavior of the CPL

And also the relevant jitter of the proposed PLL demonstrated in the fig. 8. Fig. 9 allocated to show the output waveforms. Finally, in fig. 10 and fig. 11 difference and similarity between the phases of the input and feedback signals at the output PFD block are exhibited, respectively. In order to show the superiorities of the proposed PLL, table I summarizes the features of the work and also comparing the proposed structure with some similar approaches are reflected in table II.

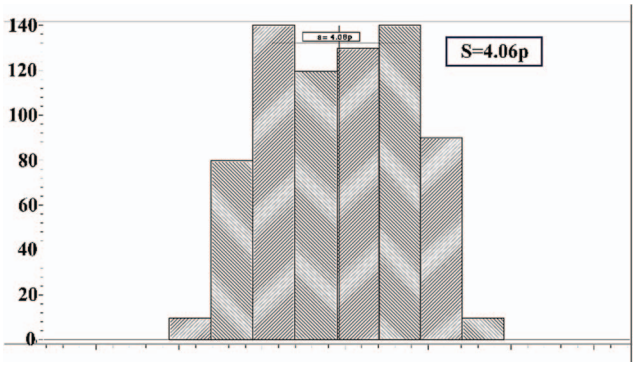

Fig. 8. The relevant jitter of the proposed PLL

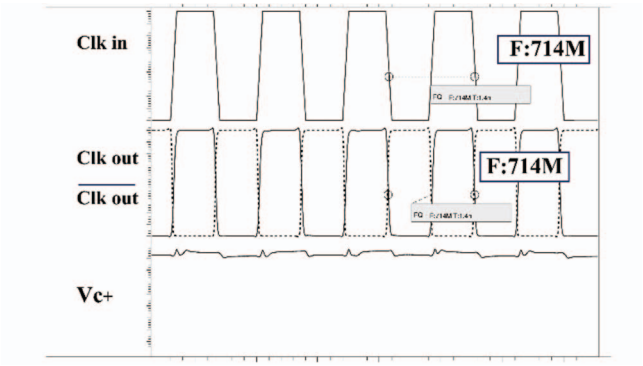

Fig. 9. The zoomed output waveforms of the proposed PLL

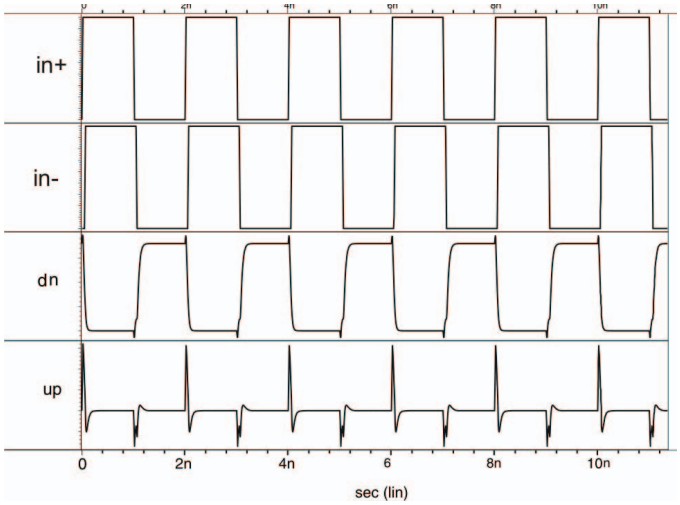

Fig. 10. Output waveforms of the PFD when two inputs have different phases (about 50ps)

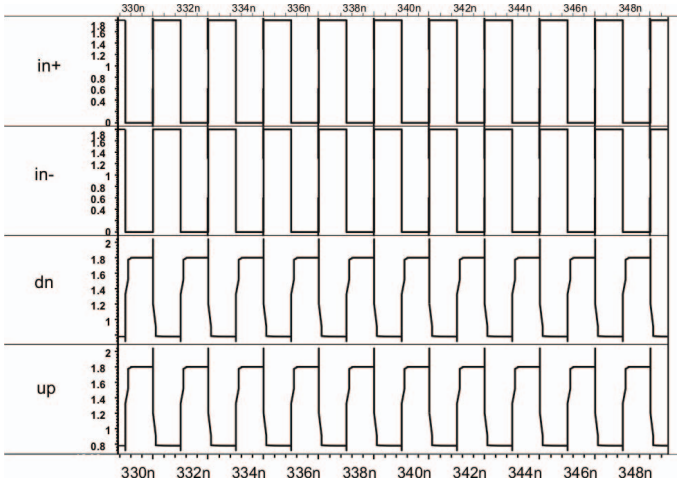

Fig. 11. Output waveforms of the PFD when two inputs have similar phases

TABLE I
FEATURES OF THE WORK

Process	180nm
Supply voltage	1.8v
Frequency	600MHz 900MHz
Jitter RMS	4.06ps
Power supply noise	50mV
Power	4.6mW

TABLE II.
COMPARISON

	This work	[6]	[7]	[8]
Process	0.18μm	0.18μm	0.6μm	0.40μm
Supply voltage	1.8V	1.8V	3.3V	2.5V
Frequency	600MHz 900MHz	768MHz 1020MHz	300MHz 800MHz	340 MHz 612 MHz
Jitter RMS	4.06ps	7.08ps	14.52ps	8.4 ps
Power supply noise	50mV	-	-	-
Power	4.6mW	-	105mW	100 mW

III. CONCLUTION

A new Phase Locked Loop (PLL) is described in this paper, which benefits from minimum jitter in the operation frequency range of 600MHZ to 900MHZ. The proposed structure benefits from a full differential architecture that consists of several blocks of differential VCO, a differential PFD and a differential CP leads to limiting the RMS jitter to 4.06ps, with 50mV power supply noise in the frequency range of 750MHz. The simulation results extracted through the HSPICE software in 0.18μm CMOS TSMC standard technology demonstrate the power-consumption of 4.6mW at the supply voltage of 1.8V.

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