# Versatile Low-Output-Resistance Low-Voltage Current-to-Voltage Analog Converter

Ryszard Wojtyna

Abstract—The paper presents a simple low-voltage transresistor attractive for on-chip analog-signal-processing. The proposed circuit offers not only an almost rail-to-rail operation and quite good linearity of DC transfer characteristic but also reasonably low value of its output resistance. This enables a voltage mode operation even if the transresistor is loaded by a not necessarily very high loading resistance. The obtained result is due to adding to the transresistor-input-stage a simple rail-to-rail voltage follower. The presented solution is an original proposal of the author. Input stage of the transresistor is built of only 4 MOS transistors and creates a simple quasi-linear current-to-voltage convertor. Output stage of it is built of 9 MOS transistors, plays a role of a very precise atypical voltage follower. In respect of simplicity and headroom, the proposed follower is better than conventional OA-based voltage followers. Preliminary simulation results are in a good agreement with the theory presented.

Index Terms—CMOS analog integrated circuits, low-voltage signal processing, current-to-voltage conversion, transresistor

# I. INTRODUCTION

RECENTLY one observes a growing interest in the field of advanced analog electronics. This concerns not only electronics used in optical fiber communication and optoelectronics but also analog signal processing [1]-[5]. The reason for that is a need to supplement digital electronics in more and more areas.

As regards signal processing, an important role plays a fact that analog processing creates a possibility of realizing both voltage mode and current mode operations implemented within a chip. Application of differential pair technique is an additional factor increasing potential of on chip analog processing.

Going from voltage-mode to current-mode operation and from current-mode to voltage-mode requires a good quality voltage-to-current converter (transconductor) or current-to-voltage converter (transresistor). This is like in cooperation between digital and analog electronics, where both digital-to-analog and analog-to-digital converters are needed.

In the literature, one can find different proposals of low-power transresistor implementations [6]-[10]. These proposals are focused mainly on achieving a close to linear conversion. In this paper, a new idea of creating quasi-linear low-power transresistor is presented. This idea is based on using two components connected in series. One of them is responsible for ensuring a possibly good linearity of the realized transfer function. A simple component used for this aim is based on the

R. Wojtyna is with the Faculty of Telecommunication, Computer Science & Electrical Engineering, University of Technology and Life Sciences, Bydgoszcz, Poland (e-mail: woj@utp.edu.pl)

idea described in [7]. Being a modification of this circuit, it functions as input stage of the proposed transresistor. The second component of the transresistor is a voltage follower, whose task is to obtain as small as possible output resistance of it. As the follower, a modified version of differential-amplifier-based voltage buffer, presented in [14], has been utilized.

The rest of the paper is organized as follows. Section 2 specifies voltage mode operation as well as current mode operation in view of the transresistor input and output requirements. Section 3 presents the simple initial transresistor stage that generates a quasi-linear transfer curve. In Section 4, superiority of common-drain over common-source used in output stage of the proposed transresitor is clarified. Section 5 presents the voltage follower added to the basic initial transresistor in order to achieve the wanted low output resistance. Complete transresistor circuit including all previously discussed elements is shown in Section 6. SPICE simulation results are shown in Section 7 and concluding remarks are gathered in Section 8.

#### II. CURRENT MODE AND VOLTAGE MODE OPERATION

To define voltage mode and current mode operation of electronic devices and circuits, consider the simple electrical model shown in Fig. 1. In this model, the voltage  $V_T$  presents ideal voltage source and  $Z_T$  internal impedance of this source. Such a series connection creates so called Thevenin's source, which is very useful in network theory. The  $Z_L$  impedance, on the right hand side, represents some loading block. Voltage across this impedance is denoted by  $V_L$ .

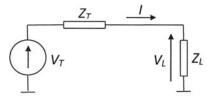


Fig. 1. Simple model explaining voltage as well as current mode of electronic circuit operations.

Making use of Kirchhoff's Rules and Ohm's Law, it is seen that the below given equations can be written as:

$$I = \frac{V_T}{Z_T + Z_L} \tag{1}$$

$$V_L = V_T \frac{Z_L}{Z_T + Z_I} \tag{2}$$

If the below given inequality (3) is fulfilled

$$\left|Z_{L}\right| >> \left|Z_{T}\right| , \tag{3}$$

then we obtain

$$V_L \cong V_T \neq f(Z_L) \tag{4}$$

which means, that the  $V_L$  voltage across the load is almost identical as the driving voltage source,  $V_T$ , and is independent on the loading  $Z_L$  impedance. This is the case of voltage mode operation.

Another situation takes place when the below given inequality holds.

$$\left|Z_{T}\right| >> \left|Z_{L}\right| \tag{5}$$

In such a case, we get:

$$I \cong \frac{V_T}{Z_T} \neq f(Z_L) \tag{6}$$

As can be seen from (6), the current denoted by I is dependent on the  $V_T$  and  $Z_T$  driving source and is not affected by the loading impedance. This is the current mode operation. In practice, current mode operation is realizable only when implemented in the integrated circuit form. Circuits considered further in this paper are based on the current mode as well as voltage mode operations. Both operation modes complement each other.

#### III. SIMPLE QUASI-LINEAR TRANSRESISTOR

Diagram of the proposed simple transresistor is presented in Fig. 2. The M<sub>1</sub> and M<sub>2</sub> transistors form a current mirror. The other two transistors, M<sub>3</sub> and M<sub>4</sub>, which are connected in series, create a nonlinear resistor. Nonlinear character of the resistor enables achieving a quasi-linear current-to-voltage conversion. The obtained almost linear operation is reached in a rather wide voltage range. To achieve this goal, the transistor M4 should operate in a non-saturation region (triode region). Proper designing the transistor sizes plays also an important role here.

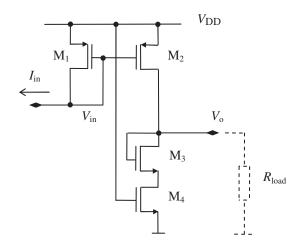


Fig. 2. Simple low-voltage current-to-voltage converter without voltage follower at the output.

One of conditions that must be fulfilled to achieve a quasilinear characteristic is to satisfy the below given inequality:

$$V_{DS} < V_{GS} - V_{th} , \qquad (7)$$

where  $V_{DS}$  is a drain-source voltage,  $V_{GS}$  a gate-source voltage and  $V_{th}$  is threshold voltage of the transistor M<sub>4</sub>.

To obtain a low voltage operation of the transresistor of Fig. 2, length of the M4 transistor channel must be considerably larger than its width.

### IV. COMMON SOURCE VERSUS COMMON DRAIN OUPUT STAGES

An essential disadvantage of the converter shown in Fig. 2 is its very high output resistance. In this paper, it is proposed to attach to the converter of Fig. 2 atypical voltage follower. An important matter of the proposed follower is using a common-drain configuration of the output stage, shown in part b) of Fig. 3. Then, variations of the output voltages can be only a little smaller than the follower supply voltage. This allows us to get a low-voltage operation of the transresistor (rail to rail operation). A satisfactory low level of the follower output resistance can be achieved by applying a very strong negative feedback to the circuit b) of Fig. 3.

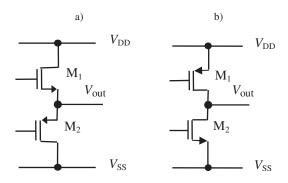


Fig. 3. Two configurations of output stages used in voltage followers:
a) low output resistance but narrow output voltage swingb) high output resistance but almost rail-to-rail operation.

Full diagram of the voltage follower that includes details concerning the feedback loop realization is discussed in the next section.

#### V. ATYPICAL VOLTAGE FOLLOWER WITH STRONG FEEDBACK

The proposed voltage follower, complementing the transresistor input stage of Fig. 2, is shown in Fig.4. In the presented follower, a negative feedback loop is applied. As a consequence, a strong reduction of output resistance and strong increase of input resistances of the follower can be achieved. In this way, the follower contributes to improving the transresistor properties, considerably.

In the top part of Fig. 4, denoted by a), the  $g_m$  element is a transconductance amplifier. The expected reduction of the follower output resistance significantly depends on how strong is the feedback. The stranger it is the better. Strength of the feedback is determined by gain of the open feedback loop. In

case of the used transresistor circuit, of prime importance is to obtain the great reduction of its output resistance. This is because the output  $M_{10}$ ,  $M_{20}$  transistors operate in commonsource configuration, which means a very large output resistance of the  $M_{10}\text{-}M_{20}$  pair. Even though common-drain configuration provides lower output resistance, the commonsource pair is superior to a common-drain pair because it offers bigger output voltage swing for a given supply voltage. The other transistors, i.e.  $M_{30}\text{-}M_{90}$ , are used to build a transconductance amplifier needed to create the feedback loop.

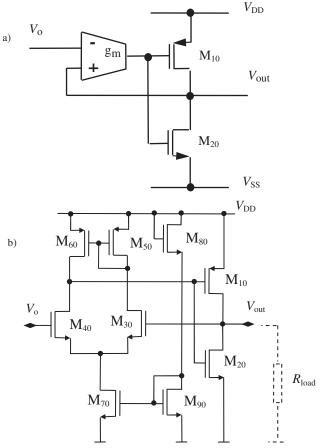


Fig. 4. High precision voltage follower with almost rail-to-rail operation and reasonably low output resistance:

a) simplified model, b) detailed diagram.

Applying a small-signal linear model of the proposed MOS transistors, output resistance of the considered voltage follower can be expressed as:

$$R_{of} \cong \frac{1}{\left(g_{ds1} + g_{ds2}\right)\left(1 + A\beta\right)} = \frac{R_o}{\left(1 + A\beta\right)} , \qquad (8)$$

where  $R_o$  is the follower output resistance under conditions when the feedback loop is open,  $g_{ds1}$  and  $g_{ds2}$  are drain-source conductances of the transistors  $M_{10}$ ,  $M_{20}$ , respectively, and  $A\beta$  is the dimensionless loop gain described by:

$$A\beta \cong \frac{g_{md} (g_{m1} + g_{m2})}{g_{dsd} (g_{ds1} + g_{ds2})}, \tag{9}$$

where  $g_{md}$  is a transconductance gain of the M<sub>30</sub>-M<sub>70</sub> transconductance differential amplifier,  $g_{dsd}$  drain-source output conductance of the M<sub>30</sub>-M<sub>70</sub> differential amplifier and  $g_{m1}$  and  $g_{m2}$  are transconductance gains of the M<sub>10</sub>, M<sub>20</sub> transistors, respectively.

If  $A\beta$  is very high and satisfies the condition:

$$A\beta >> 1 \tag{10}$$

then the expression (8) takes the simplified form:

$$R_{of} \cong \frac{R_o}{A\beta} \cong R_o \frac{g_{dsd}(g_{ds1} + g_{ds2})}{g_{md}(g_{m1} + g_{m2})} << R_o$$
 (11)

# VI. COMPLETE TRANSRESITOR WITH VOLTAGE FOLLOWER AT THE OUTPUT

Diagram of the complete transresistor, resulting from combining the simple circuit shown in Fig. 2 with the voltage follower of Fig. 4, is presented in Fig. 5.

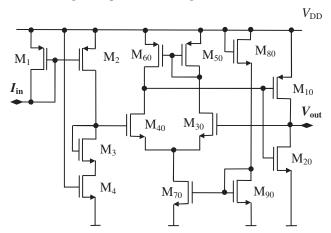


Fig. 5. Low-voltage transresistor with the atypical voltage follower of Fig. 4 decreasing the circuit output resistance.

Note that adding the voltage follower of Fig. 4 should cause almost no influence on the transresistor of Fig. 2. This is because output of this transresistor is connected only to gate of the  $M_{40}$  transistor and presents a very high input resistance. This resistance is additionally increased by acting the negative feedback, which can be expressed as:

$$R_{If} \cong R_I A \beta \cong R_I \frac{g_{md}(g_{m1} + g_{m2})}{g_{dsd}(g_{ds1} + g_{ds2})} >> R_I$$
, (12)

where  $R_{If}$  is input resistance of the M<sub>30</sub>-M<sub>70</sub> differential amplifier when feedback loop is closed, and  $R_I$  is the input resistance when the loop is open. Meaning of other parameters in (12) is the same as in the formulas (8) and (9).

#### VII. SPICE SIMULATION RESULTS

The performed SPICE simulations concern 0.35um CMOS process. Simulation factors are the following: supply voltage equal to  $V_{\rm DD}$  =2V; N-channel transistors threshold voltage equal to  $V_{\rm THN}$ =0.4655V; P-channel transistor threshold voltage

is  $V_{\rm THP} = -0.617V$ . Transistor length (L) and width (W) are given in Table 1 in case of the transresistor of Fig 2, and in Table 2 in case of the voltage follower of Fig. 4.

TABLE I
TRANSISTOR SIZES OF THE TRANSRESISTOR OF FIG. 2

Trans.	$M_1$	$M_2$	$M_3$	$M_4$	
W[µm]	88	66	1	1	
L[µm]	1	1	18	100	

TABLE II
TRANSISTOR SIZES OF THE FOLLOWER OF FIG. 4

Trans.	$M_{10}$	$M_{20}$	$M_{30}$	$M_{40}$	$M_{50}$	$M_{60}$	$M_{70}$	$M_{80}$	$M_{90}$
W[µm]	90	2	1	1	1	1	1	1	56
L[µm]	1	1	1	1	1	1	12	57	1

As already mentioned, the circuit of Fig. 2 should have a relatively good linearity of its transfer function and be simple. There are different ways to measure nonlinearities in situations like this. Among techniques, harmonic distortions, nonlinearity deviation and Volterra series can be applied for this purpose. The Volterra series is well suited to deal with problems concerning so called small nonlinearities [10]-[12]. Its disadvantage, however, is complexity and also problems with convergence of the Volterra series. This happens when the nonlinearity becomes bigger. For this reason, a decision to use yet another method has been taken. The made choice was to apply a simpler method based on derivative calculations. In our case, the calculation subject was the nonlinear curve presenting the current-to-voltage transfer function. Using this method, a satisfactory result has been achieved in case of small nonlinearities. That is the main reason why we chose the derivative based approach to the nonlinearity assessment issue.

Fig. 6 shows transfer characteristic of the  $M_1$ - $M_4$  transresistor. It is seen that the obtained current-to-voltage relation is quasi-linear in the current range from about  $0.1\mu m$  to  $2.2\mu m$ , which corresponds to voltage variation from about 0.55V to 1.95V. The achieved results are satisfactory if we take into account simplicity of the circuit (only 4 transistors).

Input resistance of the  $M_1$ - $M_4$  circuit can be determined by means of the graphs shown in Fig. 7. To be precise, absolute value of the upper curve determines the input resistance. As can be seen, value of this resistance decreases, i.e. approaches zero, if the input current grows up. Its mean value is relatively low (about  $10k\Omega$ ). This agrees with theoretical predictions and results from high aspect ratios of the M1 and M2 transistors.

Big disadvantage of the  $M_1$ - $M_4$  transresistor is its high output resistance. This is illustrated in Fig. 8. Voltage mode operation at the transresistor output requires a loading resistance being much larger (at least by two orders of magnitude) than output resistance of the  $M_1$ - $M_4$  circuit. For this reason, the load resistance must by extremely high. When dealing with analog signals this may be a problem.

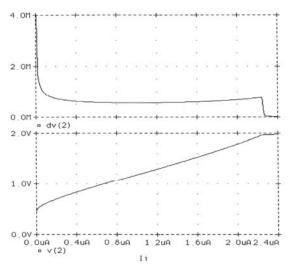


Fig. 6. DC transfer characteristic of the simple transresistor of Fig. 2: a) output voltage,  $V_0$ , versus  $I_{\rm in}$  input current (bottom), b) derivative  ${\rm d}(V_0)/{\rm d}I_{\rm in}$  versus  $I_{\rm in}$  (upper).

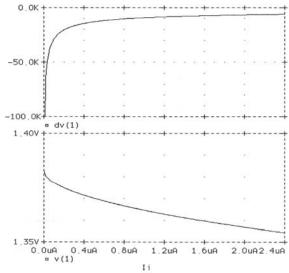


Fig. 7. Input resistance of the transresistor of Fig. 2: a) output voltage,  $V_{\rm in}$ , versus  $I_{\rm in}$  input current (bottom), b) derivative  $d(V_{\rm in})/dI_{\rm in}$  versus  $I_{\rm in}$  (upper).

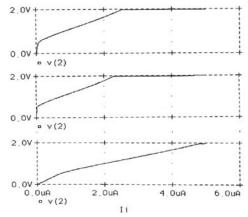


Fig. 8. Output voltage,  $V_0$ , as a function of the  $I_{\rm in}$  input current for different values of the  $R_{\rm load}$  resistor loading the transresitor of Fig. 2:

- a)  $R_{load}$  equal to  $1M\Omega$  (bottom),
- b)  $R_{\text{load}}$  equal to  $10\text{M}\Omega$  (middle),
- c)  $R_{load}$  equal to infinity (upper).

Fig. 8 presents the influence of  $R_{\rm load}$  resistance on voltage signal obtained at the  $M_1$ - $M_4$  transresistor output. Three values of the  $R_{\rm load}$  loads are considered. The first value is  $1 M \Omega$  (bottom), the second is  $10 M \Omega$  (middle), and the third is equal to infinity (upper). A difference between the upper and middle trace is small. The essential difference exists between the upper and bottom plots. Notice that the upper plot signal is approximately twice as high as that of the bottom one. Hence, the output resistance of the  $M_1$ - $M_4$  transresistor is close to  $1 M \Omega$ . This is a great value, too great for the transresistor to be used as a versatile current-controlled voltage source. The last matter that is worth taking into account is current and power consumed from supply rail of the  $M_1$ - $M_4$  transresistor.

In Fig. 9, the bottom curve presents current and upper shows the consumed power. Notice that power consumed by the proposed  $M_1$ - $M_4$  transresistor is very low. This results from both, the small number of transistors used and proper designing the transistor sizes. It is worth emphasizing that the current and power consumptions drop to zero if the input current goes to zero. This is a consequence of using current mirror at the circuit input.

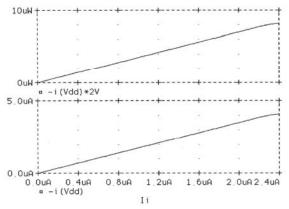


Fig. 9. Current (bottom) and power (upper) consumed by the transresistor without voltage follower.

Fig. 10 illustrates how important part in the proposed transresistor plays the voltage follower of Fig. 4. In all three plots of this figure, the required and obtained output voltages as functions of the follower input voltage are given. Black markers concern ideal voltage at the follower output while white markers refer to output voltage of the circuit shown in Fig. 2. To assess output resistance, the same methodology like in case of the  $M_1$ - $M_4$  transresistor can be applied. For the  $R_{load}$ resistance being equal to the circuit output resistance, output voltage signal becomes equal to about half of maximum value of the signal. The maximal level of the output voltage signal is achieved when  $R_{load}$  is equal to infinity, i.e. when the follower is not loaded. Having this in mind, we conclude that the obtained output resistance of the circuit of Fig. 2 is equal to about  $1k\Omega$ . Comparing this value with the output resistance of the  $M_1$ - $M_4$  transresistor (1M $\Omega$ ) we see that adding to the  $M_1$ -M<sub>4</sub> circuit the voltage follower leads to reduction of output resistance by about 3 orders of magnitude. This is an impressive result.

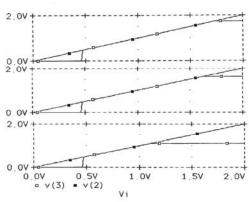


Fig. 10.  $V_0$  input voltage (marked in black) and  $V_{\text{out}}$  output one (white markers of the follower of Fig. 2, for different values of the loading  $R_{\text{load}}$  resistor:

- a)  $R_{\text{load}}$  equal to  $1\text{k}\Omega$  (bottom),
- b)  $R_{load}$  equal to  $10k\Omega$  (middle),
- c)  $R_{load}$  equal to infinity (upper).

In Fig. 11, the circuit output voltage (marked by white) and the required voltage (marked by black) are almost identical in the voltage range from about 0.45V to 1.75V, provided that  $R_{load}$  is much higher than  $1k\Omega$  (at least by 2 orders of magnitude). The achieved almost ideal transfer properties of the voltage follower are mainly due to the strong negative feedback applied. The observed voltage range restrictions are caused by the  $M_{30}$ - $M_{70}$  differential amplifier.

Fig. 12 presents power (upper plot) and current (bottom plot) consumed by the complete transresistor of Fig. 5. In comparison with results concerning the simple transresistor of Fig. 2 (see Fig. 9), the power and current consumptions shown here are rather high. This is caused by the applied voltage follower.

At the end, it is worth emphasizing that the used 2V supply voltage of the presented circuit is quite small in view of the sum of absolute values of the PMOS and NMOS threshold voltages, being equal to 0.617+0.4655 = 1.087V. As for analog signal processing, this result is promising.

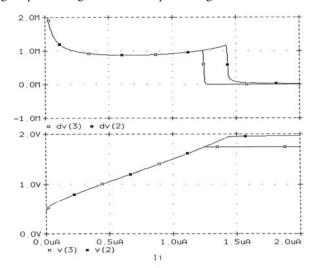


Fig. 11. DC transfer characteristics of the transresistor shown in Fig. 5 with the applied voltage follower:

- a)  $V_0$  voltage at the follower input (marked in black) and  $V_{\text{out}}$  voltage at the follower output (white markers) versus the  $I_{\text{in}}$  current (bottom),
- b) derivatives  $d(V_0)/dI_{in}$  (black) and  $d(V_{out})/dI_{in}$  (white) versus  $I_{in}$  (upper).

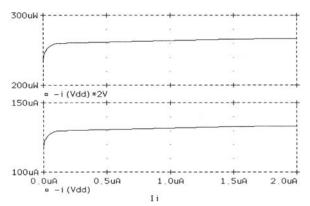


Fig. 12. Current (bottom) and power (upper) consumed by the transresistor with the voltage follower.

#### VIII. CONCLUSIONS

The paper presents a new proposal in the field of current to voltage conversion. A novel transresisitor being suitable for analog signal processing has been considered. Specificity of analog signal processing is that both voltage mode and current mode processing can be applied when implementing within a chip. This means a need for using voltage-to-current as well as current-to-voltage conversion, i.e. creating low-voltage transconductors and transresistors. In this paper, a CMOS transresistor circuit is presented. Its important advantage, apart from simplicity, is relatively low output resistance. As a consequence, the transresistor can serve as a currentcontrolled voltage source. This enables to work not only with very high loading resistances but also with quite small ones. In the proposed transresistor, the achieved output resistance is low (about  $1k\Omega$ ). The reached low output resistance is a result of applying very strong negative feedback acting around a simple transconductance amplifier (see Figs. 4 and 5). A simplified mathematical model of the circuit has also been presented (sections II, III, V and VI), which describe the transresistor operation and its properties. Among others, a rather good linearity of the made current-to-voltage conversion has been reached by means of only 4 CMOS Theoretically predicted operation of the transresistor was verified using SPICE simulations. In the carried out simulations, the main goal was to verify whether the proposed idea is right. Having this in mind, a relatively simple model of the circuit was applied. The obtained simulation results have preliminary character and are in a good agreement with theory. More detailed research in this field will be continued.

## REFERENCES

 E. Vittoz, "Micropower techniques" in design of analog-digital VLSI circuits for telecommunications and signal processing", Edit. J. Franca and Y. Tsividis, Prentice Hall, 1993.

- [2] W. Machowski, S. Kuta, J. Jasielski, J. Kołodziejski, "Fast low voltage analog four-quadrant multipliers based on CMOS inverters", International Journal of Electronics and Telecommunications, vol. 56, no. 4, s. 381-386, 2010.
- [3] R. Wojtyna, "Analog-technique-based neuroprocessing implemented in hardware", IEEE Workshop SPA 2009 (Signal Processing – Algorithms, Architectures, Arrangements and Applications), pp. 9-12, 2009.
- [4] R. Długosz, T. Talaśka, W. Pedrycz, R. Wojtyna, "Realization of the Conscience Mechanism in CMOS Implementation of Winner-Takes-All Self-Organizing Neural Networks", IEEE Trans. Neural Networks, Vol. 21, No. 6, pp.961-971, 2010.
- [5] R. Wojtyna, "Differential-pair-based Current-mode Analog Signal Processing", International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES), pp. 585-588, Toruń 2015.
- [6] M. Schlarmann, R. L.Geiger, "Simple CMOS Transresistor", Electronics Letters, Vol. 37, Issue 23. pp. 1386-1387, 2001.
- [7] R. Wojtyna, T. Talaśka, "Transresistance CMOS neuron for adaptive neural networks implemented in hardware", Bulletin of the Polish Academy of Sciences, Technical Sciences, Vol. 54, No. 4, pp. 443-448, 2006
- [8] K. Gupta, B.P. Singh, R. Choudhary, "Design and Analysis of Current-to-Voltage and Voltage-to-Current Converters using 0.35um technology", International Journal of Emerging and Advanced Engineering, Vol. 2, Issue 4, April 2012.
- [9] Texas Instruments, "AN-1244 photo-diode current-to-voltage converters", Application Report SNOA423B-August 2002 - Revised May 2013.
- [10] S. Narayanan, "Transresistor Distortion analysis using Volterra series representation", The Bell Syst. Tech. Journal, vol. 46, May-June 1967, pp. 991-1119.
- [11] W. J. Rough, "Nonlinear system theory: the Volterra/Winner approach", Johns Hopkins Univ. Press Baltimore (MD) 1981.
- [12] A. Borys, "An Analysis of slew-induced distortion in single –amplifier active filers using the Volterra-Winner series technique", Int. Journal of Circuits Theory and Application", vol. 10, 1982, pp. 81-94.
- [13] R. Wojtyna, "CMOS voltage buffer for extremely low supply operation", Electron Technology Journal, pp. 288-292, Vol. 32, No. 3, ITE 1999.
- [14] R. Wojtyna, "Low-voltage Quasi-linear Current-to-Voltage Analog Signal Processing", International Conference MIXDES'2016, pp. 585-588, Łódź, 2016.



Ryszard Wojtyna received the M.Sc. in electronics from the Technical University of Gdańsk, Ph.D. degree in electronics from the Technical University of Poznań and Dr. of Science degree (D.Sci.) in electronics from the Technical University of Łódź, all in Poland, in 1974, 1982 and 1997, respectively. In 1974, he joined the Institute of Telecommunication, University of Technology and Live Sciences, in Bydgoszcz, Poland. Currently, he is Associate Professor at this university and head of

Institute of Electronics and Computer Science. His main research interests are in the field of low-power analog signal processing based on both voltage-mode and current-mode CMOS circuits. R. Wojtyna published 138 works, including 87after receiving the D.Sci. degree. He was a supervisor of 4 doctorates, realized partly in cooperation with the University of Alberta in Edmonton, Canada. R. Wojtyna is a member of Committee of Electronics and Committee of Technical Cybernetics of the Polish Academy of Sciences (PAN). He is also a member of Polish Electrical Engineers Association (SEP).