BULLETIN OF THE POLISH ACADEMY OF SCIENCES
TECHNICAL SCIENCES, Vol. 69(3), 2021, Article number: e137386
DOI: 10.24425/bpasts.2021.137386

Multiparameter reliability model for SiC power MOSFET subjected to repetitive thermomechanical load

Sebastian BĄBA*

TRUMPF Huettinger Sp. z o.o., Research and Development Department, 05-220 Zielonka, Poland

Abstract. The main drawback of any Design for Reliability methodology is lack of easy accessible reliability models, prepared individually for each critical component. In this paper, a reliability model for SiC power MOSFET in *SOT* – 227*B* housing, subjected to power cycling, is presented. Discussion covers preparation of accelerated lifetime test required to develop such reliability model, analysis of semiconductor degradation progress, samples post-failure analysis and identification of reliability model parameters. Such model may be further used for failure prognostics or useful lifetime estimation of high performance power supplies.

Key words: reliability engineering; reliability modelling; power MOSFET; SiC.

1. Introduction

Power electronics has penetrated every branch of life in XXI century – starting from power conversion for renewable energy sources, through electric vehicles, up to a variety of industrial applications. Thus, reliability aspects of modern power electronics are more and more often discussed by researchers and engineers. These topics covers various applications of power electronic converters – from plasma surface processing [1], through renewable energy sources [2], up to electric aircraft concept and automotive industry [3].

Among areas of research which focus on increasing reliability of modern power converters, the Design for Reliability (DfR) methodology [4, 5] was found especially interesting. This concept is based on the idea that overall reliability of power converter can be assessed for pre-defined set of stress levels, based on known reliability models for either power converter functional modules or its critical components. By analogy to critical components of e.g., pump system [6], critical elements of modern power converter are power semiconductor devices, capacitors, mechanical connectors, integrated circuits, and others. Typically, DfR procedure consists of the following steps:

2) mission profile and environmental parameters definition,
3) system-level mission profile evaluation,
4) circuit modelling,
5) stressors levels evaluation for critical components,
6) reliability evaluation for critical components,
7) system-level reliability assessment.

The significant drawback of this approach is that for each critical component there are numerous different failure modes and each of them is accelerated by various stressors. Therefore, a reliability models should be prepared not only for each critical component separately, but for each failure mode, as a function of stress level for better accuracy [7, 8]. Another problem is that the reliability model parameters of each failure mode are unique for each component as they depend on the structure of the component (e.g., thickness and length of wire bonds in the case of semiconductor devices) and manufacturing process (e.g., cooling ramp) of the critical component itself.

In this paper, a reliability model of SiC power MOSFET in *SOT* – 227*B* housing is presented. Although reliability modelling of SiC devices was investigated by various researchers, the previous papers was focused on multichip IGBT or MOSFET modules [9, 10] and discrete devices in *TO* – 220 or *TO* – 247 housing [11, 12]. The industry-grade *SOT* – 227*B* housing, for high power semiconductor devices, has not been investigated yet. The developed reliability model was prepared based on an Active Power Cycling (APC) test results, optimized to expose *fatigue-like* failure modes of encapsulated discrete devices: bond wire lift-off, solder joint fatigue, bond wire heel cracking, solder delamination or brittle cracking. The test bench itself, detailed description of test procedure and preliminary results were already discussed in [13], thus here only a basic description of APC test is given. Instead, this paper covers failure mechanism analysis, proposal of reliability model and reliability model parameter identification process.

This paper is organized as follows: in Section 2 the APC test concept is introduced. Discussion is followed in Section 3, where test results are presented. Next, in Section 4 the mathematical model used for the reliability assessment of encapsulated SiC devices is discussed. The summary and conclusions are given in Section 5.

8. Accelerated lifetime testing

The dominant failure modes for encapsulated SiC power MOSFETs are either chip-related or package-related. The typical chip-related failure modes are:

*e-mail: sebastian.baba@trumpf.com

Manuscript submitted 2021-02-06, revised 2021-03-23, initially accepted for publication 2021-04-15, published in June 2021

1) gate oxide degradation and time dependent dielectric breakdown (TDDB) [14, 15],
2) brittle cracking, induced by heavy mechanical stress caused by mismatch in thermal expansion coefficient (CTE) between SiC and other materials used in semiconductor manufacturing [16],
3) single event effects (SEE) caused by high energy particles (e.g., neutrons) [17].

Next chip-related failure mode is stacking fault, caused by third quadrant operation of SiC power MOSFET. This topic is still under investigation by various researchers [14, 18]. Other dominant failure modes are package related – e.g., solder delamination, solder joint fatigue, bond wire lift-off, bond wire heel-cracking or corrosion [19, 20].

Other way to group main failure modes of SiC power devices is usage of the Bathtub curve, depicted in Fig. 1. Typically, lifetime of every power electronic component can be divided into three regions:

1) the "Infant Mortality" or "Intrinsic Failure" region, where failures are mostly caused by internal defects or impurities, and they are strictly related to quality of manufacturing process,
2) the "Useful Lifetime" or "Random Failure" region, where failure rate is relatively constant,
3) the "Fatigue Failure" or "Extrinsic Failure" region, where probability of failure significantly increases due to progressing wear-out of the device.

Therefore, as either TDDB, brittle cracking or *fatigue-like* failure modes are a result of progressing degradation of SiC power semiconductor device, these failure modes are typical for "Extrinsic Failure" region. In contrast, the SEE failures are typically the dominant component of failure rate mix during the "Useful Lifetime" region, and stacking faults shall be present mostly in the "Infant Mortality" region, as they are directly related to quality of manufacturing process.

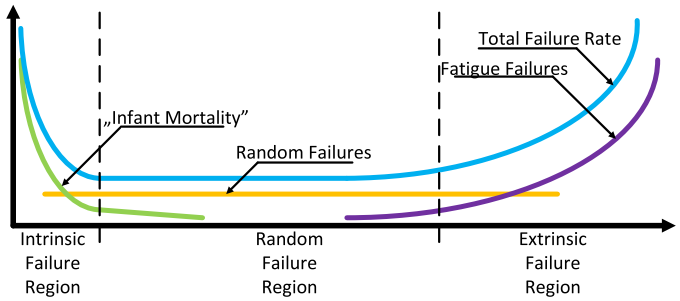


Fig. 1. The "Bathtub Curve", simplified graphical representation of failure rate change over time

The goal of presented reliability model is to determine the Useful Lifetime of SiC power MOSFET subjected to heavy thermomechanical load – typical to power cycling operating conditions. The alternate definition of the Useful Lifetime, states that it is a time when the degradation mechanisms initiates, e.g., single bond wire gets lifted off. Typically, End of Life (EoL) criteria is denoted as the slight shift of the power semiconductor electrical parameters from its nominal value [21]. However, in the both cases the Accelerated Lifetime Testing (ALT) procedure and reliability model identification procedure is exactly the same. The only differences are the EOL criterias used in ALT, and the input data used for reliability modeling. In this paper, the reliability model was prepared based on actual failures recorded during APC test, in contrast to the typically utilized approach [22–24].

Typical test methods used by researchers to introduce heavy thermomechanical load to power semiconductor structure, and thus – to accelerate *fatigue-like* failure modes are Thermal Cycling (TC), Power Cycling (PC) and Current Cycling (CC). In TC, referred also as *passive* cycling, the amplitude and slope of temperature swing are remained constant over the test progress. However, this approach has a significant disadvantage – in real life operating conditions, progressing degradation of semiconductor device results in higher and higher junction temperature per cycle, which causes a self-acceleration mechanism. Moreover, the junction temperature slope in TC is far less than in case of PC or CC, as in these tests it is limited only by the thermal capacitance of the heatsink. Thus, the mechanical stress in semiconductor structure is significantly higher in either PC or CC than in TC, which corresponds to significant difference in test results [25, 26].

The alternate approach is the PC test, referred also as *active* cycling, as power semiconductor structure is actively heated by power losses. Although, recent study [27] does not distinguish difference between PC and CC, in the first case power dissipated in tested semiconductor device is constant during ALT, while in the second case the current flowing through tested devices is remained constant during ALT. Therefore, in CC test a power dissipated across each tested device increases along degradation of semiconductor device progresses. Simply, increased channel on-state resistance ($R_{DS_{on}}$) or collector-emitter junction voltage drop (V_{CE}), results in higher power dissipation for the same current conducted through tested device. In fact, this is next self-acceleration mechanism, which additionally shorten power semiconductor useful lifetime. Thus, there is a significant difference between PC and CC test results [24].

The CC test, described in e.g., AQG-324 guideline [28], is well suitable for automotive, railway or grid applications, where conduction losses dominate. However, because of their superior performance (e.g., low gate charge and parasitic capacitance), *SiC* power MOSFETs are typically used in high frequency switching application, like resonant- or soft-switching converters, in which *SiC* devices are subjected to rather switching than conduction losses. Unfortunately, in certain applications it is rather difficult to estimate if SiC power MOSFET switching losses will increase or remain fairly constant during operation of power converter, as they are dependant on various exterior conditions – e.g., degradation rate of driver circuit, ambient temperature, environmental conditions, load, etc. Thus, it was decided to conduct a PC test with constant level of power dissipated across tested samples, to increase applicability of the test results.

The sampleset consisted of 52 SiC power MOSFETs (initially 40 samples, 12 samples were added after $\sim 65k$ power cycles), which were subjected to operating conditions listed in

Tables 1 and 2 respectively. Devices Under Test (DUTs) were connected in series, and voltage drop across each sample (V_{DS}) was as controlled separately, with proper adjustment of gate-source (V_{GS}) potential. The amplitude of initial junction temperature swing – at the very beginning of the ALT – was determined based on baseplate temperature (T_C) measurement, dissipated power (P_L) and known initial thermal impedance between junction and case $Z_{TH_{J-C}}$. For purposes of health monitoring, $R_{DS_{on}}$ and V_{FWD} were measured once per 2000–2500 cycles, similarly to concept presented in [12]. As presented in [13], such approach is sufficient to detect progressing degradation of SiC power MOSFETs. The test itself was conducted up to fatal failure, as obtaining the information for *how long* the heavily degraded device is capable to operate was an additional goal of research.

Table 1
Operating conditions of tested semiconductor devices: nominal values

Sample set no.	P_L [W]	ΔT_J [°C]	$T_{J_{LOW}}$ [°C]	$T_{J_{HIGH}}$ [°C]
A	150.5	90.5	30	120.5
B	175	105.3	50	155.3
C	126	76.5	50	126.5
D	126	76.5	30	106.5
J	175	105.3	30	135.3

Table 2
Operating conditions of tested semiconductor devices: dispersion

	P_L [W]		ΔT_J [°C]		$T_{J_{HIGH}}$ [°C]	
	Mid-range	+/−	Mid-range	+/−	Mid-range	+/−
A	150.66	0.43	90.40	0.26	120.40	0.26
B	174.95	1.34	104.97	0.80	154.97	0.80
C	126.91	0.39	76.14	0.24	126.14	0.24
D	127.64	0.36	76.58	0.22	106.58	0.22
J	175.16	2.04	105.09	1.22	135.09	1.22

3. Test results

Failures recorded during test are listed in Table 3. To verify if failures were indeed caused by *fatigue-like* failure modes, 32 random selected samples were subjected to post-failure analysis, which consisted of following steps:
1) electrical measurement,
2) X-Ray imaging,
3) Confocal Scanning Acoustic Microscopy (CSAM),
4) post-decapsulation visual inspection.

As presented in Table 4, most failures resulted in both Gate-Source and Drain-Source shorted.

Table 3
Failures recorded during APC test

	group A	group B	group C	group D	group J
#1	63394	33163	–	92328	28973
#2	79651	63189	96526	82532	21451
#3	82532	24643	–	92328	24874
#4	82532	63189	–	92328	19157
#5	92328	33359	75037	92328	24727
#6	63404	16283	–	92328	28973
#7	92328	33100	–	82512	25719
#8	67710	18975	–	92328	22882
#9	63394	16756	133117	76829	28973
#10	48793	63189	–	91794	28973
#11	N/A	N/A	N/A	N/A	19686
#12	N/A	N/A	N/A	N/A	19536

Table 4
Electrical test results of failed SiC power MOSFETs

Sample	$G-S$	$D-S$	Sample	$G-S$	$D-S$
1A	Shorted	Shorted	1C	–	–
2A	Short circuit to PE		2C	Shorted	15$k\,\Omega$
3A	Shorted	Shorted	3C	–	–
4A	Shorted	Shorted	4C	–	–
5A	Shorted	Shorted	5C	Open	Shorted
6A	Shorted	Shorted	6C	–	–
7A	Shorted	Shorted	7C	–	–
8A	Shorted	Shorted	8C	–	–
9A	Shorted	Shorted	9C	Shorted	Shorted
10A	2.2 Ω	Shorted	10C	–	–
1B	Open	Instable	1D	Shorted	Shorted
2B	Shorted	Shorted	2D	Shorted	Shorted
3B	Shorted	Shorted	3D	Shorted	Shorted
4B	Shorted	Shorted	4D	Shorted	Shorted
5B	Shorted	Shorted	5D	Shorted	Shorted
6B	Shorted	Shorted	6D	Shorted	Shorted
7B	4 Ω	3.5 Ω	7D	Shorted	Shorted
8B	Instable	Instable	8D	Shorted	Shorted
9B	Shorted	Open	9D	Shorted	Shorted
10B	Shorted	Shorted	10D	Shorted	Shorted
1J	Shorted	Shorted	7J	Shorted	Shorted
2J	Shorted	Shorted	8J	Shorted	Open
3J	Shorted	Shorted	9J	Shorted	Shorted
4J	Shorted	Shorted	10J	Shorted	Shorted
5J	Shorted	Shorted	11J	Shorted	Shorted
6J	Shorted	Shorted	12J	Shorted	Shorted

Laboratory analysis has shown that among analyzed samples, over 24 DUTs had few or all bond wires lifted-off. Moreover, in single bond wire, the heel-crack was found (see Fig. 2). In some devices, although most of bond wires were lifted-off, the soldering beneath the chip remained intact (see Fig. 3). However, C-SAM imaging revealed severe solder delamination in 19 DUTs – in certain examples chip was completely detached from the metal paddle. In some samples, X-Ray imaging and visual inspection of decapsulated device revealed also a crack across the SiC chip.

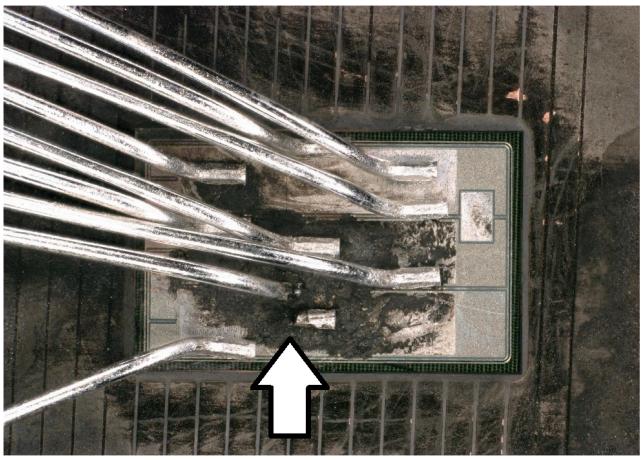
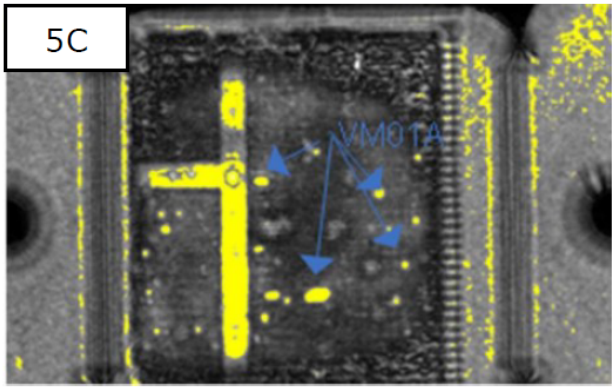


Fig. 2. Top view of DUT #6*J* after chemical decapsulation process. Cracked bond wire is marked with white arrow

a)



b)

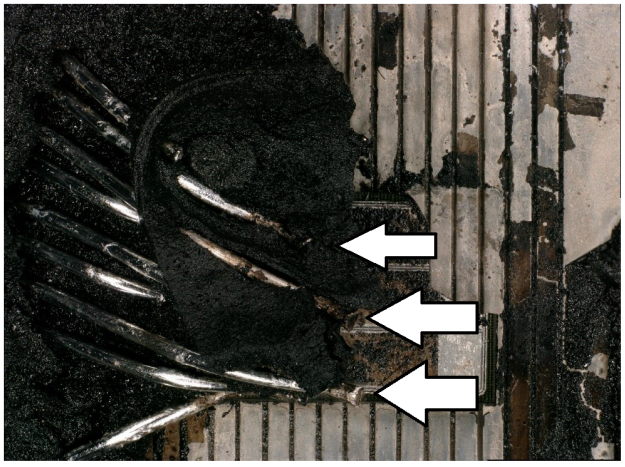


Fig. 3. Bottom-up CSAM imaging a), and post decapsulation photography of DUT #5*C*. Minor voids and cavities, marked with blue arrow, are not considered as rejectable according to the J-STD-020E standard, while clearly some of bond wires are lifted off (see white arrows)

Images of semiconductor devices subjected to chemical decapsulation process were further analyzed in order to determine whether there is any correlation between initial position of bond wires and probability of lifting them off. For this purpose, each bond wire was labeled with number and total amount of lifted bond wires was summed up. As presented in Fig. 4, there is no distinct correlation between initial position of bond wire and probability of their detachement. Next, post-failure analysis confirmed that tested power MOSFETs failed due to *fatigue-like* failure modes. Thus, it was possible to use this test results to develop a reliability model, which could be used to estimate Useful Lifetime of SiC power MOSFET in $SOT-227b$ housing.

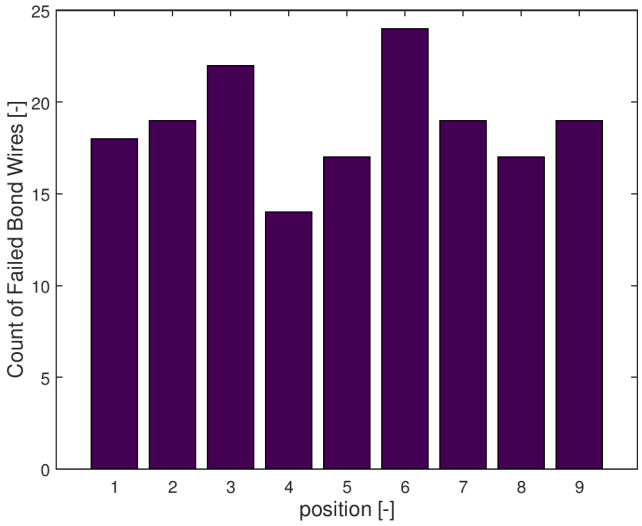
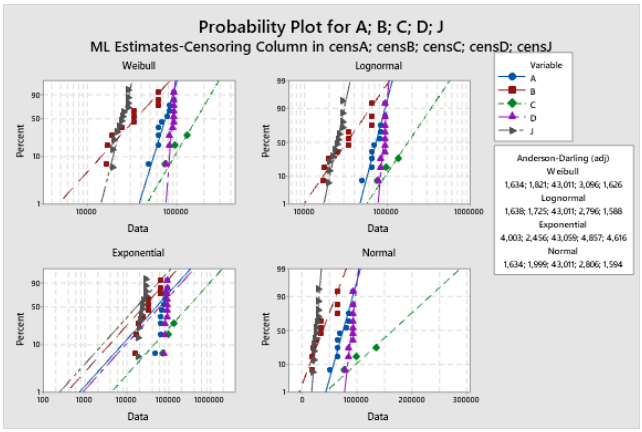


Fig. 4. The cumulative distribution of lifted bond wires vs their position

4. Reliability model

One of the most recognized mathematical models used in reliability engineering is a Weibull distribution [29], which has been proven as suitable for various failure-modes of semiconductor power devices – from fatigue of solder interconnection [30] to time-dependent dielectric breakdown of gate-oxide layer [31]. Thus, it was expected that Weibull model will be also suitable for *fatigue-like* failure modes. To confirm this thesis, a various mathematical models were fitted to failures with Maximum Likehood Estimation (MLE) algorithm. As depicted in Fig. 5, neither of compared distributions (2- and 3- parameter Lognormal, 1- and 2- parameter Exponential, Logistic, Normal) allowed for significantly better fitting. Moreover, both visual inspection and analysis of Anderson-Darling test results suggests that either 2- or 3- parameter Weibull model assures satisfactory projection of recorded data. Thus, the Weibull model was chosen for further investigation.

a)



b)

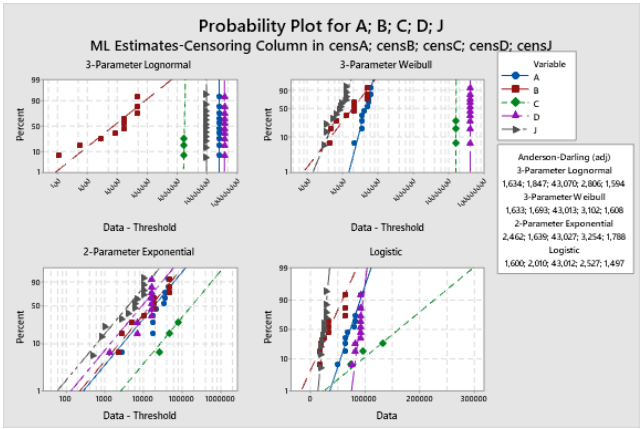
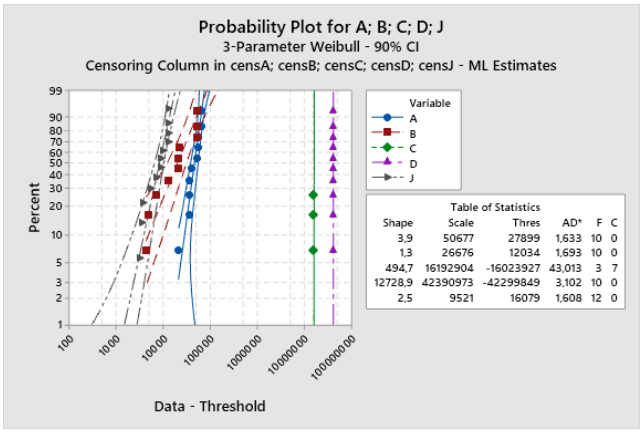


Fig. 5. Cross-comparison of various mathematical distributions fitted to the APC test results

a)



b)

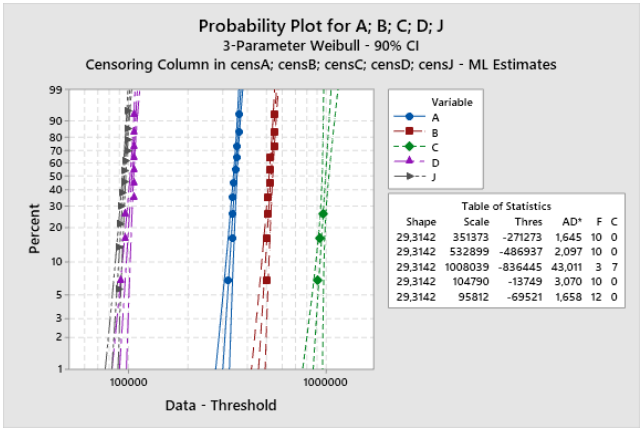


Fig. 6. Probability plots prepared for each tested sample set of SiC power MOSFETs, based on 3-parameter Weibull model asumming separate a) and common b) *shape* parameter

Typically, Weibull distribution is described with equation (1), where $f(t)$ is a Probability Density Function (PDF), β, η and γ are model parameters, called *shape parameter*, *scale parameter* and *location parameter* respectively.

$$f(t) = \left(\frac{\beta}{\eta}\right)\left(\frac{t-\gamma}{\eta}\right)^{\beta-1}\left(e^{-\left(\frac{t-\gamma}{\eta}\right)^{\beta}}\right). \tag{1}$$

Next, the β, η and γ parameters were identified for each distribution. Then, the probability plots were drawn accordingly, as depicted in Fig. 6. As a *shape* parameter is related to failure mode itself, and common failure mode was already confirmed for all samples during post-failure analysis, the common *shape* parameter was assumed for all models. Although models presented in Fig. 6 properly project reliability of SiC MOSFETs, there are still far from any useful form. As an example, each of these models is correct only for specific stress level – e.g., junction temperature swing or maximum junction temperature. Thus, the universal model, which could be used in DfR procedure was developed.

For this purpose, the *scale* parameter had to be modified to form of multivariable function. Either LESIT [32], originally developed for solder connections, or CIPS2008 model [33], originally developed for Si IGBT modules, could be used. Original forms of LESIT model and CIPS2008 model are presented in (2) and (3), respectively.

$$N_f = A \cdot (\Delta T_J)^{\alpha} \cdot exp^{\frac{E_A}{k_B \cdot (T_{MEAN}+273)}}, \tag{2}$$

$$N_f = K \cdot (\Delta T_J)^{\beta_1} \cdot exp^{\frac{\beta_2}{T_J+273}} \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6}. \tag{3}$$

In these models, the N_f is mean useful lifetime expressed in cycles, while parameters A, K, α, β_1–β_6 are the material constants, E_A is activation energy and k_B is Boltzmann constant. In both formulas, amplitude of temperature swing per cycle (ΔT_J), mean junction temperature (T_{MEAN}), and absolute maximum junction temperature (T_J), are expressed in Celcius. In addition, CIPS2008 model includes also impact of power on-time (t_{on}), current per wire bond (I), chip blocking voltage (V) and diameter of bonding wire (D) in useful lifetime calculation.

As it was stated in previous paragraph, either LESIT or CIPS2008 models were originally developed for different applications. Thus, all constant parameters had to be identified based on the APC test results. As all power cycles were performed with the same on-time, and only one kind of SiC power MOSFET was subjected for Accelerated Lifetime Testing (ALT), the

CIPS2008 model could be simplified into following form (4).

$$N_f = K \cdot (\Delta T_J)^{\beta_1} \cdot exp^{\frac{\beta_2}{T_J+273}} \cdot I^{\beta_3}. \tag{4}$$

Therefore, to prepare a universal model, a Weibull model in which the *scale* parameter is a function of stress levels, equations (2) and (4) were used.

$$\eta_1(\Delta T_J, T_{J_{MAX}}) = A \cdot (\Delta T_J)^{\alpha} \cdot exp^{\frac{E_A}{k_B \cdot (T_{J_{MAX}}+273)}}, \tag{5}$$

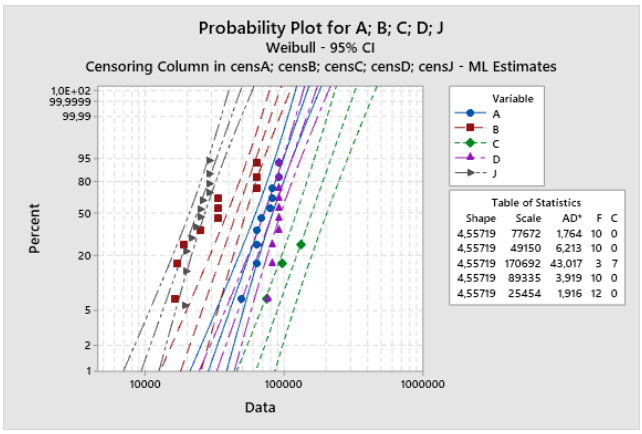
$$\eta_2(\Delta T_J, T_{J_{MAX}}, I_{DS}) = K \cdot (\Delta T_J)^{\beta_1} \cdot exp^{\frac{\beta_2}{T_{J_{MAX}}+273}} \cdot I_{DS}^{\beta_3} \tag{6}$$

The last remaining parameter in Weibull distribution formula (1) is the *location* parameter. For discussed universal model, it was assumed that failure may occur at any time, resulting in $\gamma = 0$. This allowed to simplify 3-parameter Weibull distribution to it's 2-parameter equivalent (7). This form was used to prepare a universal model, suitable for the purposes of a DfR procedure.

$$f(t) = (\frac{\beta}{\eta})(\frac{t}{\eta})^{\beta-1}(e^{-(\frac{t}{\eta})^{\beta}}) \tag{7}$$

Thus, probability plots depicted in Fig. 6 were replaced with 2-parameter equivalents, as presented in Fig. 7.

a)



b)

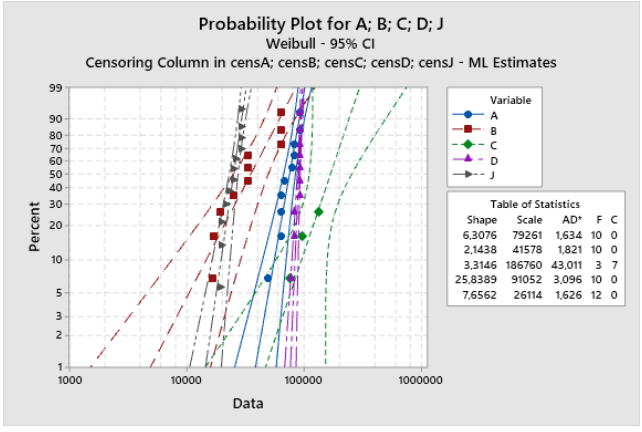


Fig. 7. Probability plots prepared for each tested sample set of SiC power MOSFETs, based on 2-parameter Weibull model assuming separate a) and common b) *shape* parameter

To identify material parameters given in Eqs. (5)-(6) a multiple linear regression was performed. The residual plot depicted in Fig. 8, indicated that:

- there was no correlation between residuals,
- usage of the LESIT model results in significantly higher estimation error than in the case of CIPS2008 model.

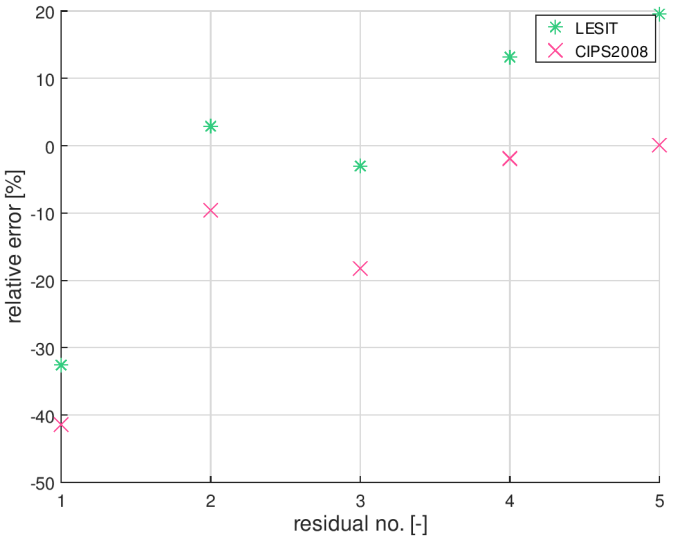


Fig. 8. Residual plot for Weibull distribution *scale* parameter estimators, based on LESIT and CIPS2008 models

The second conclusion was additionally confirmed when Mean Time To Failure (MTTF) of SiC power MOSFETs subjected to APC test was compared with developed models. As presented in Fig. 9 the LESIT, as well as the CIPS2008 models, offer satisfactory projection of laboratory test results. Thus, both models were found suitable for reliability modelling of SiC power MOSFET in $SOT-227B$ housing. However, a simplified form

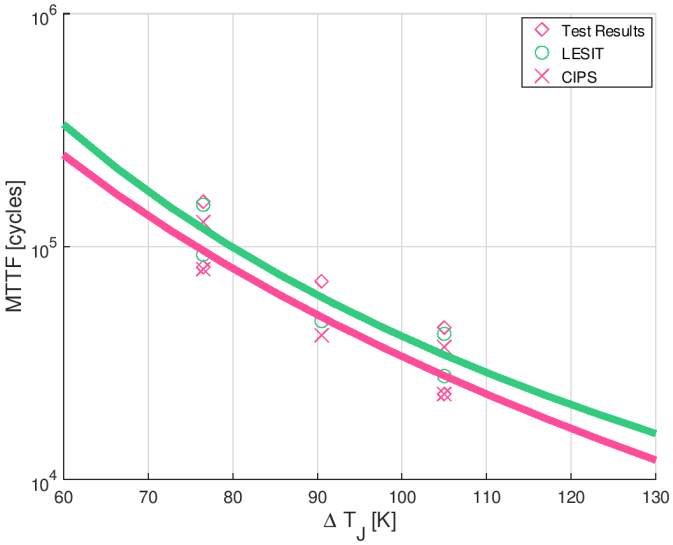


Fig. 9. Comparison of test results with MTTF for SiC power MOSFET estimated based on Weibull-LEST model and Weibull-CIPS model

of CIPS2008 equation was chosen for further evaluation of the universal reliability model. This decision was caused by fact that even simplified form of CIP2008 model cover higher amount of stress factors. The identified values of material constants and activation energy, corresponding to Eqs. (5)–(6) are listed in Table 5.

Table 5
Material constants identified for LESIT and CIPS2008 models

Parameter	*LESIT*	Parameter	*CIPS*2008
A	$1.65e15$	K	$3.37e13$
α	-5.96	β_1	-3.88
k_B	$1.38e-23$	β_2	31.73
E_A	$3.11e-25$	β_3	-0.82

Lastly, the MTTF curves for different junction temperature swing amplitudes and operating current values were identified. Both Fig. 10 and closer analysis of β_1 and β_3 parameters suggests that amplitude of junction temperature swing has significantly higher impact on power MOSFET reliability than the operating current. Furthermore, the PDF for SiC power MOSFETs subjected to various operating conditions were prepared with presented universal model (see Fig. 11). Based on such PDFs it is possible to calculate how failure rate changes over the time, or what is power MOSFET useful lifetime defined as mean value (same as MTTF), or so-called *BX life* – the time at which $X\%$ of MOSFETs will fail. These data may be further used in DfR procedure to estimate either railure rate or useful lifetime of high performance power converter.

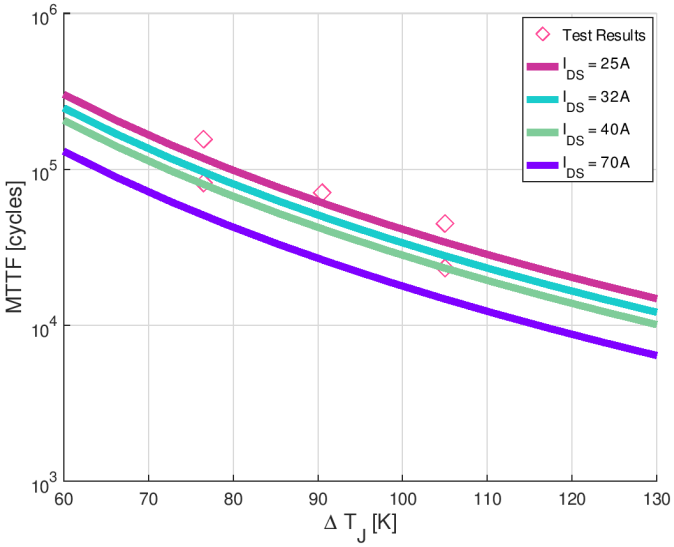


Fig. 10. MTTF estimation for SiC power MOSFETs subjected to power cycling at various operating conditions. The ambient temperature assumed in analysis is $40°C$

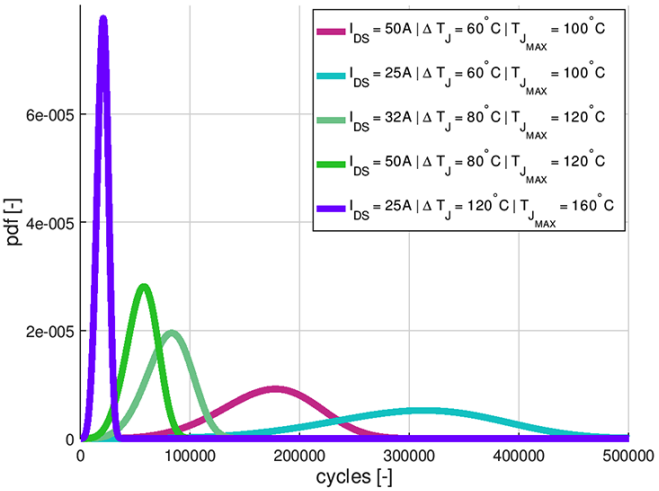


Fig. 11. Probability density functions derived for SiC power MOSFETs subjected to power cycling at various operating conditions

5. Conclusions

In this paper, a universal reliability model for SiC power MOSFET in *SOT* – 227*B* housing was presented. Beside universal model itself, a detailed description of procedure required to develop such model was also discussed. Proposed model offers great flexibility, as allows to determine the useful lifetime denoted as, e.g.,:

- time when pre-defined percentage of population will fail,
- time when PDF reaches pre-defined level,
- time when probability of failure reaches pre-defined level,
- and many others.

Thus, presented tool is found suitable for purposes of Design for Reliability procedure.

Moreover, following conclusions are given:

1. The Active Power Cycling test is suitable for analysis of *fatigue-like* failure modes.
2. The degradation caused by thermomechanical load, ends up in a fatal short-circuit, which is a crucial information for any designer of fault-tolerant power converter.
3. There was no correlation between position of bond wire, and probability of lift-off.
4. Weibull distribution is suitable for reliability modelling of *fatigue-like* failure modes.
5. Both CIPS2008 and LESIT models are suitable for modelling of fatigue-like failures for SiC power MOSFETs in *SOT* – 227*B*.

References

[1] S. Baba, W. Gajewski, M. Jasinski, M. Zelechowski, and M.P. Kaźmierkowski, "High performance power supplies for plasma materials processing", *IEEE Access* 9, 19327–19344 (2021).

[2] K. Fischer, K. Pelka, A. Bartschat, B. Tegtmeier, D. Coronado, C. Broer, and J. Wenske, "Reliability of power converters in wind turbines: Exploratory analysis of failure and operating data from a worldwide turbine fleet", *IEEE Trans. Power Electron.* 34(7), 6332–6344 (2019).

[3] S. O'Donnell, P. Wheeler, and A. Castellazzi, "Reliability analysis of sic mosfet power module for more electric aircraft motor drive applications", *2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles International Transportation Electrification Conference (ESARS-ITEC)*, 1–4 (2018).

[4] I. Vernica, H. Wang, and F. Blaabjerg, "Design for reliability and robustness tool platform for power electronic systems – study case on motor drive applications", *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 1799–1806 (2018).

[5] Y. Shen, A. Chub, H. Wang, D. Vinnikov, E. Liivik, and F. Blaabjerg, "Wear-out failure analysis of an impedance-source pv microinverter based on system-level electrothermal modeling", *IEEE Trans. Ind. Electron*. 66(5), 3914–3927 (2019).

[6] M. Bajerlein, M. Bor, W. Karpiuk, R. Smolec, and M. Spadło, "Strength analysis of critical components of high-pressure fuel pump with hypocycloid drive", *Bull. Pol. Acad. Sci. Tech. Sci*. 68(6), 1341–1350 (2020).

[7] W. Wang and D.B. Kececioglu, "Fitting the Weibull log-linear model to accelerated life-test data", *IEEE Trans. Reliab*. 49(2), 217–223 (2000).

[8] T. Tomaszewski, P. Strzelecki, M. Wachowski, and M. Stopel, "Fatigue life prediction for acid-resistant steel plate under operating loads", *Bull. Pol. Acad. Sci. Tech. Sci*. 68(4), 2300–1917 (2020).

[9] J. Zhang, Z. Qiu, E. Zhang, and P. Ning, "Comparison and analysis of power cycling and thermal cycling lifetime of igbt module", *2018 21st International Conference on Electrical Machines and Systems (ICEMS)*, 876–880 (2018).

[10] M. Dbeiss and Y. Avenas, "Power semiconductor ageing test bench dedicated to photovoltaic applications", *IEEE Trans. Ind. Appl*. 55(3), 3003–3010 (2019).

[11] T. Ziemann, U. Grossner, and J. Neuenschwander, "Power cycling of commercial sic mosfets", *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 24–31 (2018).

[12] E. Ugur, F. Yang, S. Pu, S. Zhao, and B. Akin, "Degradation assessment and precursor identification for sic mosfets under high temp cycling", *IEEE Trans. Ind. Appl*. 55(3), 2858–2867 (2019).

[13] S. Baba, A. Gieraltowski, M.T. Jasinski, F. Blaabjerg, A.S. Bahman, and M. Zelechowski, "Active power cycling test bench for sic power mosfets – principles, design and implementation", *IEEE Trans. Power Electron*. 36(3), 2661–2675 (2021).

[14] J. Liu, G. Zhang, B. Wang, W. Li, and J. Wang, "Gate failure physics of sic mosfets under short-circuit stress", *IEEE Electron Device Lett*. 41 (1), 103–106 (2020).

[15] U. Karki and F.Z. Peng, "Effect of gate-oxide degradation on electrical parameters of power mosfets", *IEEE Trans. Power Electron*. 33(12), 10764–10773 (2018).

[16] Y. Huang, Y. Luo, F. Xiao, and B. Liu, "Failure mechanism of die-attach solder joints in igbt modules under pulse high-current power cycling", *IEEE J. Emerg. Sel. Top. Power Electron*. 7(1), 99–107 (2019).

[17] S.-H. Ryu, "Sic power mosfet ruggedness", *ECPE Workshop: Power Semiconductor Robustness – What Kills Power Devices?*, ECPE, 1–1 (2020).

[18] J. Sun, J.Wei, Z. Zheng, Y.Wang, and K. J. Chen, "Short circuit capability and short circuit induced vth instability of a 1.2-kv sic power mosfet", *IEEE J. Emerg. Sel. Top. Power Electron*. 7(3), 1539–1546 (2019).

[19] U. Choi and F. Blaabjerg, "Separation of wear-out failure modes of igbt modules in grid-connected inverter systems", *IEEE Trans. Power Electron*. 33(7), 6217–6223 (2018).

[20] C. Zorn and N. Kaminski, "Acceleration of temperature humidity bias (thb) testing on igbt modules by high bias levels", *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, 385–388 (2015).

[21] IEC 60749-34 Ed. 1.0 b:2005, Semiconductor devices – mechanical and climatic test methods – part 34: Power cycling, American National Standards Institute (ANSI) (August 19, 2007).

[22] F. Wagner, G. Reber, M. Rittner, M. Guyenot, M. Nitzsche, and B. Wunderle, "Power cycling of sic-mosfet single-chip modules with additional measurement cycles for life end determination", *CIPS 2020; 11th International Conference on Integrated Power Electronics Systems*, 1–6 (2020).

[23] C. Schwabe, P. Seidel, and J. Lutz, "Power cycling capability of silicon low-voltage mosfets under different operation conditions", *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 495–498 (2019).

[24] C. Durand, M. Klingler, D. Coutellier, and H. Naceur, "Power cycling reliability of power module: A survey", *IEEE Trans. Device Mater. Reliab*. 16(1), 80–97 (2016).

[25] U. Scheuermann and S. Schuler, "Power cycling results for different control strategies", *Microelectron. Reliab*. 50(9), 1203–1209 (2010), 21st European Symposium on the Reliability of Electron Devices, Failure Physics and Analysis.

[26] M. Sathik, T.K. Jet, C.J. Gajanayake, R. Simanjorang, and A.K. Gupta, "Comparison of power cycling and thermal cycling effects on the thermal impedance degradation in igbt modules", *IECON 2015 – 41st Annual Conference of the IEEE Industrial Electronics Society*, 001170–001175 (2015).

[27] M. Thoben and M. Tuellmann, "Lifetime testing i (pc principles)", *ECPE Tutorial: Testing Automotive Power Modules According to the ECPE Guideline AQG 324* (2021).

[28] European Center for Power Electronics, "Qualification of power modules for use in power electronics converter units in motor vehicles", *ECPE Guideline AQG 324* (2019).

[29] V. Raveendran, M. Andresen, and M. Liserre, "Improving on-board converter reliability for more electric aircraft with lifetime-based control", *IEEE Trans. Ind. Electron*. 66(7), 5787–5796 (2019).

[30] B. Zhou, T. Lu, and J. You, "Study on fatigue ductility coefficient and life prediction for mixed solder joints under thermal cycle loads", *2014 10th International Conference on Reliability, Maintainability and Safety (ICRMS)*, 686–690 (2014).

[31] K. Okada, K. Kurimoto, and M. Suzuki, "Intrinsic mechanism of non-linearity in weibull tddb lifetime and its impact on lifetime prediction", *2015 IEEE International Reliability Physics Symposium*, 2A.4.1–2A.4.5 (2015).

[32] J. Ling, T. Xu, R. Chen, O. Valentin and C. Luechinger, "Cu and Al-Cu composite-material interconnects for power devices", *2012 IEEE 62nd Electronic Components and Technology Conference*, 1905–1911 (2012), doi: 10.1109/ECTC.2012.6249098.

[33] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of igbt modules – various factors influencing lifetime", *5th International Conference on Integrated Power Electronics Systems*, 1–6 (2008).