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Characterization of Al_2O_3/4H-SiC and Al_2O_3/SiO_2/4H-SiC MOS structures

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Abstract. The paper presents the results of characterization of MOS structures with aluminum oxide layer deposited by ALD method on silicon carbide substrates. The effect of the application of thin SiO_2 buffer layer on the electrical properties of the MOS structures with Al_2O_3 layer has been examined. Critical electric field values at the level of 7.5–8 MV/cm were obtained. The use of 5 nm thick SiO_2 buffer layer caused a decrease in the leakage current of the gate by more than two decade of magnitude. Evaluated density of trap states near the conduction band of silicon carbide in Al_2O_3/4H-SiC MOS is about of $1x10^{13}$ $eV^{-1}cm^{-2}$. In contrast, the density of the trap states in the Al_2O_3/SiO_2/4H-SiC structure is lower about of one decade of magnitude *i.e.* $1x10^{12}$ $eV^{-1}cm^{-2}$. A remarkable change in the MOS structure is also a decrease of density of electron traps located deeply in the 4H-SiC conduction band below detection limit due to using of the SiO_2 buffer layer.

Key words: aluminum oxide, MOS, silicon carbide, 4H-SiC, high-κ dielectrics.

1. Introduction

Due to excellent material properties of silicon carbide, such as high value of critical electric field, high electron saturation velocity and thermal conductivity, silicon carbide semiconductor devices are now frequently used in power electronics [1]. From the perspective of application, power MOSFET transistors with breakdown voltage over 1 kV are particularly desirable. Electrical parameters of the new generation of silicon carbide MOSFETs are not yet satisfactory [2]. This problem results from the high density of interface traps at the dielectric-semiconductor interface, which are formed during high temperature oxidation of silicon carbide. This significantly deteriorates electron mobility in the channel, which rarely exceeds 100 cm^2/Vs [3]. Simultaneously, within research on silicon carbide oxidation, works on applying high relative electric permittivity dielectrics (high-κ), such as hafnium oxide HfO_2 (ε_r = 15–25) or aluminum oxide Al_2O_3 (ε_r = 8–11) [4] in silicon carbide MOSFET technology have been carried out recently. Aluminum oxide has higher energy band gap (E_g ~ 7 eV) as compared to other high-κ dielectrics, which makes this material promising for application in 4H-SiC MOS power devices. However, due to relatively low value of barrier height between conduction bands of Al_2O_3 and 4H-SiC (φ_B ~ 1.5–1.6 eV), applying additional buffer layers is required to reduce gate leakage current markedly [5]. In addition, the buffer layer can also decrease the density of traps at dielectric-semiconductor interface [6]. In this work we present the results of the characterization of aluminum oxide layers grown by atomic layer deposition (ALD) method on 4H-SiC substrates, also on the substrate with thin SiO_2 buffer layer deposited by plasma enhanced chemical vapor deposition (PECVD) [7].

2. Experimental details

MOS structures used in this study were fabricated on low-resistivity 4H-SiC substrates ($n \sim 5\times10^{18}$ cm^{-3}) with n-type ($n \sim 5\times10^{15}$ cm^{-3}), 10 μm thick epitaxial layer. Prior to the MOS fabrication the substrates were cleaned in organic solvents and dipped in 10% HF solution to remove the native oxide. The nickel layer was sputtered on the backside and annealed (Ar, 1050°C) to form an ohmic contact. Two kinds of samples were fabricated. On one part of samples, 5 nm SiO_2 buffer layer was fabricated by PECVD using SiH_4 and N_2O plasma. Afterwards, a 50 nm layer of Al_2O_3 was deposited on all samples by ALD. Al_2O_3 layers were deposited at 200°C using trimethylaluminium (TMA) and water vapor (H_2O) as Al and O precursors, respectively. Finally, a top layer of Ti/Al gate electrode (φ = 200 μm) was deposited on top of Al_2O_3 by sputtering and patterned by lift-off technique. A schematic sketch of fabricated Al_2O_3/4H-SiC and Al_2O_3/SiO_2/4H-SiC structures is presented in Fig. 1.

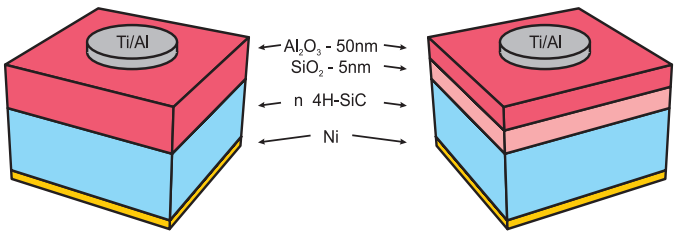

Fig. 1. Scheme of fabricated Al_2O_3/4H-SiC and Al_2O_3/SiO_2/4H-SiC MOS structures

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The surface morphology of aluminum oxide on 4H-SiC was examined by use of atomic force microscopy (AFM). Optical properties were determined using variable angle spectroscopic ellipsometry (VASE). Electrical characterization of fabricated MOS capacitors includes measurements of current-voltage (I–V) and capacitance-voltage (C–V) characteristics.

3. Results and discussion

3.1. Optical characterization and surface morphology. Optical properties of Al_2O_3 layer were determined by VASE. Optical parameters of the Al_2O_3 film were modeled using Tauc-Lorentz dispersion model. An excellent fit of model parameters to experimental data was obtained (the mean squared error MSE was 0.53, Fig. 2a). Based on VASE analysis, the wavelength dependence of refractive index and extinction coefficient were determined (Fig. 2b). The extinction coefficient was equal zero in studied wavelength range. The refractive coefficient values are typical for amorphous Al_2O_3 layers [8] and in 240–930 nm range it was decreasing approximately from 1.76 to 1.64. The thickness of Al_2O_3 film was determined to be 50.6 nm. Surface roughness (RMS) measured by means of AFM was about 0.46 nm, which indicates very good smoothness of ALD deposited Al_2O_3 films (Fig. 2c).

3.2. Electrical characterization. Figure 3 shows the measured current-voltage characteristics of Al_2O_3/4H-SiC and Al_2O_3/SiO_2/4H-SiC MOS structures. As can be observed, the leakage current of MOS structures without SiO_2 buffer layer is greater than in the case of buffer layer. For electric field E within the values up to 2 MV/cm or up to 3MV/cm, the leakage current is below noise level of the measurement setup for the case without or with the SiO_2 buffer layer, respectively. For E = 5 MV/cm leakage current of Al_2O_3/SiO_2/4H-SiC structures is over two orders of magnitude lower, and for E = 7.5 MV/cm over there orders of magnitude lower than in case of the Al_2O_3/4H-SiC structures. In comparison with hafnium oxide layers deposited by ALD on 4H-SiC, Al_2O_3 layers deposited directly on 4H-SiC have much larger value of critical electric field (E_c = 4.5 MV/cm for HfO_2), which stems from the larger barrier height between conduction

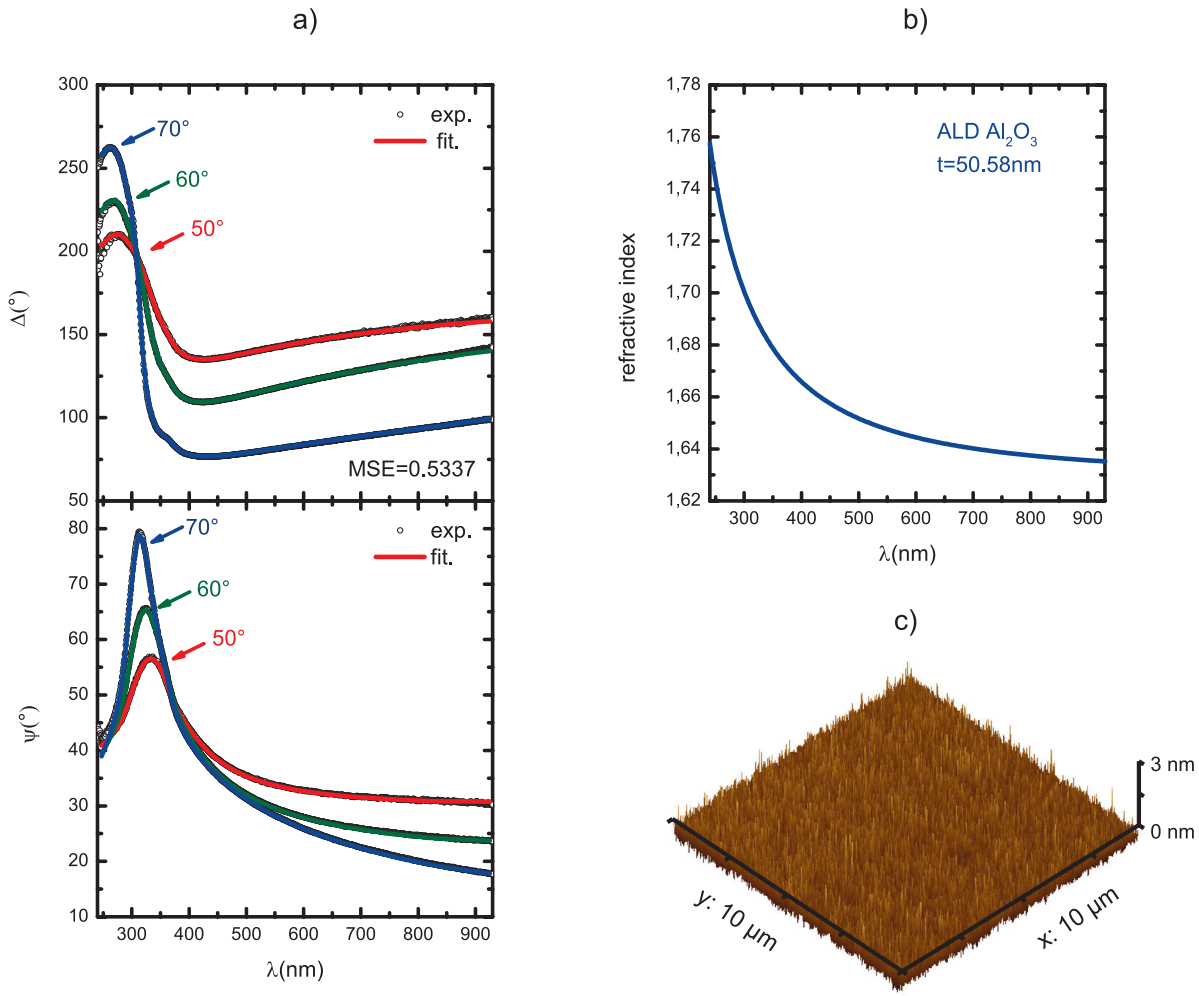

Fig. 2. a) Dependence of ellipsometric angles Ψ and Δ, b) the refractive index of Al_2O_3 layers deposited by ALD method, c) an AFM image of the surface of the Al_2O_3 film

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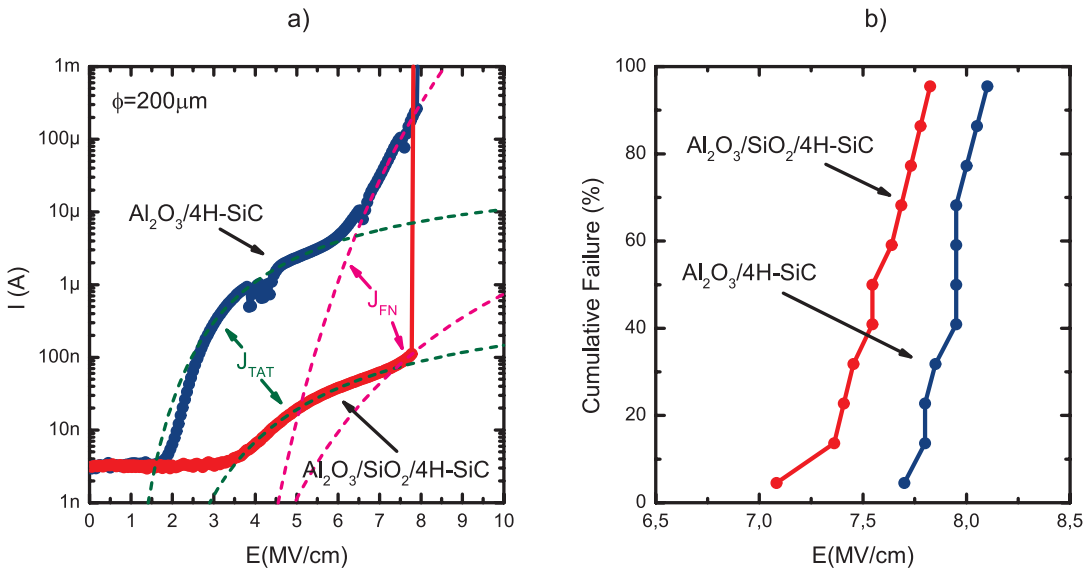

Fig. 3. a) Current-voltage characteristics, b) distribution of electric breakdown probability of Al_2O_3/4H-SiC and Al_2O_3/SiO_2/4H-SiC MOS structures

band of the dielectric and semiconductor. Similarly, for Al_2O_3/SiO_2 gate stack the critical electric field is higher by approximately 1 MV/cm than in the case of HfO_2/SiO_2 with the same buffer layer thickness [7].

Based on current-voltage characteristics, conduction mechanism of the leakage current in each of the structure was determined. For electric field E within the values up to about 6 MV/cm for Al_2O_3/4H-SiC and up to 7 MV/cm for Al_2O_3/SiO_2/4H-SiC structures the best fits to experimental data were obtained by using formula describing trap-assisted tunneling current (J_{TAT}) [9]:

$$J_{TAT} = A\exp\left(\frac{-8\pi\sqrt{2qm^*}}{3hE}\varphi_t^{3/2}\right), \qquad (1)$$

where A is constant, m^* is electron effective mass in Al_2O_3, h is Planck constant and φ_T is trap energy level with regard to conduction band edge of the dielectric. The energy of traps in case of Al_2O_3/4H-SiC and Al_2O_3/SiO_2/4H-SiC MOS structures was 0.38 and 0.46 eV. For electric field values above 6 MV/cm and 7 MV/cm, the dominant leakage current mechanism is tunneling through triangular barrier, i.e., tunneling in Folwer-Nordheim regime (J_{FN}). The leakage current associated with Fowler-Nordheim tunneling is described by the following formula [9]:

$$J_{FN} = \frac{q^2}{8\pi h\varphi_B}E^2\exp\left(\frac{-8\pi\sqrt{2qm^*}}{3hE}\varphi_B^{3/2}\right), \qquad (2)$$

where q is elementary charge and φ_B is barrier height between conduction bands of dielectric and semiconductor. Determined φ_B values are 1.56 eV and 1.52 eV for the structures with and without SiO_2 buffer layer, respectively. These values are close to values for Al_2O_3 and 4H-SiC reported in the literature [10]. Obtained critical electric field values were about 7.5–8 MV/cm. For the MOS structure without SiO_2 buffer layer E_c is slightly higher (0.5 MV/cm) than in the case with SiO_2 buffer layers. This might be altered by uncertainty of electric field values. However, quite similar critical electric field values indicate that electric breakdown occurs in the Al_2O_3 layers for both type of structures.

The C–V characteristics were measured at 1 MHz frequency. Due to the substantial shift of the measured C–V characteristics as a function of measuring voltage caused by the presence of significant charge in the gate stack or the high level of electrons trapped at the dielectric-semiconductor interface, we adopted the following methodology of measurements. The first measurement is made from accumulation to depletion and back. This step was preceded by a 5 minute voltage stress (–30 V) aiming at least partially discharge slow traps states and/or reduce the impact of mobile charge on the measured characteristics. From these measurements the energetic distribution of fast traps states near conduction band using Terman method [11] was extracted. Next, 5 min positive voltage stress (30 V) was performed and C–V characteristics were measured from accumulation to depletion and back. From shift of C–V curves measured under both conditions, the amount of slow states and fixed and mobile charge in the dielectric can be evaluated. Figure 4a shows measured C–V characteristics of Al_2O_3/4H-SiC and Al_2O_3/SiO_2/4H-SiC MOS capacitors. Calculated relative dielectric constant of Al_2O_3 was about 9. As follows from C–V measurements, the capacitor measured for the first time was characterized by relatively low flat band voltage. However, after voltage stress went into accumulation range, the flatband voltage was significantly shifted towards more positive values. This is due to trapping of carriers by high concentration of near interface traps. In case of the MOS structures with SiO_2 buffer layer this phenomenon is significant-

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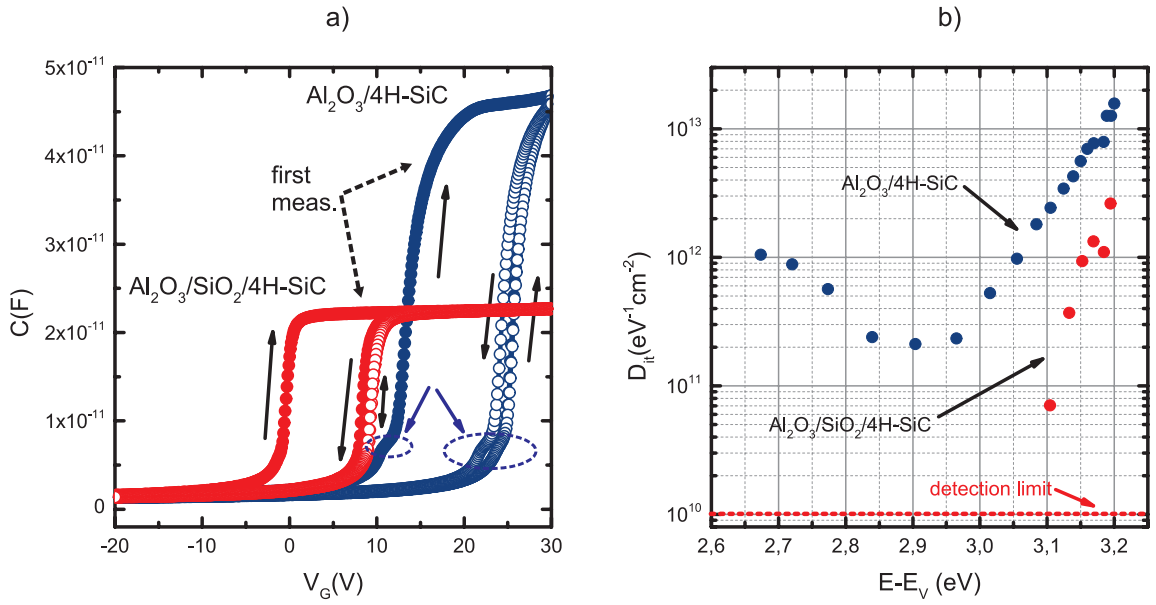

Fig. 4. a) Capacitance-voltage characteristics of Al_2O_3/4H-SiC and Al_2O_3/SiO_2/4H-SiC MOS structures, b) energy distribution of the density of surface states at dielectric-semiconductor interface based on capacitance-voltage characteristics

ly reduced. This indicates that trapping occurs in Al_2O_3 layer, and the use of even 5 nm thick SiO_2 buffer layer decreases this phenomenon by moving the trapping centers from semiconductor surface. By analyzing the energetic distribution of traps states at the dielectric-semiconductor interface (Fig. 4b), it can be seen that in the case of Al_2O_3/4H-SiC structures the density of interface traps (D_{it}) near the conduction band was about $1.5\times10^{13}\,eV^{-1}cm^{-2}$ (for $E–E_v = 3.2$ eV), and was almost an order of magnitude higher than in the case of Al_2O_3/SiO_2/4H-SiC structures ($D_{it} = 2.6\times10^{12}\,eV^{-1}cm^{-2}$, $E–E_v = 3.2$ eV). Moreover, in the case of structures with SiO_2 buffer layer, a rapid decrease of D_{it} in function of the distance from the conduction band edge can be observed. For trap states with $E–E_v$ located within up to 3.1 eV above the valence band edge, interface traps density falls below the detection limit of Terman method (~ $10^{10}\,eV^{-1}\,cm^{-2}$). In the case of Al_2O_3/4H-SiC MOS structures, the increase in the density of trap states located deeper in the band gap of 4H-SiC can be seen, which is manifested by increase of C–V characteristics (marked by circles in Fig. 4a). As compared to the literature data relating to Al_2O_3/SiO_2/4H-SiC structures with a SiO_2 buffer layer formed by thermal oxidation of 4H-SiC [12], the Al_2O_3 MOS structures with similar thickness of SiO_2 layer deposited by PECVD are characterized by much faster decrease of the density of interfaces traps located in the depth of the band gap of 4H-SiC. For Al_2O_3/SiO_2 layers presented in [12], the density of interface states does not fall below $1\times10^{12}\,eV^{-1}cm^{-2}$ to 0.5 eV from conduction band edge.

4. Conclusions

The results of characterization of atomic layer deposited aluminum oxide on silicon carbide for MOS structures are presented. Fabricated MOS structures with and without thin SiO_2 buffer layer are characterized by very high critical electric field values in range 7.5¸ 8 MV/cm. The use of 5 nm thick SiO_2 buffer layer causes decrease of gate leakage current by at least two-orders of magnitude in comparison to Al_2O_3 layers on bare 4H-SiC. Analysis of C–V measurements related to the dielectric-semiconductor interface shown that by the application of the (5 nm) SiO_2 buffer layer interface traps density near conduction band of 4H-SiC can be decreased almost by an order of magnitude from 1×10^{13} to $1\times10^{12}\,eV^{-1}\,cm^{-2}$. Moreover, the density of traps located deeper in the 4H-SiC bandgap decreased below $1\times10^{10}\,eV^{-1}\,cm^{-2}$, i.e. the value undetectable by Terman method applied in this work.

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