Verilog-A Inductor Compact Model for the Efficient Simulation of Class-D VCOs

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***Abstract*—This paper presents the use of a Verilog-A compact model for integrated spiral inductors, for the simulation of Class-D CMOS oscillators. The model takes into consideration the geometric parameters characterizing the inductor layout, as well as the technological parameters. The accuracy of the model is checked against simulations with ASITIC simulator and limitations of the model are established. The model is integrated into Cadence environment, offering the designer the possibility to efficiently simulate radio frequency blocks considering the non-idealities of both the inductors and the transistors in nanometric technologies. The particular case for a class-D oscillator is illustrated.**

***Index Terms*—Verilog-A, RF modeling, tapered Inductor, Class D Oscillator**

I. INTRODUCTION

THE use of nanometric technologies requires the extensive use of modern design automation (EDA) environments, where dedicated compact models support accurate simulation results. The need for developing compact models capable of accurately coping with the ever-evolving semiconductor devices has motivated the widespread use of Verilog-A. Over the last decade, Verilog-A has been used for the implementation of MOSFET transistor models in deep-submicron/nanometric technologies [1-4], among others. Verilog-A as well as Verilog-AMS have also been used in the development of behavioural models for high-level characterization of RF/analog building blocks such as operational amplifiers [3], sigma-delta modulators [4], [5], or phase-locked-loops [6] .

The rapid evolution of technologies where devices are migrating towards nanometric sizes, and capable of operating at higher frequencies in the Giga-Hertz range has motivated the widespread development of fully integrated RF building blocks for wireless communications, where power efficiency is a major concern. In the particular case of voltage controlled oscilators for wireless applications, the availability of MOSFET switches with excellent conductivity, enabled the design of class-D oscillators [7]. These oscillators offer the possibility of lowering both the phase noise and supply voltage as required by modern mobile communication systems. For the maximization of oscillator phase noise, however, designing the needed high quality integrated inductors is still a challenging task. Over the last decade, EDA tools have shown a strong commitment to offer designers the possibility for obtaining circuits characterization in an accurate and effective way. Although accurate models for active devices are made available for each new technology, the characterization of passive devices, such as integrated inductors, is still very limited. Designers usually choose an inductor from the set of solutions offered by the technology, and then optimize the RF building block for the inductor chosen. This solution, however, does not offer the possibility for exploring the entire design space, since no optimization of the inductor parameters is performed. It is, therefore, of paramount importance for the designers, to have the possibility for efficiently characterizing both passive and active circuit elements in the same design environment, so that the overall optimization of such RF/analog circuits as LNAs or VCOs may be obtained.

This paper describes a Verilog-A model for integrated inductors. In Section II the lumped element inductor model is introduced, and the equations for evaluating each element values are presented. The equations considered take into account the geometric parameters of each segment of the integrated inductor, thus enabling the characterisation of tapered devices. The model implementation in Verilog-A is described in Section III, where the validity of the model is also discussed. Finally the design of integrated inductors with the Cadence optimization tool is described, and limitations of results are pointed out. In Section IV an application example considering the simulation of a class-D LC-oscillator employing the inductor model is presented. Finally, conclusions are offered in Section V.

II. INTEGRATED INDUCTOR MODEL

Obtaining accurate inductor design solutions where the technology losses are minimized makes imperious the use of optimization-based methodologies. The need for evaluating the inductor behavior in the optimization loop makes the use of electromagnetic simulators timely prohibitive. To efficiently characterize integrated inductors behavioral models have been proposed. Over the last decade several integrated inductor models have been proposed as a way of offering designers the possibility of characterizing the device behavior in an accurate and efficient way. The most widely used is the π-model [8], represented in Fig. 1.

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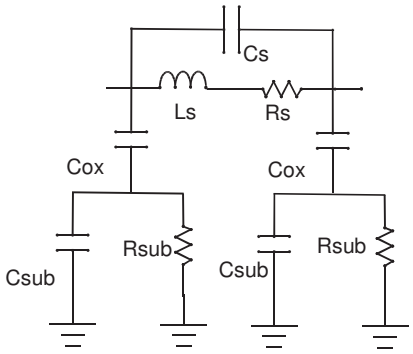

Fig. 1. Integrated inductor Pi-model.

For the evaluation of the model parameter values, expressions in [9] may be used. For the determination of the series inductance, *Ls*, however, more complex expressions, as proposed in [10], for accurately modelling non-square or tapered inductors should be adopted. In this approach the overall inductance is obtained taking into consideration the self-inductance of each segment comprising the inductor, as well as the mutual inductances between each pair of segments. Considering the octagonal inductor represented in Fig. 2 the overall series inductance, *Ls*, is obtained with

$$L_s = L_1 + \cdots + L_{25} + 2\left(M_{1,9} + .. + M_{17,25}\right) - 2\left(M_{1,5} + .. + M_{21,25} + M_{1,2} + .. + M_{24,25}\right). \quad (1)$$

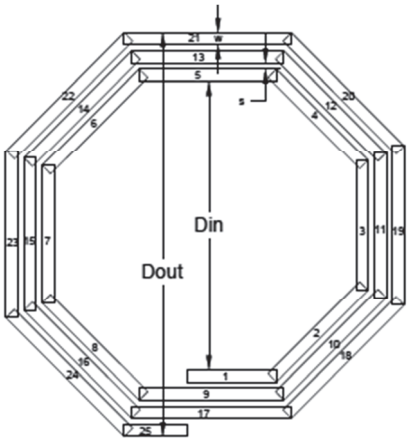

Fig. 2. Octagonal inductor

The self-inductance, L_i, of each segment, i, may be evaluated with

$$L_i = 2l_i\left(ln\left(\frac{2l_i}{w_i + t}\right) + 0.50049 + \left(\frac{w_i + t}{3l_i}\right)\right). \quad (2)$$

Considering l_i the length, w_i the width and t the thickness of segment i. The mutual inductance, M_{ij}, between parallel segments, i and j, is evaluated with

$$M_{ij} = 2l_i\left(ln\left(\frac{l}{\mathrm{d}} + \sqrt{1 + \left(\frac{l}{\mathrm{d}}\right)^2}\right) - \sqrt{1 + \left(\frac{d}{\mathrm{l}}\right)^2} + \frac{d}{\mathrm{l}}\right). \quad (3)$$

where, d, is the geometric mean distance between the two segments, i and j. The geometric mean distance between parallel segments is evaluated considering

$$ln(d) = ln(p) - \frac{w^2}{12p^2} - \frac{w^4}{60p^4} - \frac{w^6}{168p^6} - \frac{w^8}{360p^8} - \frac{w^{10}}{660p^{10}}. \quad (4)$$

where p is the pitch of the two wires and w is the width of the segments considered.

The mutual inductance between any two non-parallel segments, as illustrated in Fig. 3 , may be obtained with

$$M_{ij} = 2\cos(\varepsilon)\left((\mu + l)\tanh^{-1}\left(\frac{m}{R_1 + R_2}\right) + (\nu + m)\tanh^{-1}\left(\frac{l}{R_1 + R_2}\right) - \mu\tanh^{-1}\left(\frac{m}{R_3 + R_4}\right) - \nu\tanh^{-1}\left(\frac{m}{R_2 + R_3}\right)\right). \quad (5)$$

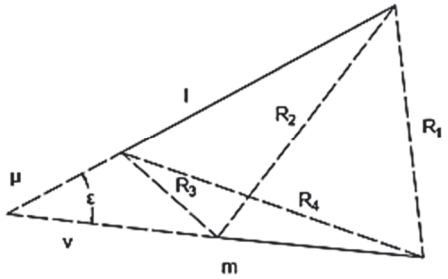

Fig. 3. Generic case for non-parallel segments

III. VERILOG-A MODEL

In the particular case where integrated inductors to be used in RF building blocks to be implemented in deep sub-micrometric or even nanometric technologies is envisaged, simulation in an electrical simulator, e.g., Cadence Spectre, must be considered as a way of granting the accurate characterization of the active devices for the technology chosen. The implementation of the above considered inductor model in Verilog-A makes use of the functions for the evaluation of the self-inductance and the mutual inductance between segments illustrated below.

The Verilog-A code implementation for the evaluation of the series inductor, *Ls,* was integrated into Cadence environment.

The implemented model also accounts for tapered inductors, considering the width, w_i, for each segment, i, is given by

$$w_i = w_1 + \left(w_f - w_1\right)\frac{i - 1}{(kn - 1)}, \quad (6)$$

where $w_{1(f)}$ is the width of the first (last) segment, n is the number of turns and k accounts for the polygonal shape of the inductor.

The results obtained for non-tapered inductors were compared against simulation with ASITIC simulator, and are represented in TABLE I.

```
// VerilogA inductance evaluation
function real selfind;
input l,w,t;
real l,w,t;
  selfind=2*l*1e-7*(ln(2*l/(w+t))+0.50049+(w+t)/(3*l));
endfunction

function real Gmd;
//evaluates geometric mean distance
input w,p;
real w,p,wp;
begin
   wp=w/p;
  Gmd=ln(p)-pow(wp,2)/12-pow(wp,4)/60-pow(wp,6)/168-
pow(wp,8)/360-pow(wp,10)/660;
Gmd=exp(Gmd);
end
endfunction

function real mpindx;
// mutual inductance parallel same length
input l,p;
real l,p;
real d, l1,d1;
begin
  d=Gmd(l,p);
  l1=l/d;
  d1=d/l;
  mpindx=2*l*1e-7*(ln(l1+pow((1+pow(l1,2)),0.5))-
pow((1+pow(d1,2)),0.5)+d1);
end
endfunction

function real mutualpInd;
// mutual inductance parallel
input p,m,q,pitch ;
real  p,m,q,pitch ;
begin
  if (q==0.0)
    mutualpInd=mpindx(m+p,pitch)-mpindx(p,pitch);
else
    mutualpInd=(mpindx(m+p,pitch)+mpindx(m+q,pitch)-
(mpindx(p,pitch)+mpindx(q,pitch)));
end
endfunction

function real mutualnpInd;
input ep,miu,niu,l,m,R1,R2,R3,R4;
real ep,miu,niu,l,m,R1,R2,R3,R4;

begin
  mutualnpInd=(miu+l)*atan(m/(R1+R2))
+(niu+m)*atan(l/(R1+R2))-miu*atan(m/(R3+R4))-
niu*atan(m/(R2+R3));
 mutualnpInd=2*cos(ep)*1e-7*mutualnpInd;
end
endfunction
```

Results for tapered square inductors were also obtained and are represented in TABLE II, where only square inductors are presented, due to limitations of the ASITIC simulator when tapered devices are to be simulated.

TABLE I
SERIES INDUCTOR VALUE FOR UMC130 INDUCTORS WITH 340X340μM^2 AND W=10μM

Shape	N_turns	Ls_Verilog [nH]	Ls_Asitic [nH]
Square	2	3.28	3.29
	3	6.05	6.07
	4	9.02	9.06
Hexagonal	2	2.18	2.19
	3	3.93	3.93
	4	5.70	5.70
Octagonal	2	2.34	2.34
	3	4.24	4.24
	4	6.21	6.21

TABLE II
SERIES INDUCTOR VALUE FOR UMC130 INDUCTORS

N_turns	Dout [μm]	w_1 [μm]	w_f [μm]	s [μm]	Ls_Verilog [nH]	Ls_Asitic [nH]
2	300	5	10	2.5	3.00	3.00
3	300	5	10	2.5	5.64	5.64
4	300	5	10	2.5	8.56	8.68
2	400	5	15	4.5	3.98	3.98
3	400	5	15	4.5	7.35	7.43
4	400	5	15	4.5	11.10	11.23
2	350	10	35	7.0	3.40	3.38
3	350	10	35	7.0	5.64	5.67
4	350	15	35	7.0	7.48	7.57

A. Integrated Inductor Compact Model

The integrated inductor compact model implemented in Verilog-A is illustrated below, where the evaluation of the series inductance, *Ls*, is obtained with the previously presented function.

```
// VerilogA pi-model
`include "constants.vams"
`include "disciplines.vams"
module inductor(a,b);
inout a,b;
electrical a,b,c,d;
branch (a,b) bserie;
branch (a,b) bcap;
// … Declare technological parameters
…..
// … Declare Lumped element variables and freq.
……
// initialization of geometrical parameters
parameter real n=1;
……
analog begin
t=2e-6;
s=5e-6;
miu= 4*3.14*1e-7;
E0=8.854187817e-12;
Eox=4*E0;
Esub=11.9*E0;
tox=5.42e-6;
……
dout=dinx+(2*n+1)*wx+(2*n-1)*s;
davg=0.5*(dout+dinx);
ratio=(dout-dinx)/(dout+dinx);
R0=(10e-3)*t //Rsheet=10e-3;
```

```
sigma=sqrt(R0/(3.14*miu*freq);
teff=(1-exp(-t/sigma));
Rs=(R0*l)/(wx.teff*sigma);
toxMund=tox-tund-4.76e-6;
Cs=(n-1)*wx*wx*Eox/toxMund;
//evaluate Ls, Cox, Rsub,Cub
…
//topological description of Pi model

I(d)<+ V(d)/Rsub + Csub*ddt(V(d));
I(a,d)<+ Cox*ddt(V(a,d));
I(c)<+ V(c)/Rsub + Csub*ddt(V(c));
I(b,c)<+ Cox*ddt(V(b,c));
V(bserie)<+ Ls*ddt(I(bserie)) + Rs*I(bserie);
I(bcap)<+ Cs*ddt(V(bcap));
 end
```

B. Comparison between Tapered and Fixed Width Inductors

In the first examples the frequency response of a fixed width against a tapered inductor with output diameter of 350µm is considered. In both cases the frequency behavior of the inductance and quality factor are illustrated in Fig. 4.

The case for a fixed width square inductor with two turns, and metal width, w=7 µm, is represented in blue. In red, the behavior of a tapered inductor with a metal width between 5 µm and 35 µm and 2.5 turns is represented. As can be easily concluded, for similar inductance value and area, the tapered device offers a significant improvement in the quality factor. It is to be noted, however, that this enhancement in the quality factor is obtained at the expense of a significant reduction in the resonance frequency of the inductor. This is due to the fact that having metal stripes with larger width at the outer turns will increase the parasitic capacitances.

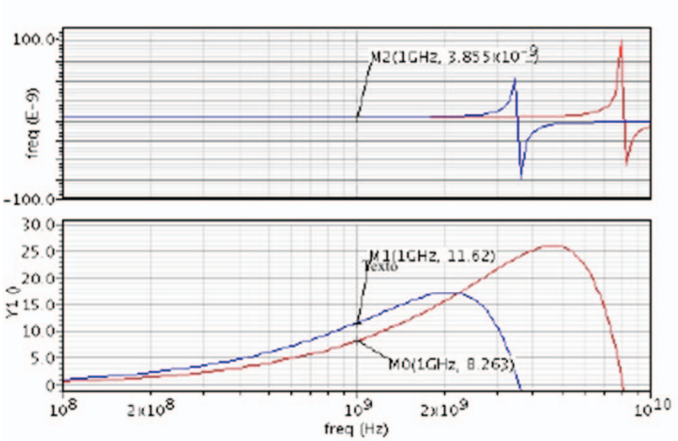

Fig. 4. Frequency behavior of fixed-width and tapered inductor

C. Inductor Optimization

The availability of the inductor model in the Cadence environment offers the possibility for designing inductors using the optimization tool. The case for a 6nH inductor is illustrated below, where constraints on the output diameter, and metal width were given, according to

$$350\ \mu m \le D_{out} \le 800\ \mu m$$
$$5\ \mu m \le w \le 40\ \mu m \qquad (7)$$

Results obtained for square, hexagonal and octagonal inductors are represented in TABLE III. From the solutions obtained, a few conclusions may be driven, e.g.: The quality factor increases with the number of turns of the inductor as well as with the number of sides of the polygonal shape. The output diameter is smaller for the square inductor and maximum for the hexagonal inductor.

It is to be noted, however, that the results obtained reflect some limitations from the optimization tool used, where different steps for each variable cannot be considered. In the particular case for the number of turns, optimization was performed for the different number of turns considering a step of half turn. Moreover, the step for the width, *w*, as well as the output diameter, D_{out}, should obey constrains imposed by the technology. To overcome this limitation the values obtained for the width and the output diameter should be rounded to the nearest value allowed by the technology.

TABLE III
OPTIMIZATION RESULTS FOR A 6NH INDUCTOR

n	Square / hexagonal / octagonal			Results
2	5.996	5.981	5.981	Inductance (@1GHz)
	10.96	12.17	12.27	Quality Factor(@1GHz)
	542.9	784	690.1	Dout (µm)
	12.08	17.06	14.41	W (µm)
2.5	5.999	5.968	5.981	Inductance (@1GHz)
	12.28	14.01	14.46	Quality Factor(@1GHz)
	416	618	544	Dout (µm)
	12.5	18.91	16.24	W (µm)
3	5.981	5.979	5.995	Inductance (@1GHz)
	14.54	16.26	17.76	Quality Factor(@1GHz)
	378.7	573.4	494.8	Dout (µm)
	15.44	28.25	20.95	W (µm)
4	5.887	5.981	5.973	Inductance (@1GHz)
	17.93	18.17	19.45	Quality Factor(@1GHz)
	353.2	537.8	414.1	Dout (µm)
	21.37	32.08	23.33	W (µm)

IV. APPLICATION EXAMPLE

In this section an application example considering the design of 1.0 GHz class-D *LC*-oscillator, using the topology represented Fig. 5 is addressed. The main advantage of this class-D oscillator stems from the non-existence of a tail NMOS current source, which reduces the maximum output voltage swing. This limitation may be extremely severe for new technologies where the supply voltage is lower than 1.2V.

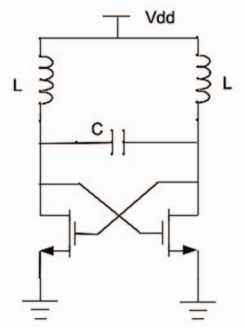

Fig. 5. Class-D oscillator

According to [7] the theoretical value for peak amplitude of the single-ended output voltage is given by

$$V_{peak} = V_{DD}\left(1+\sqrt{\frac{\alpha^2\pi^2}{4}+1}\right) \approx 3.27V_{DD}. \quad (8)$$

The oscillation frequency, considering a single-ended operation is given by

$$f = \frac{1}{2\pi\alpha}\sqrt{\frac{1}{LC_{eq}}}. \quad (9)$$

where $\alpha \approx 1.3$ and C_{eq} should account for the tank capacitance, C, and the parasitic capacitances of the MOSFETS implementing the switches.

In this example the UMC130 technology was considered. The switches were implemented with W/L=7.2u/129n, and a tank capacitance of 4pF is used. An inductor of 3nH and a supply voltage of 0.8V were considered.

The single-ended output voltage waveforms obtained are represented in Fig. 6. Two cases are represented. In blue, the output voltage waveform for an oscillator with ideal inductors is represented. An oscillation frequency of 1.079GHz and a peak voltage of 2.402V are obtained. The red waveform corresponds to the case where the Verilog-A model for the non-ideal inductor is used. An octagonal inductor with three turns is considered. In this case the oscillation frequency is reduced to 0.742GHz and a peak voltage of 2.24V is observed.

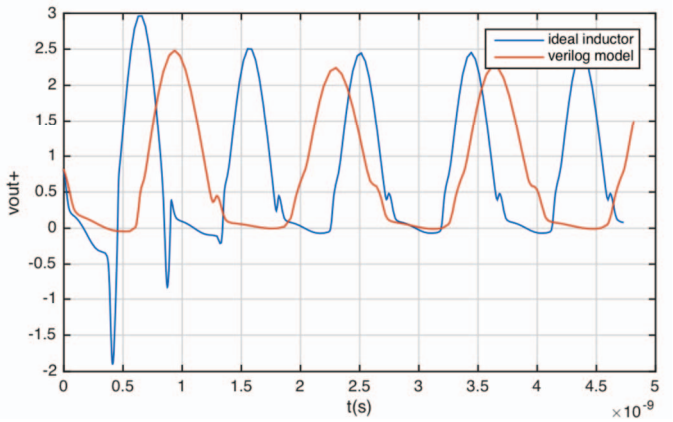

Fig. 6. Single-ended output voltage waveform in Class-D oscillator

V. CONCLUSIONS

This paper presented the implementation in Verilog-A of a compact model for integrated square, hexagonal or octagonal inductors. The model considers as input parameters the geometrical characterization of the inductor, and offers the possibility for characterizing both fixed width and tapered inductors. Results obtained with the model were validated against simulations with ASITIC. The frequency behavior of a tapered inductor against a fixed-width inductor was presented, illustrating the benefits/limitations of each design option. The design of inductors, using the model developed, in the CADENCE optimization tool was also presented. Finally, the example for the design of a 1.0 GHz class-D LC-oscillator, using the inductor model was described. Results were compared against simulation with ideal inductors and show that using simple behavioral Verilog-A model offers an efficient way of obtaining a first design, where the parasitic capacitances and losses of the tank are taken into account.

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