Power-saving Voltage-to-Current Conversion with the Use of CMOS Differential Amplifier

Ryszard Wojtyna

***Abstract*—Differential amplifiers are well known as input stage preamplifiers. This is because they exhibit the ability to reduce unwanted common-mode effects considerably. As a consequence, both noise and input signal of the amplifier can have low values. Proper operation of differential amplifiers is possible when implemented in chip form. For typical use of such CMOS amplifiers, input signals are delivered to differential-pair gate-terminals while tail terminal is used to ensure the required bias of the pair. The paper shows that the roles of gates and tail terminal can be changed. In other words, the tail current can be used as input signal while the gate ones as voltages controlling the amplifier gain. This enables to combine the achievable low noise with power efficient operation of the circuit. Necessary conditions for that are discussed in this paper. Suitability of atypically used differential amplifiers for voltage-to-current conversion is explained. Two examples of CMOS circuits implementing power economic conversion of this type are presented.**

***Index Terms*—Analog signal processing, differential amplifiers, CMOS electronics, low-power analog circuits**

I. Introduction

RECENTLY, one observes a growing interest in applying analog techniques to solve different signal processing tasks. This takes place in such science and research areas like artificial neural networks, sensor techniques, wireless telecommunications, medical diagnosis and others [1]-[11]. The reason for the increase in the analog technique popularity is because such a processing introduces new values and becomes either a valuable and sometimes necessary complement to what digital electronics offers. Advances in CMOS processes, resulting in enlarging integration scale of chips, create new possibilities of on chip signal processing. The increased number of transistors extends possibilities of implementing analog electronics within a chip considerably. However, the interest for using analog electronics is mainly due to the well known restrictions of digital technique. We can mention here situations when digital circuits are not sufficiently fast, when consume too much energy or occupy too big chip area. These drawbacks result, first of all, from sequential character of digital signal processing. Another factor negatively affecting the digital processing is a rather low clock frequency achievable. Its increase is very low, if any. This is observed for many years in standard digital systems.

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As for the new analog CMOS electronics, there are different ways to utilize possibilities offered by chip implementations. One can mention here two solutions. The first one is based on CMOS inverters [7], known from digital circuits. The other one uses differential amplifiers combined with current mode techniques [12]-[14], known from analog microelectronics. The main aim of the performed research in this field, outcomes of which are discussed here, is to utilize existing potential of the second technique in order to reduce power consumption and enlarge efficiency of on-chip signal processing.

In this paper, voltage-to-current conversion is the subject of consideration. The need for such a conversion results from the fact that on chip analog electronics is built of both voltage and current mode circuits. There are essential reasons for applying two modes, voltage and current, of analog on-chip signal processing. Firstly, to ensure low power losses in relatively long conducting paths, voltage mode operation should be applied. In some sense, this is like in electrical power grids. Secondly, if the signal is processed locally, current mode operation is superior to the voltage mode one as regards the power consumption minimization [9], [12]. The simplest way of realizing voltage-to-current conversion is to use a single MOS transistor. Unfortunately, such conversion is strongly nonlinear, which deeply restricts its usefulness. In this paper, new approach to this problem is proposed.

II. Atypical Use of Differential Amplifier

To explain the proposed circuit usefulness, consider the basic differential amplifiers shown in Fig.1. The upper circuit, denoted by *a*), is based on a *p*-channel MOS transistor, while the bottom, denoted by *b*), uses an *n*-channel MOS pair. In principle, operation of both amplifiers is the same. As a result, one can apply a common description to both amplifiers.

Typically, the I_T tail current shown in Fig. 1 is used to bias the M1-M2 pair, while the V_1 and V_2 voltages are input signals, whose difference is to be amplified. Then, the power consumed by the circuit is different from zero continuously, which is its disadvantage. To reduce the power losses, one can use the tail current as input signal and the V_1, V_2 voltages as parameters controlling the amplifier gain. In such a case, if the input current drops to zero, or becomes less than some threshold level, the power consumption also goes to zero.

This, in case of pulsed signals, can reduce the total power consumption significantly, like it is the case in digital CMOS circuits. Even though the proposed solution eliminates two input signals (V_1 and V_2), retaining only the I_T tail current, the differential amplifier exhibits the ability to reject so call common effects, like in the case of standard differential amplifiers. As a consequence, the proposed amplifier with I_T as atypical input signal is well suited for small signal operations, similarly as in typical operational amplifier. It is worth emphasizing that input signal of the amplifier not necessary must be the I_T current, like in Fig. 1. A single voltage can also be used as the input one if at the circuit input proper voltage to current conversion is performed. Moreover, it is also possible to cut off supply power from the V_1, V_2 voltage sources. This reduces the total power consumption additionally.

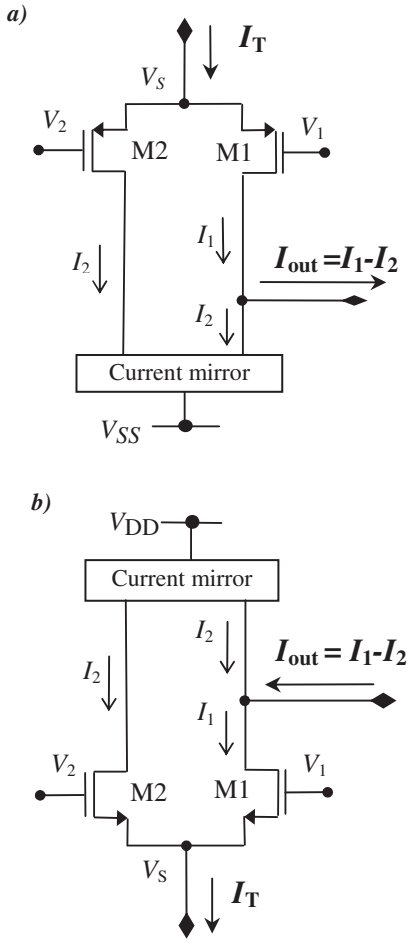

Fig. 1. Basic structures of the applied differential amplifier based on: *a) p*-channel MOS-transistor differential pair (upper), *b) n*-channel MOS-transistor differential pair (bottom).

The rest of the paper is organized as follows. Simple realization of voltage to current converter based on the diagram *a*) of Fig. 1 is presented in Section 3. Section 4 shows the idea of reducing to zero the total power taken from the circuit supply rail. Simplified theoretical description of the problem is given in Section 5. CMOS realization of very power-efficient voltage to current converter based on the diagram of Fig. 4 is presented in Section. 6. In Section 7, simulation results are discussed. Concluding remarks are gathered in Section 8.

III. Simple Voltage to Current CMOS Converter

Fig. 2 present a detailed diagram of a simple voltage-to-current converter that realizes the idea given by diagram *a*) in Fig. 1. The current mirror at the bottom is built of only two transistors, namely the M3 and M4 ones. At the top of Fig. 2, three transistors, denoted by M5, M6 and M7, are used to realize a simple voltage to current conversion. Since the atypically used differential amplifier operates in current mode and the voltage to current characteristic of M7 (when operating is strong inversion and in saturation) is quadratic, the total V_{in} to I_{out} conversion may be quasi linear. This is true if the differential-amplifier transfer function has a square root character. In next sections it is shown, that this is possible.

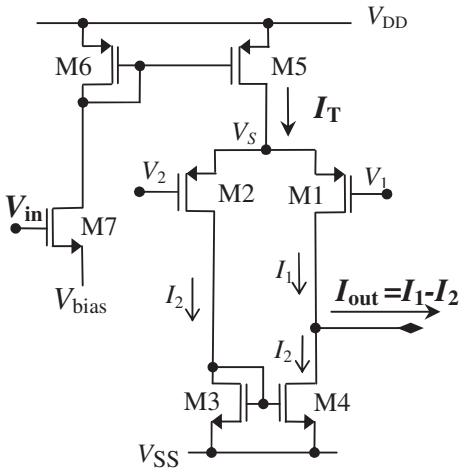

Fig. 2. Differential pair based simple CMOS voltage to current converter.

IV. Idea of Improving Power Saving by Means of Switching Technique

As mentioned in the previous section, the voltage to current conversion can be realized provided that the differential current amplifier realizes a current transfer function of the square root type. Similarly as in Fig. 2, the circuits of Fig. 4 can present a quasi linear voltage to current converter when using V_{in} as input and I_{out} as the output signal. The block diagrams of Figs. 3 and 4 show, how the V_1 and V_2 voltage sources, which are used to control the amplifier gain, can become inactive by means of the S_1 and S_2 switches. Being inactive, the sources consume no power. The difference between the circuits of Fig. 4 and Fig. 3 is that I_T current in Fig. 4 (bottom) is not the input signal but is obtained by converting the input V_{in} voltage to the I_T current. Unlike in Fig.3, the differential pair of Fig. 4 includes *n*-channel transistors. Moreover, the control of the S_1, S_2 switches in Fig. 4 is realized not be means of current but by means of voltage.

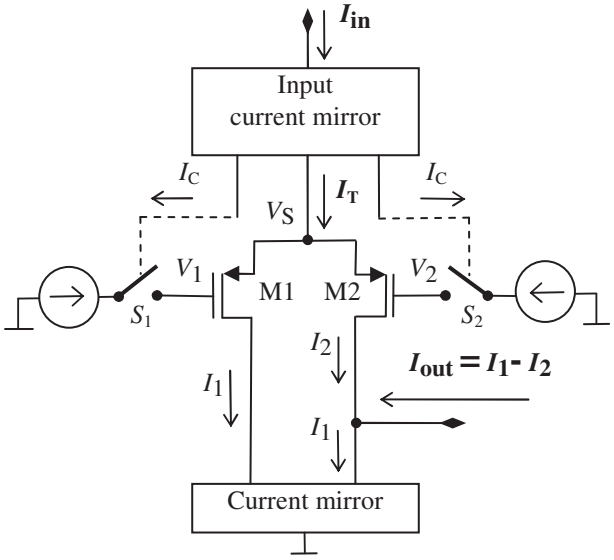

Fig. 3. Basic diagram of improved power-saving differential-current-amplifier atypically used.

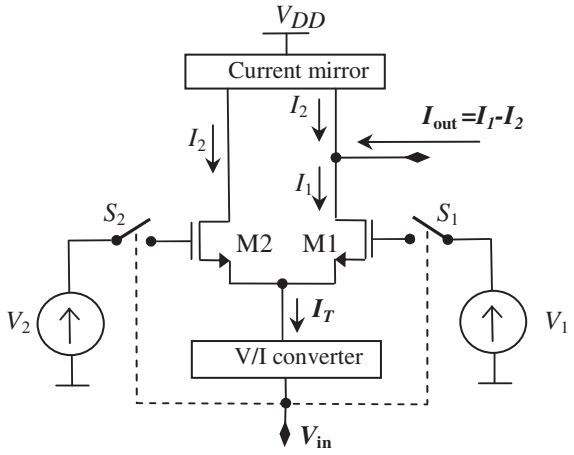

Fig. 4. Block diagram of improved power-saving differential-pair-based circuit for voltage-to-current conversion.

V. Theoretical Description of the Problem

Theoretical description of the proposed circuits is focused on determining relation between output current, I_{out}, and tail current, I_T, in the models shown in Figs. 3 and 4. Additional relationships concerning the considered circuits, i.e. I_{out} =f(I_{in}) and I_{out} =f(V_{in}), are easily achievable using MOS transistors and their connections.

In the proposed description, it is assumed that all MOS transistors operate in saturation and in strong inversion. The final relationship between I_{out} and I_T is given by (7) and results from solving the (1)-(4) set of equations.

$$I_1 \cong K(V_1 - V_S - V_{th})^2 , \tag{1}$$

$$I_2 \cong K(V_2 - V_S - V_{th})^2 , \tag{2}$$

$$I_{out} \cong I_1 - I_2 , \tag{3}$$

$$I_T \cong I_1 + I_2 , \tag{4}$$

In the square relationships, (1) and (2), describing the MOS transistors, V_S is source potential, V_{th} is threshold voltage and K is a real-valued coefficient.

The obtained expression for output current, I_{out}, of the converter shown in Fig. 4, is of the form

$$I_{out} \cong \sqrt{2K}(V_2 - V_1)\sqrt{I_T - \frac{K}{2}(V_2 - V_1)^2} \tag{5}$$

If the condition given by (6) is fulfilled

$$I_T >> \frac{K}{2}(V_2 - V_1)^2 \quad , \tag{6}$$

output current, I_{out}, as a function of the tail current, I_T, takes the below given square-root formula

$$I_{out} \cong \sqrt{2K}(V_2 - V_1)\sqrt{I_T} \tag{7}$$

In other words, the relation (7) holds if value of the V_2-V_1 voltage difference is sufficiently low.

From the obtained relationships, two things result. The first one is that the presented current can be proportional to square root of the input I_T current. This implies that we can realize an operation of square root extraction if the diagram of Fig. 3 is implemented. The second option concerns the block diagram of Fig. 4 illustrating the idea of transconductance signal processing with V_{in} as the input voltage. Since I_T can easily be expressed by V_{in}, making use of the well known quadratic relation of MOS transistors, we can finally realize a quasi-linear voltage-to-current conversion. An example of the voltage-to-current converter implementing the idea of Fig. 4, described be the formula (7), is presented in next sections of the paper. As will be seen, the proposed converter can operate in a very power-saving manner.

VI. Voltage-to-Current Converter Implementing the Power-Saving Idea of Fig. 4

In Fig. 5, detailed diagram of a CMOS voltage-to-current converter, realizing the idea of Fig. 4, is shown. The presented circuit is a modification of that published in [8] and [10]. The circuit presented in [8] was designed to realize an analog differential synapse for analog neural networks implemented on chip. It has three external terminals. One of them receives the signal to be transmitted and the other two are used to control the transfer function gain. The circuit published in [10], on the other and, was used as voltage to current converter

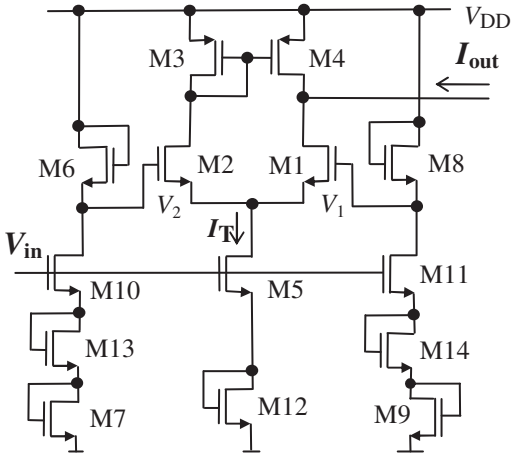

Fig. 5. CMOS power-saving quasi-linear voltage-to-current converter with an automatic switch-off mechanism improving power efficiency.

adapted for hardware implementation of self-organizing neural networks. In that converter, two external terminals are used to realize the given task. The circuit of [10] was prototyped in 0.18 micrometers CMOS technology and positively verified in the way of measurements.

The converter of Fig. 5 discussed in this paper differs from the previous ones in that it includes only one input to which the V_{in} voltage is delivered, and next converted to the output as the I_{out} current. Gain of the converter is not electronically controlled. The gain is determined by proper designing sizes of transistors included in the converter circuit.

Unlike in [8], our solution reduces to zero the total power taken from the supply rail. It results from applying the proposed switching mechanism based on the M6, M7, M8, M9, M10, M11, M13, and M14 transistors. Notice that all currents flowing through the paths between the V_{DD} rail and ground go to zero when V_{in} drops below some threshold value. This concerns the transistors M10, M13, M7 on the left hand side, and M11, M14 M9 on the right hand one in Fig. 5.

The transistors M5 and M12 are used to convert the input V_{in} voltage to the tail current I_T. As results from the formula (7), the I_T current must be proportional to square of the input voltage if we want to obtain a quasi linear relation between the output current I_{out} and the input voltage V_{in}. In our circuit, this is ensured by utilizing quadratic relation between the M5 transistor drain-current and its gate-source voltage.

VII. SPICE SIMULATION RESULTS

To verify the discussed theoretical properties of the considered converters, simulation results concerning the circuit of Fig. 2 and that of Fig. 5 are presented in this section. In case of the converter of Fig. 2, supply and bias voltages are V_{DD} =1.65V, V_{SS} = -1.65V, and V_{bias} = -1V, respectively. This gives the equality $V_{DD} - V_{SS}$ = 3.3V. Threshold voltages of the used n-channel and p-channel transistors are V_{TH} = 0.837V and V_{TH} = - 0.744V, respectively. Transistor sizes, i.e. length (L) and width (W), concerning the converter shown in Fig. 2, are given in Table 1.

TABLE I
TRANSISTOR CHANNEL SIZES OF THE CIRCUIT OF FIG. 2.

Trans.	M1	M2	M3	M4	M5	M6	M7
W(μm)	30	30	1	1	8	1	1
L(μm)	1	1	1	1	1	1	150

Simulation results presenting DC properties of the voltage-to-current converter of Fig. 2 are shown in Fig. 6. Bottom curves present the I_{out} output currents as functions of the input voltage V_{in}, for V_1 equal to zero and for different values of V_2, which change in the range from – 75mV to 75mV. Positive slopes of the bottom plot characteristics correspond to positive values of V_2. Notice that linearity of the obtained curves is quite good. The upper diagram of Fig.6 illustrates current efficiency of the converter. This efficiency, defined as ration of the I_{out} current to the V_{DD} supply current, is not bad, reaching a maximum level when the value of V_2 is the highest and equal to 75mV. For the maximum case, the obtained efficiency is about 90% and decreases slowly when V_{in} exceeds 1.2V.

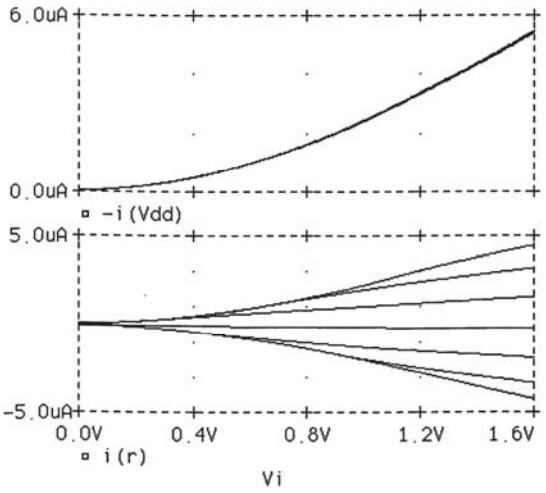

Fig. 6. Simulation results concerning the converter of Fig. 2: a) output current, I_{out}, versus input voltage, V_{in}, for different values of the V_1 - V_2 difference controlling the amplifier gain (bottom); b) current taken from the V_{DD} supply rail (upper).

As regards the converter presented in Fig. 5, the total supply voltage is equal to V_{DD} = -1.9V. Threshold voltages of the used n-channel and p-channel transistors are V_{TH} = 0.4655V and V_{TH} = - 0.617V, respectively. Transistor sizes, concerning the converter of Fig. 5 are given in Table 2.

TABLE II
TRANSISTOR CHANNEL SIZES OF THE CIRCUIT OF FIG. 5.

Trans.	M1	M2	M3	M4	M5	M6	M7
W[μm]	9	9	12	12	1	1.2	0.6
L[μm]	10	10	0.6	0.6	10	0.6	1.2
Tran.	**M8**	**M9**	**M10**	**M11**	**M12**	**M13**	**M14**
W[μm]	1.2	0.6	24	24	1	22	22
L[μm]	0.6	2.4	0.6	0.6	10	0.6	0.6

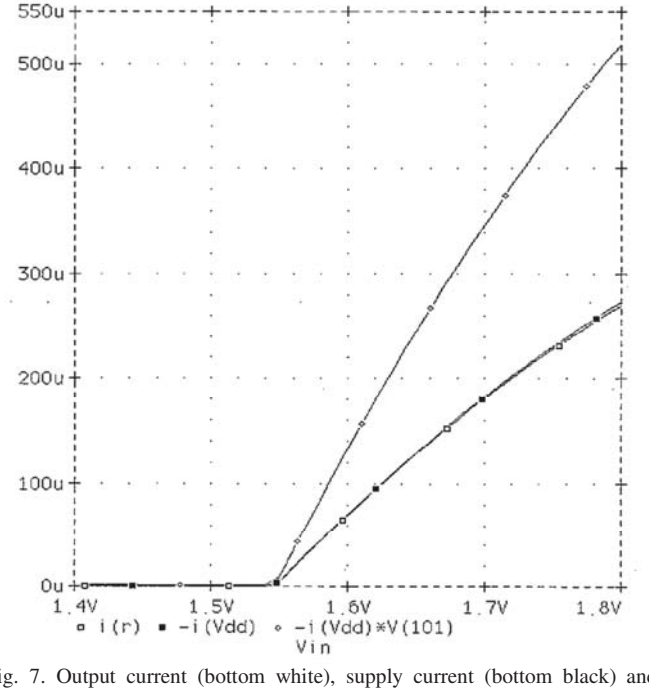

Fig. 7. Output current (bottom white), supply current (bottom black) and supply power (upper white) versus input voltage of the circuit of Fig. 5.

The upper curve of the Fig. 7 presents power taken from the supply rail, the bottom trace with black marks shows the current taken from the supply rail and the bottom curve with white marks depicts the I_{out} output current, all of them as function of the converter input voltage V_{in}. The curves of Fig. 7 are in good agreement with theoretical predictions. Notice that all of the curves go to zero if input voltage drops to about 1.55V. This is an important advantage of the circuit. Notice, moreover, that the supply current is only slightly higher than the converter output current. This means that power consumed by the converter is really very low. In this respect, the converter of Fig. 5 is better than the on of Fig. 2, i.e. is more power efficient.

Fig. 8 illustrates the converter linearity matter. In case of ideally linear transfer characteristic, speed of the I_{out} current variations, i.e. the curve slope, in response to the V_{in} variations, should be constant (middle plot). This means, that the derivative of I_{out} with respect to V_{in} should be a horizontal line shape (bottom plot). As can be seen from both curves, linearity of the voltage-to-current conversion is not perfect but can be admitted as satisfactory. The converter of Fig. 5 can be regarded as quasi linear when operating over the input voltage range from 1.55V to 1.8V. In this range, its linearity is comparably with that of the converter shown in Fig. 2. The achieved quasi linear range of operation is narrower in case of the circuit of Fig. 5 than that concerning the circuit of Fig. 2. This results mainly from lower value of the supply voltage and from greater number of the transistors used.

What else is worth emphasizing is that the applied 1.9V supply voltage of the converter of Fig. 5 is truly small compared to the sum of absolute values of the PMOS and NMOS threshold voltages, being equal to 0.617+0.4655 = 1.087V.

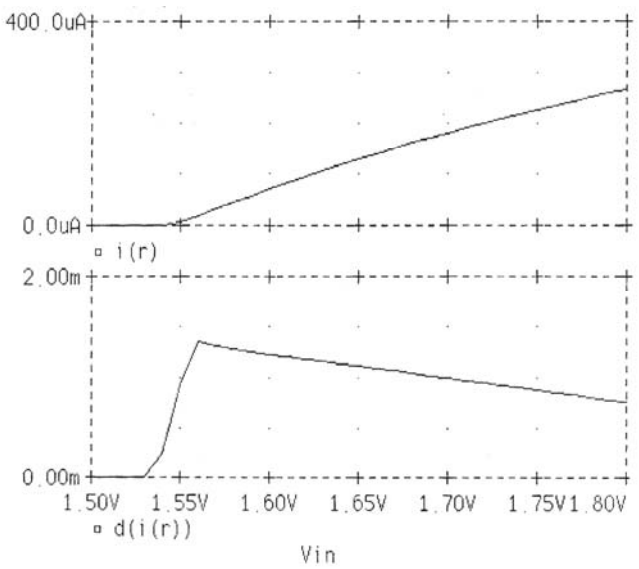

Fig. 8. DC characteristics of the voltage to current converter of Fig. 4: a) output current, I_{out}, versus input voltage V_{in} (upper), b) derivative of I_{out} with respect to V_{in} versus V_{in} (bottom).

VIII. Conclusions

Low-voltage low-power CMOS voltage-to-current converters have been presented. The converter operations are based on using differential amplifier. The main advantage of the converters is that they consume energy almost exclusively when the input voltage, V_{in}, exceeds some threshold value. Another advantage of the converters is their low sensitivity to input noise due to the common-mode rejection effect, characteristic of differential amplifiers. The difference between our circuits and the conventional differential amplifiers is that in case of the latter, the gate voltages, V_1 and V_2, are the input signals, while in the former, the tail current, I_T, is the input signal which has to be increased by the amplifier. That is why the output I_{out} current goes to zero if the input tail current, I_T, disappears. Power efficiency of the converters is the higher the stronger is the amplifier gain. The achieved power saving is better in case of the converter presented in Fig. 5. This is because the proposed simple switching technique has been applied in order to eliminate parasitic power consumed by the control voltage sources. These sources deliver the V_1 and V_2 signals to gate terminals of the M1, M2 transistors. In case of the converter of Fig.5, the improved power saving is at the cost of decreasing the range of the V_{in} input voltage variations, in which one obtains a quasi linear voltage-to-current conversion. Further studies in this field oriented on solving the problem are in progress. Our motivation is the observed increase in demand for low-power analog signal processing within an integrated circuit, in particular demand for power efficient transconductors.

References

[1] G. Cauwenberghs, M. A. Bayoumi, E. Sanchez-Sinencio, “Learning on silicon: Adaptive VLSI Neural Systems”, Kluwer Academic Publishers, 1999.

[2] S. Fakhraie, K. C. Smith, “VLSI-compatible implementations for artificial neural networks”, Kluwer Academic Publishers, 1997

[3] B. Linares-Barranco, E. Sanchez-Sinencio, A. Rodriguez-Vazquez, J. L. Huertas, “A CMOS Analog Adaptive BAM with On-Chip Learning and Weight Refreshing”, IEEE Transactions on Neural Networks, Vol. 4, No. 3, 1993, pp.445-455. 1993

[4] Shih-Lun Chen; Ho-Yin Lee; Yu-Wen Chu; Chiung-An Chen; Chin-Chun Lin; Ching-Hsing Luo, “A variable control system for wireless body sensor network”, IEEE International Symposium on Circuits and Systems (ISCAS), 18-21, pp.2034-2037, May 2008.

[5] Rodriques Vazques, S. Espejo, R. Domingues-Castro, J. L. Huertas and Sanches-Sinencio, “Current-mode techniques for the implementation of continuous and discrete-time cellular neural networks”, IEEE Transactions on CAS , CAS-40, pp. 132-146, 1993.

[6] R. Wojtyna, M. Kalista, „Quasi-linear low-power variable-gain transconductor for VLSI CMOS artificial neural networks”, Int. Workshop MIXDES’2000, pp. 473-476, Gdynia 2000 W. Machowski, S. Kuta, J. Jasielski, J. Kołodziejski, „Fast low voltage analog four-quadrant multipliers based on CMOS inverters”, International Journal of Electronics and Telecommunications, vol. 56, no. 4, s. 381-386, 2010.

[8] R. Wojtyna, T. Talaśka, „Improved Power-Saving Synapse for Adaptive Neuroprocessing on Silicon”, ICSES’2004, pp. 27-30, 2004.

[9] R. Wojtyna, „Analog-technique-based neuroprocessing implemented in hardware”, IEEE Workshop SPA 2009 (Signal Processing – Algorithms, Architectures, Arrangements and Applications), pp. 9-12, 2009.

[10] R. Długosz, T. Talaśka, W. Pedrycz, R. Wojtyna, “Realization of the Conscience Mechanism in CMOS Implementation of Winner-Takes-All Self-Organizing Neural Networks”, IEEE Trans. Neural Networks, Vol. 21, No. 6, pp.961-971, 2010.

[11] R. Długosz, T. Talaśka, "Low Power Current-Mode Binary-Tree Asynchronous Min/Max Circuit", Microelectronics Journal, Elsevier, No.1, pp.64–73, January 2010.

[12] R. Wojtyna, "CMOS transconductance-mode analog circuit for fast determining Euclidean distance", Elektronika, Nr 4/2007, pp. 65-68

[13] R. Wojtyna, "Analog low-voltage low-power CMOS circuit for learning Kohonen networks on silicon", International Conference MIXDES'2010, pp. 209-214, 2010.

[14] R. Wojtyna, "Differential-pair-based Current-mode Analog Signal Processing", International Conference MIXDES'2015, pp. 585-588 , Toruń 2015

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