A Novel High-Swing High-Speed with 187μW Power Consumption Common-Mode Feedback Block (CMFB) Based on Rail-to-Rail Technique

Sina Mahdavi, Faeze Noruzpur, Esmail Ghadimi, and Tohid Moradi Khanshan

***Abstract*—This paper presents a new high-swing, high-speed and low power continuous-time Common-Mode Feedback Block (CMFB) based on rail-to-rail technique. The main purposes of the proposed idea are to achieve high-speed, low settling time error, large output swing, and low power as well. Moreover, applying the worst case simulation (initial condition 0 and 1.8 volts) on the proposed CMFB circuit, the output voltage can be settled in the desired level just after 1.18ns noticeably. The settling time error and the power consumption of the suggested common-mode feedback circuit are just 103μV and 187μW with the power supply of 1.8 volts respectively. Meanwhile, DC gain and phase margin of the amplifier are 74dB and 67 degree correspondingly, and 0.5pF capacitor load is applied to the output nodes of the amplifier. It is noteworthy that, the proposed idea is a good candidate for low voltage applications too. Because it just needs 2 overdrive voltage (ΔV) to start its performance. Applying the proposed idea on the folded cascode amplifier it achieves SNDR of 68.68dB with the Effective Number of Bits (ENOB) 11.15 bits respectively. The proposed CMFB occupies an active area of 155.58μm^2 (10.56μm*14.73μm). Finally, the proposed structure is simulated in whole process corner condition and different temperatures from -70℃ to +70℃. Simulation results are performed using the HSPICE BSIM3 model of a 0.18μm CMOS technology.**

***Index Terms* —Common-Mode Feedback; High-Speed; Low Voltage; Folded Cascode; High Swing**

I. Introduction

RECENTLY, fully differential structures are used in mixed signal and analog systems widely. Since, fully differential structures have many benefits such as higher dynamic range, better common mode noise rejection, larger output swing rather than the single-ended counterpart [3, 8, 10, 25, 26, 28, 29]. However, despite the advantages, to stabilize the common-mode voltages for fully differential analog systems in order to adjust the common-mode output currents, a Common-mode feedback circuit (CMFB) is required [2, 3, 4, 7, 10, 12, 25]. The two differential output voltages are averaged and compared to the common-mode reference voltage (Vref), and the differential voltage is converted to the common-mode output current to adjust the common-mode voltage [1-6]. The CMFB circuit is a fundamental circuitry for a fully differential system. Without CMFB, the transistors in the system may easily drift away from saturation region due to mismatch and other process tolerances and cause a system malfunction, especially in low supply voltage applications where the voltage headroom to keep transistors in the saturation region is very small [6, 8, 9, 30].

Several CMFB configurations have been presented in the literature, using both continuous-time (CT) and switched-capacitor (SC) topologies [11, 16, 20].In order to improve the performance of the CMFB, several types of CMFB circuits have been proposed: resistor averaging circuit, switched-capacitor averaging circuit, and differential amplifier [3, 8, 10, 17, 18, 29].

In this paper, a new high-swing, high-speed and low power continuous-time Common-Mode Feedback Block (CMFB) based on rail-to-rail technique is presented. Moreover, in the proposed idea the most motivation is to increase the speed, the linearity, decrease the settling time error and improve the output swing of the common-mode feedback circuit. In addition to, it is a proper choice for using low voltage applications too.

The proposed paper is organized as follow: Section II describes the principle of the CMFB, briefly. in section III different types of the CMFB are discussed. Proposed common-mode feedback is presented in section IV. In section V simulation results of the paper are specified and finally, section VI concludes the paper.

II. The Principle of the CMFB

As discussed above, to permanent common-mode voltages at the output of differential-mode circuits, common-mode feedback (CMFB) circuits are required [1, 2]. For this case, CMFB circuits usually sense the average (common-mode) voltage of the differential output voltages $V_{CM} = ((V_{out+} + V_{out-})/2)$, which is compared to the desired reference voltage (Vref). So, the resulting error is amplified by an error amplifier and often transformed to a common mode current which adjusts the common-mode voltage [3, 5, 6, 8, 22, 23, 24, 27, 29]. Fig. 1 and 2 show the general block diagram of the CMFB, also (1) indicates the output voltage of the common mode circuit.

$$V_{CMFB} = \left(\frac{(V_{out+}+V_{out-})}{2}\right) * A_V(S) \quad (1)$$

S. Mahdavi and F. Noruzpur are with Department of Microelectronics Engineering, Urmia Graduate Institute, Urmia, Iran (e-mails: m.s.mahdavi@urumi.ac.ir, m.f.noruzpur@urumi.ac.ir).

E. Ghadimi is with Department of Mechanical Engineering, Tabriz Branch, Islamic Azad University, Tabriz, Iran (e-mail: Esmailghadimi240@yahoo.com).

T.M. Khanshan is with Urmia University, Urmia, Iran (e-mail: t.moradi@urmia.ac.ir).

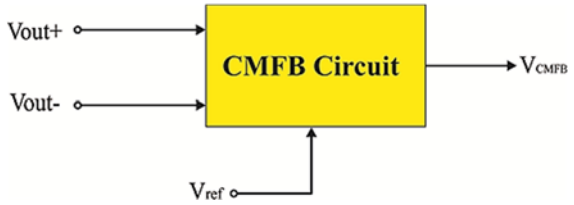

Fig. 1. A general block diagram of the CMFB circuit

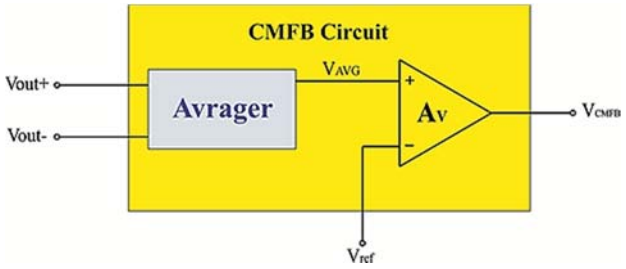

Fig. 2. A general block diagram of the CMFB with its internal circuits

As it is clear that, a CMFB just apply on the differential amplifiers, due to that a simple fully differential amplifier is depicted in Fig. 3, and some mathematic equations and small signal analysis are presented to achieve the DC gain of the amplifier in both differential and common-mode case. Fig. 4 shows how the CMFB is applied on the fully differential amplifier. As it is obvious in mentioned figure, the output common-mode voltage of the amplifier is employed to the input terminal of the CMFB circuit and it senses the average (common-mode) voltage of the differential output voltages which is compared to the desired reference voltage (Vref).

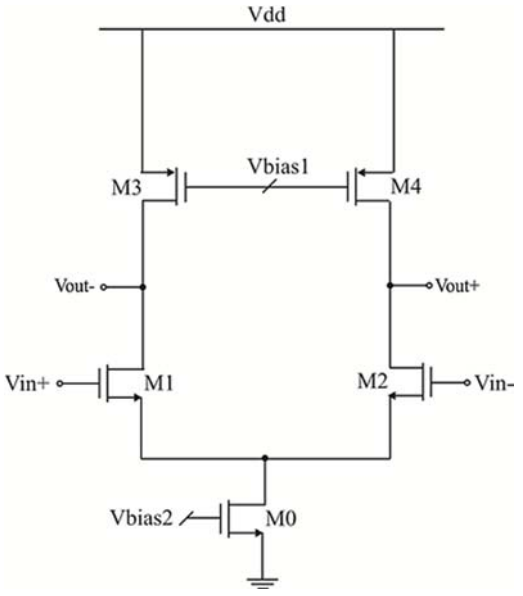

Fig. 3. A simple fully differential amplifier

Consequently, the resulting error is amplified by an error amplifier and converted to a common mode current which adjusts the common-mode voltage as well. Meanwhile, Fig. 5 and 6 present the simplified AC small signal model of the fully differential and half circuit of the amplifier in common-mode analysis respectively [22-24, 27].

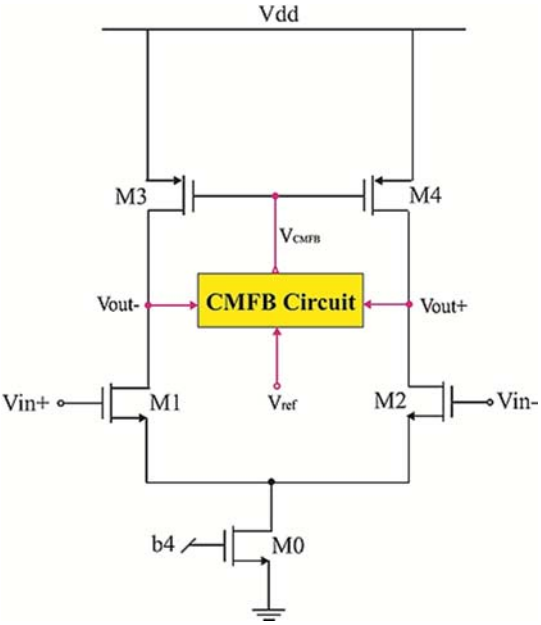

Fig. 4. A simple fully differential amplifier with applying CMFB circuit

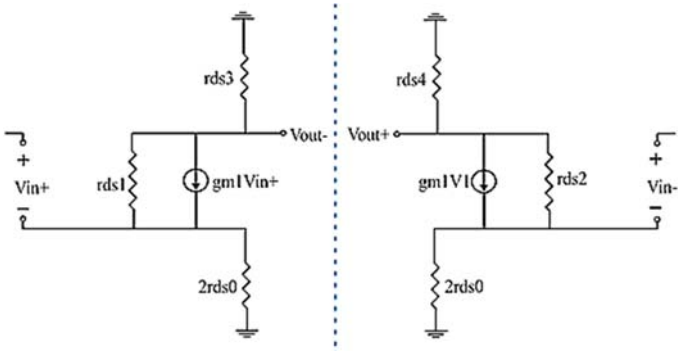

Fig. 5. A simplified AC small signal model of the simple fully differential amplifier in common-mode analysis

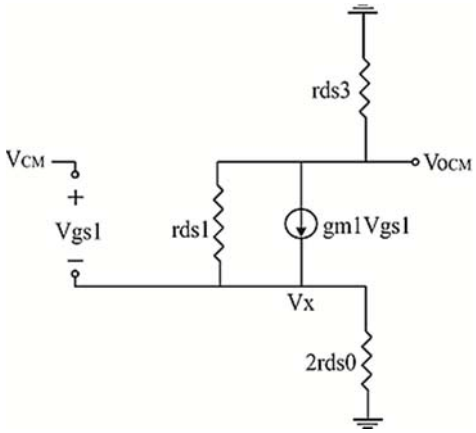

Fig. 6. A simplified AC small signal model of the amplifier (half circuit) in common-mode analysis

It is noteworthy that, completely difference-mode analysis hides all information about common-mode, and vice versa, also it happens in simulations too. Equations (2), (3), (4) and (5) are presented in order to attain the DC gain of the amplifier in the common-mode analysis, also the DC gain of the amplifier in the differential analysis are specified in (6), (7) and (8) respectively. As (5) and (8) show the DC gain in the common-

mode analysis is very lower than the differential one. For the meantime, in the next section, the different types of the CMFB such as Resistor averaging circuit(R-C), switched-capacitor averaging circuit, and differential difference amplifier (DDA) are discussed [22-25, 29].

$$Vgs1 = V_{CM} - V_x \tag{2}$$

$$g_{m1}(V_{CM} - V_x\ ) + \left(\frac{V_{OCM}}{rds3}\right) + \left(\frac{V_{OCM} - V_x}{rds1}\right) = 0 \tag{3}$$

$$V_x = \left(\frac{(g_{m1} * rds1 * V_{CM}) - V_{OCM}}{((-1) + (g_{m1} * rds1))}\right) \tag{4}$$

$$\Longrightarrow \left(\frac{V_{OCM}}{V_{CM}}\right) = A_{VCM} \cong \left(\frac{1}{\left(\frac{1}{g_{m1}}\right) + (2rds0)}\right) * rds3 \tag{5}$$

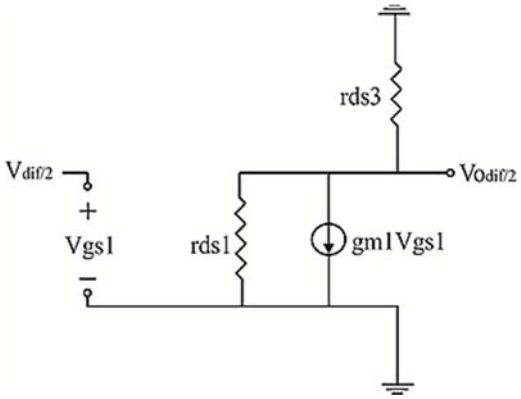

Fig. 7. A simplified AC small signal model of the amplifier (half circuit) in differential analysis

$$V_{dif/2} = Vgs1 \tag{6}$$

$$g_{m1} * \left(\frac{V_{dif}}{2}\right) = (V_{\frac{Odif}{2}})/(rds1||rds3\ ) \tag{7}$$

$$\Longrightarrow \left(\frac{\frac{V_{Odif}}{2}}{\frac{V_{dif}}{2}}\right) = A_{Vdif} \cong g_{m1} * (rds1||rds3\ ) \tag{8}$$

III. Different Types of the CMFB

Three different types of CMFB circuits have been developed: resistor averaging circuit(R-C), switched-capacitor averaging circuit, and differential difference amplifier (DDA) [8, 13, 15, 20, 29]. First, the resistor-averaging technique achieves very good common- mode (CM) detection accuracy but suffers from large chip area due to the large resistors. Likewise, the R-C common-mode feedback circuit can work at different supplies but requires large resistance to maintain the high DC gain and large output swing [2, 19]. Second, the switched capacitor CMFB circuit eliminates the resistive loading issue, but, it suffers from clock-injected noise and its application is limited to sampled data systems [16-18]. Also, it has the smaller passive area, but its loop bandwidth and stability are very sensitive to the supply voltage because of the supply-dependent on-resistance of the switches. [14, 17, 18, 19]. The DDA CMFB circuit utilizes transistors to average and compares the CM voltages, the continuous-time operation is hence achieved and the bandwidth of the CMFB circuit can be designed to be close to the bandwidth of the Fully Differential Amplifier with the realistic area and power consumption [4, 8, 11, 12, 13, 29]. Moreover, it does not need large area passive components, but it has the limited linear signal range for the main amplifier and is not suitable for a low supply. However, the conventional DDA CMFB techniques had limited input range and low detection accuracy when the differential input voltage is large, meanwhile, Fig. 8, shows the conventional DDA CMFB circuit. [2, 19, 20, 30]. In order to overcome some of the mentioned drawbacks, a new high-swing, high-speed and low power continuous-time Common-Mode Feedback Block (CMFB) based on rail-to-rail technique is presented in the next section.

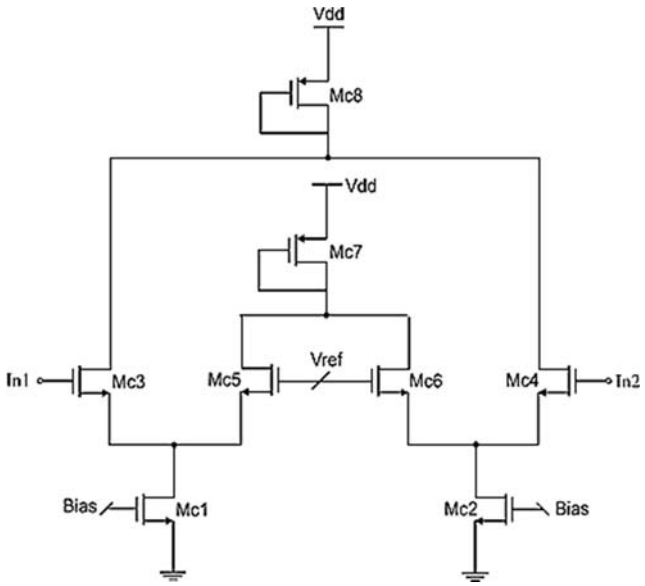

Fig. 8. A conventional DDA CMFB circuit

IV. The Proposed CMFB

The proposed common-mode feedback circuit and a simply folded cascode amplifier are indicated in Fig. 9 and 10 respectively. In the suggested CMFB circuit, the basic idea is to eliminate the diode-connected transistors in the conventional DDA CMFB which applies the error correction signal to the folded cascode op-amp [3, 4, 8, 29]. Since the diode-connected transistor generates an enormous delay in the feedback signal's path. As a result, by removing this transistor, the speed of the CMFB circuit will be increased extremely [4, 8, 29].

Thus, a new high-swing, high-speed and low power continuous-time Common-Mode Feedback Block (CMFB) based on rail-to-rail technique is presented. The main aims of the proposed idea are to achieve high-speed, high-linearity and low power CMFB accompanied wideband dynamic range and large output swing noticeably. The outputs of the amplifier are applied to the gate terminals of the differential pairs M1 – M4 in order to sense the output value which can play the function of the sensors of the proposed CMFB as well. On the other hand, the resistors of the R1-R2 are the actuators of the circuit, in order to compare the output value of the differential amplifiers with the desired level, the reference voltage

(Vref=Vdd/2) is applied to the gate terminals of the M5 –M8 properly. Meanwhile, the transistors M11-M14 are the current source of the CMFB. In addition to, for improving the stability of the proposed circuit transistors M9- M10 are exerted. It is clear that, if the output common mode voltage of the amplifier is high in this condition the n-type network (M1-M2, M5-M6, M11-M12) is activated is activated to stabilize the output value at the desired level. Also, if the output value is low in that time the p-network is activated, which all the transistors operate in the saturation region.

This rail-to-rail technique is a guarantee that the output value of the amplifier can be adjusted in the preferred level during the most operation process as well.

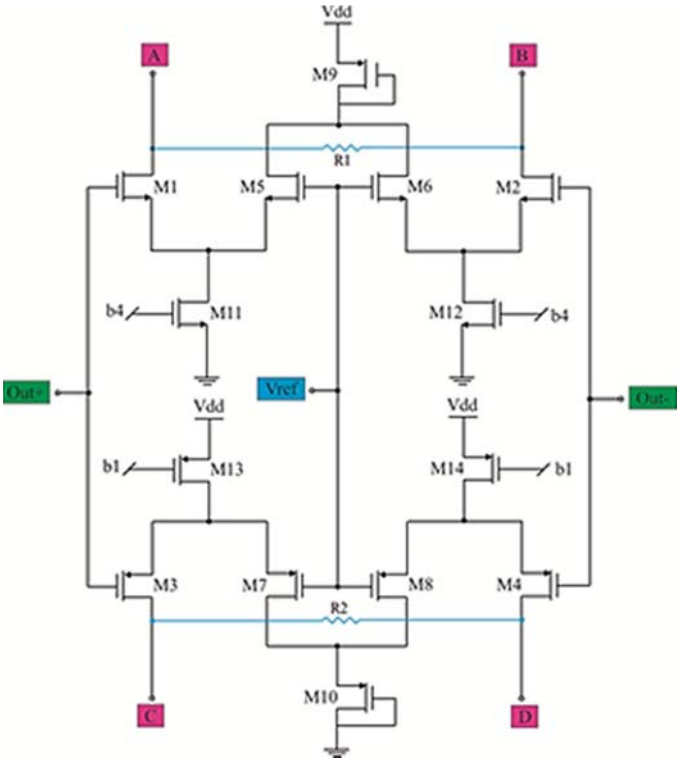

Fig. 9. The proposed CMFB circuit

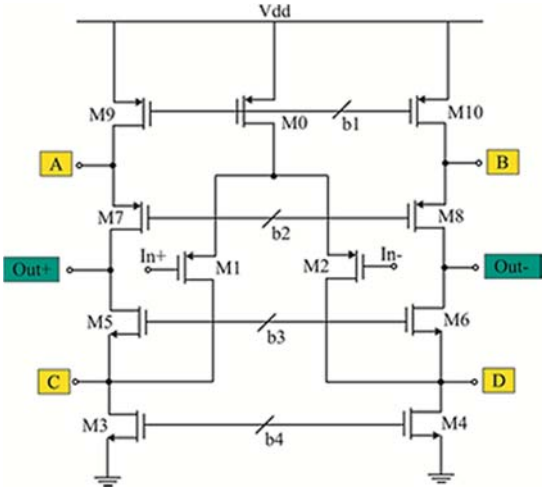

Fig. 10. A simple folded cascode amplifier

It is noteworthy that, as (10) shows the output swing of the proposed CMFB is improved rather than conventional one. Also, the output swing voltages in the conventional and proposed CMFB are represented in (9) and (10) respectively, where ΔV and Vth are overdrive voltage and the threshold voltage of the transistor correspondingly. Equation (10) proves, by using this method, the threshold voltage and one overdrive voltage of the (9) is removed as well. Due to this fact, the proposed idea is an appropriate option for low voltage applications too. Furthermore, the another key feature of the mentioned CMFB circuit is widely dynamic range voltage with low error, it means that if Vref adjusted near to 0.50 to 1.50 volts, the output voltage of the amplifier can be settled at the desired level as well. It is considered that, during the operation of the CMFB, all the transistors work in the saturation region.

$$\text{Output Swing}=\text{Vdd}-3\Delta V-\text{Vth} \quad (9)$$

$$\text{Output Swing}=\text{Vdd}-2\Delta V \quad (10)$$

V. Simulation Results

In this section, the simulation results of the proposed CMFB are presented. A 1000 irritation Monte Carlo analysis are applied to the Bode plots of the CMFB loop of the amplifier with and without capacitor load which is presented in Fig. 11 labeled (a) and (b) respectively, meanwhile, the unity gain bandwidth is 934MHz and 2.28GHz for the CMFB loop, and the phase margin is 49° and 67° correspondingly, also the DC gain is 74dB as well. The transient response of the output proposed common-mode feedback in TT corner and rest of the corner process (SF, FS, FF and SS) are indicated in Fig. 12 and 13 respectively. As it is clear that in Fig. 12, employing the worst case simulation (initial condition 0 and 1.8 volts) on the proposed CMFB circuit, the output voltage is settled at the desired level just after 1.18ns as well. Meanwhile, the 1000 irritation Monte Carlo analysis are applied to the transient response of the output common-mode voltage for 3% variation of transistors threshold voltage and temperature variation on the proposed CMFB which are shown in Fig. 14 and 15 correspondingly. Moreover, Fig. 16 shows the different reference voltage (Vref) versus output voltage of the amplifier in all corner processes reliably. It is noteworthy that in Fig. 16 applying the reference voltage (Vref) from 0.50 to 1.50 Volts, the suggested common-mode voltage capability to keep the output voltage in desired value (low error) appropriately. The FFT spectrum of the folded cascode amplifier is represented in Fig. 17. Considerably, to exert a Nyquist input (149.84MHz) at 300MHz sampling rate with the amplitude of 1mV the SNDR and SFDR are 68.68dB and 79.45dB respectively. Finally, the layout of the proposed CMFB is depicted in Fig.18. Meanwhile, the proposed CMFB has been designed in a standard 0.18 µm CMOS process with the power supply of 1.8V and simulated by HSPICE software using level 49 parameters (BSIM3v3).

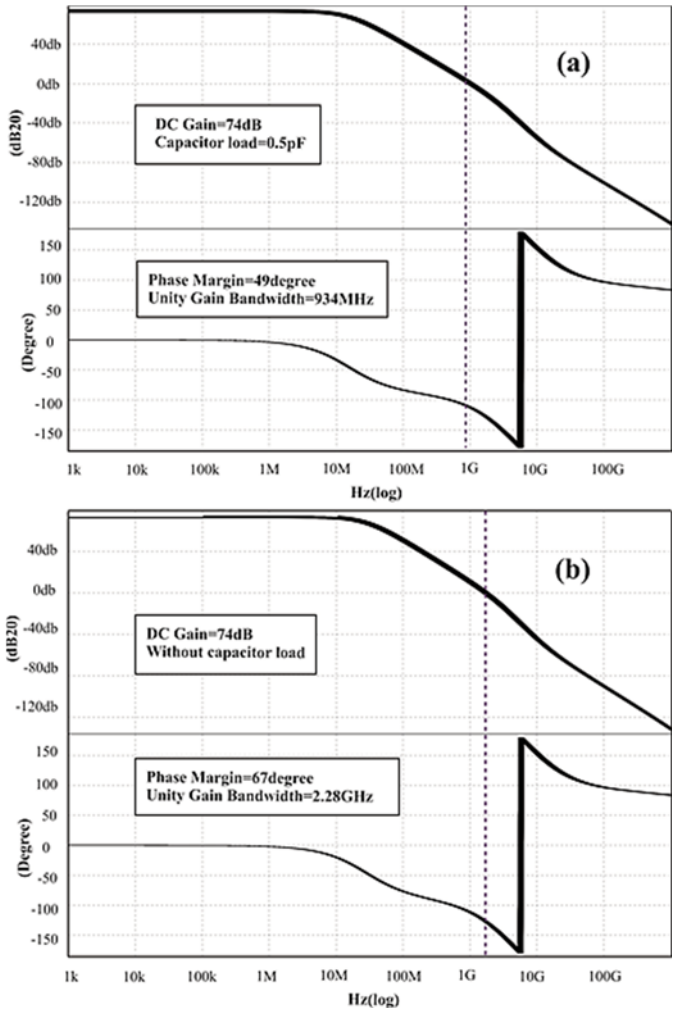

Fig. 11. 1000 Monte-Carlo analysis on the loop gain frequency response of the proposed CMFB circuit

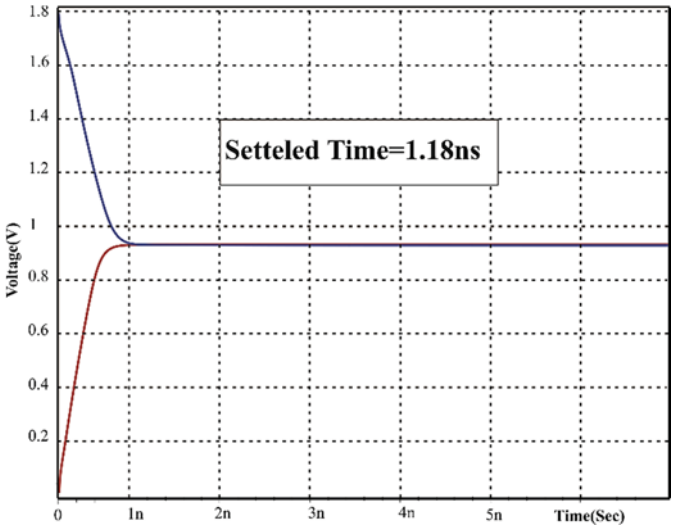

Fig. 12. Transient response of the output common-mode voltage in TT corner process

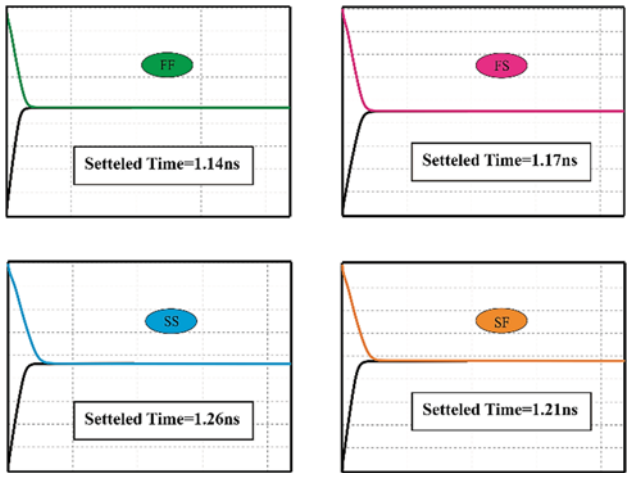

Fig. 13. Transient response of the output common-mode voltage in the process corners of SF, FS, FF and SS.

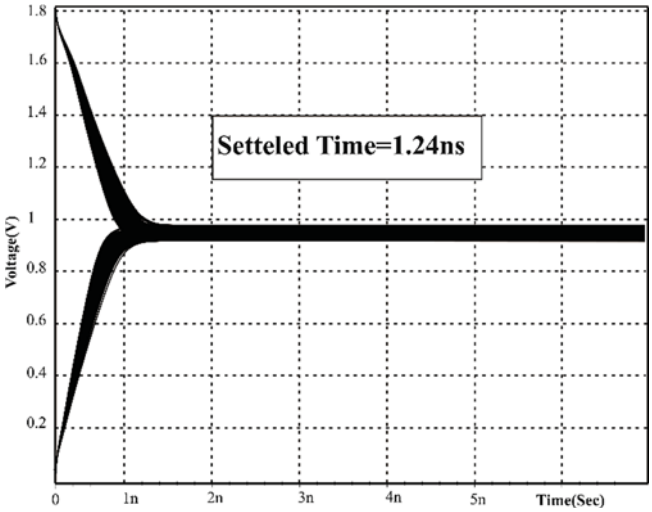

Fig. 14. 1000 Monte-Carlo analysis on the transient response of the output common-mode voltage by applying 3%varation of transistors threshold voltage

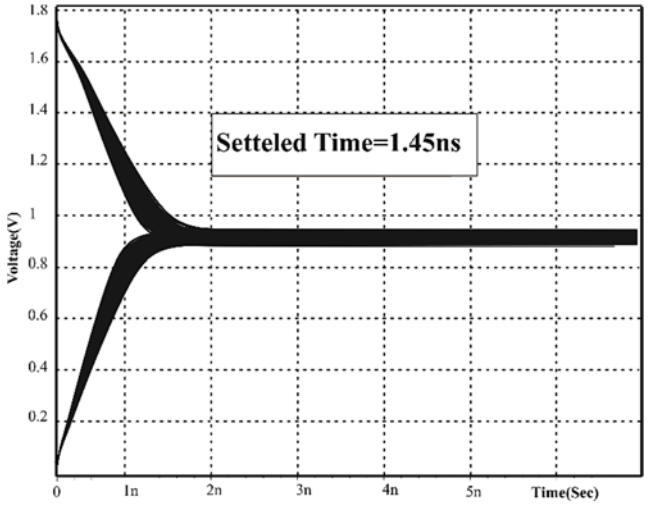

Fig. 15. 1000 Monte-Carlo analysis on the transient response of the output common-mode voltage by applying temperature variation from -70°C to +70°C

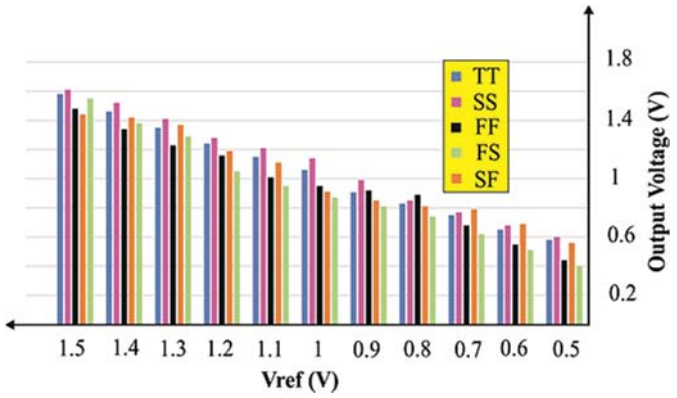

Fig. 16. Output common-mode voltage error: 0.50<Vref<1.50 in all process corners

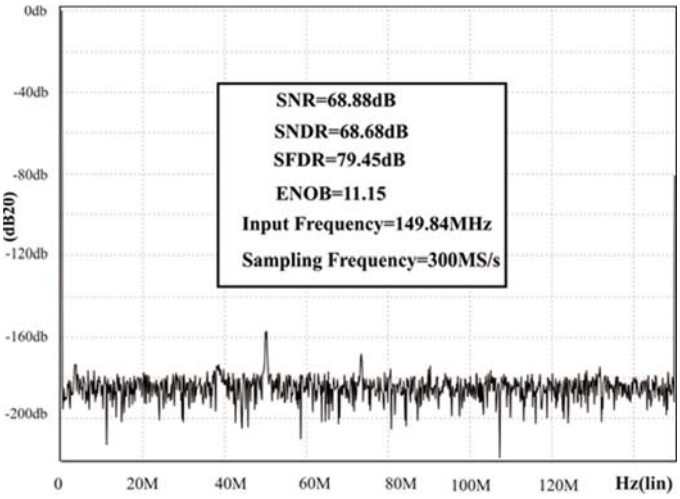

Fig. 17. Output FFT spectrum of the amplifier

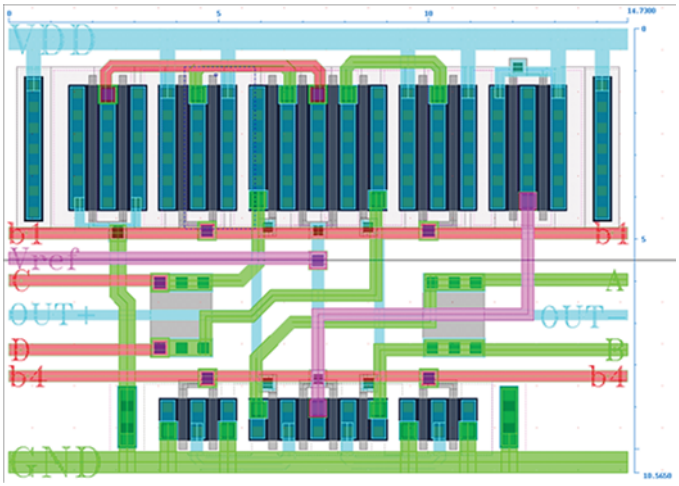

Fig. 18. The layout of the proposed CMFB

VI. Conclusions

A new high-swing, high-speed and low power continuous-time Common-Mode Feedback Block (CMFB) based on rail-to-rail technique is presented in this paper. The main aims of the proposed idea are achieving high linearity and high-speed CMFB accompanied wideband dynamic range, large output swing and low power as well. Furthermore, applying the worst case simulation (initial condition 0 and 1.8 Volts) on the proposed CMFB circuit, the output voltage can be settled in the desired level just after 1.18ns noticeably. Meanwhile, the proposed idea is a good candidate for low voltage and large output swing applications too. Because it just needs 2 overdrive voltage (ΔV) to start its performance. The power consumption of the suggested common-mode feedback circuit is just 187µW with the power supply of 1.8 volts. Finally, the Table I summarizes the performance of the proposed CMFB. The proposed circuit is simulated in whole process corner condition. Simulation results are performed using the HSPICE BSIM3 model of a 0.18µm CMOS technology.

TABLE I
CMFB PERFORMANCE SUMMARY

Parameters	Value
Technology	0.18µm
Supply Voltage	1.8V
Power supply noise	50mV
Power consumption	187µW
Settling error	103µV
Settling Time	1.18ns
Unity gain bandwidth	934MHz
Phase margin	67 degree
DC gain	74dB
Sampling rate (F_S)	300MS/s
SNDR	68.68dB
ENOB	11.15
CL	0.5pF
Chip area	10.56µm*14.73µm

References

[1] J. Zhang et. al., "A 0.6-V 82-dB 28.6-µW Continuous-Time Audio Delta-Sigma Modulator,", IEEE Journal of solid-state Circuits, vol.46, 2011, pp. 2326-2335.

[2] Y. Liu, C. Zhan, T.S. Yim, and W.H. Ki, "Continuous-Time Common-Mode Feedback Detection Circuits with Enhanced Detection Accuracy,", 2012 IEEE International Conference Electron Devices an Solid State Circuit (EDSSC), 2012, pp: 1-4.

[3] S. Mahdavi, A. Soltani, M. Poreh, S. Tayyeb ghasemi, T. Moradi Khanshan, "An Ultra High speed Low power Low settling time error and wide dynamic range voltage Continuous-time Common-Mode Feedback Circuit in 0.18µm CMOS,", Bulletin de la Société Royale des Sciences de Liège, Vol. 85, 2016, pp: 1457 – 1464

[4] T. Moradi Khaneshan, S. Naghavi, M. Nematzade, Kh. Hadidi, A. Abrishamifar, A. Khoei. "A Fast and Low Settling Error Continuous - Time Common-Mode Feedback Circuit Based On Differential Difference Amplifier", Journal of Circuits, Systems, and Computers © World Scientific Publishing Company. Vol. 23, No. 05, 2013.

[5] Y.K. Cho, B.H. Park, "Loop Stability Compensation Technique for Continuous-Time Common-Mode Feedback Circuits", 2015 International SoC Design Conference (ISOCC), 2015, PP: 241 – 242

[6] F. Castaño, G. Torelli, R. Pérez-Aloe, J. Carrillo, "Low-voltage rail-to-rail bulk-driven CMFB network with improved gain and bandwidth", 2010 17th IEEE International Conference on Electronics, Circuits and Systems, 2010, PP: 207 – 210

[7] J. Ramírez-Angulo, A. Nargis, G. Carvajal, A. López-Martín, "CMOS operational amplifiers with continuous-time capacitive common mode feedback", Proceedings of 2010 IEEE International Symposium on Circuits and Systems, 2010, PP: 1280 – 1283

[8] S. Mahdavi, F. Noruzpur, L. Alizadeh, M. Jalilzadeh, F. Judy "A 0.88nS Settling Time 115µV Settling Error with 68.18dB SNDR Continuous-time Common-Mode Feedback (CMFB) Circuit in 180nm CMOS Technology", International Journal of Mechatronics, Electrical and Computer Technology (IJMEC), vol.7(26), 2017, pp. 3674- 3684

[9] J. Carrillo; G. Torelli; M. Dominguez; R. Perez-Aloe; J. Valverde; J. Francisco Duque-Carrillo, "A Family of Low-Voltage Bulk-Driven CMOS Continuous-Time CMFB Circuits", IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 57, Issue 11, 2010, pp. 863 - 867.

[10] J. Wang, S. Bu, Z. Fu, D. Li, K. Pun, "An efficient frequency compensation scheme for CMFB loop in fully differential amplifiers", 2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), 2015, pp: 415 – 418

[11] A. Simonetti, A. Trifiletti, "An improved common-mode feedback loop for the differential-difference amplifier", 2011 NORCHIP, 2011, pp: 241-242

[12] H. Ma, Y. Ye, M. Yu, J. Lai, "A Novel Common-Mode Sensing Circuit with Large Input Swing for Op-AMP with Common-Mode Feedback", 2007 7th International Conference on ASIC, 2007, pp: 465-468.

[13] L. Luh, J. Choma, Jr., and J. Draper, "A Continuous-Time Common-Mode Feedback Circuit (CMFB) for High-Impedance Current-Mode Applications,", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol.44, ISSUE 4, 2000, pp. 363-369.

[14] M. Ali-bakhshian , K. Sadeghi, "A Novel continues time common mode feedback for low voltage switch opamp", 2004 international symposium on Low power electronics and design,2004,pp: 296-300

[15] Juan M. Carrillo; Josh L. Ausin; J. Francisco Duque-Carrillo, "CMOS continuous-time CMFB circuit with improved linearity", 2007 18th European Conference on Circuit Theory and Design,2007,pp: 40 – 43.

[16] D. Hernandez-Garduno; J. Silva-Martinez; J. Francisco Duque-Carrillo, "Continuous-time common-mode feedback for high-speed switched-capacitor networks", IEEE Journal of Solid-State Circuits, Vol. 40, Issue 8, 2005, pp. 1740 - 1747.

[17] O. Choksi; L.R. Carley, "Analysis of switched-capacitor common-mode feedback circuit", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 50, Issue 12, 2003, pp. 906 - 917.

[18] F.A. Amoroso; A. Pugliese; G. Cappuccino; G. Cocorullo, "Efficient switched-capacitor common-mode feedback circuit for high-speed low-power amplifiers", Electronics Letters, Vol. 44, Issue 21, 2008, pp. 1225 - 1226.

[19] C.W. Hsu and P.R. Kinget, "A Supply-Scalable Differential Amplifier With Pulse-Controlled Common-Mode Feedback," ,proceeding of the IEEE 2014 custom Integrated Circuits Conference, 2014, pp: 1-4.

[20] L. Zhang, R. Hu, C. Zhu, Y. Wang, Z. Zhang, R. Ye1, and Y. Gao, "A two-stage low-power amplifier with switch-capacitor common-mode feedback circuits,", 2014 XXXIth URSI General Assembly an Scientific Symposium(URSI GASS), 2014, pp: 1-4.

[21] X. Liu, J. F. McDonald ,L. Senior , "Design of Single-Stage Folded-Cascode Gain Boost Amplifier for 14bit 12.5Ms/S Pipelined Analog-to-Digital Converter", 2012 10th IEEE International Conference on Semiconductor Electronics(ICSE), 2012, pp: 622-626.

[22] Kh. Hadidi, "Data Converter Course Notes" Urmia University, Urmia, Iran, 2005.

[23] D. Johns, K. Martin, "Analog Integrated Circuit Design" University of Toronto, 1997.

[24] B. Razavi, "Design of Analog CMOS Integrated Circuits" Boston, McGraw-Hill, International Edition, 2001.

[25] J. Silva-Martinez, M. Steyaert, and W. Sansen, "Design techniques for high-performance full-CMOS OTA-RC continuous-time filters," Solid-State Circuits, IEEE Journal of, vol. 27, no. 7, pp. 993–1001, 1992.

[26] H. Recoules, R. Bouchakour, P. Loumeau, and F.T. Braz, "Two SC-CMFB networks used in fully differential OTA: measurements and improvements", Circuits and Systems, Proceedings. Midwest Symposium on, pp. 352–355, 1998.

[27] K. Ann Ng, Y. Ping Xu, "A Low-Power, High CMRR Neural Amplifier System Employing CMOS Inverter-Based OTAs With CMFB Through Supply Rails", IEEE Journal of Solid-State Circuits, Vol. 51, Issue 3, 2016, pp. 724 - 737.

[28] S. Mahdavi, "A 12 bit 76MS/s SAR ADC with a Capacitor Merged Technique in 0.18µm CMOS Technology", Journal of Electrical and Computer Engineering Innovations (JECEI), in press.

[29] S. Mahdavi, F. Noruzpur, E. Ghadimi, T. Moradi Khanshan, "A new fast rail-to-rail continuous-time common-mode feedback circuit," 2017 MIXDES - 24th International Conference "Mixed Design of Integrated Circuits and Systems, 2017, pp. 387 - 391.

[30] W. Yan and H. Zimmermann, "Continuous-Time Common-Mode Feedback Circuit for Applications with Large Output Swing and High Output Impedance,", 2008 11th IEEE Worshop on Design an Diagnostics of Electronic Circuits and Systems, ISCE2008, PP:1-5.

Sina Mahdavi was born in Ahar, East Azerbaijan, Iran, in 1988. He received his A.Sc. degree in Power Electrical Engineering from Technical and Vocational University of Tabriz, and B.Sc. degree in Control Engineering from Azerbaijan University of Applied Sciences and Technology, Tabriz, Iran, in 2009 and 2011 respectively. Also, he received his M.Sc. degree in Microelectronics Engineering from Urmia Graduate Institute, Urmia, Iran, in 2016 (with honor). His research interests are Analog and Digital Integrated Circuits Design, High-Resolution High-Speed Analog to Digital and Digital to Analog Converters, VLSI, OPAMP Design Techniques, Linear and Non-linear Control Systems, Mechatronics, PLC, Electric Motor and fuzzy systems, also he is study on Physics, Mathematics, Pharmacology, Management, Life Insurance and English Teaching, too. He is Editorial Board/ Reviewer Member of some International Journals and Member of the Iranian Consortium of Academics Specialists. Moreover, he is the Member of the East Azerbaijan Engineering System Organization and Young Researchers and Elite Club, Tabriz Branch, Islamic Azad University, and Student Member of the IEEE. He is currently with Tabriz Office of Education in Tabriz, Iran.

Faeze Noruzpur was born in Urmia, Iran, in 1985. She received her A.Sc. degree in Communication Engineering from Islamic Azad University of Bukan, and B.Sc. degree in Electronics Engineering from Elmo fan Graduate Institute, Urmia, Iran, in 2006 and 2011 respectively. Also, she is currently pursuing her M.Sc. degree in Microelectromechanical systems engineering from Urmia Graduate Institute, Urmia, Iran. Her research interests are Image sensor, Image processing, VLSI and fuzzy systems.

Esmail Ghadimi was born in Tabriz, East Azerbaijan, Iran, in 1989. He received his A.Sc. degree in Power Electrical Engineering from Technical and Vocational University of Tabriz, and B.Sc. degree in Control Engineering from Azerbaijan University of Applied Sciences and Technology, Tabriz, Iran, in 2009 and 2011 respectively. Also, he received his M.Sc. degree in Mechatronic Engineering from Islamic Azad University Tabriz Branch, Tabriz, Iran, in 2014. His research interests are Linear and Non-linear Control Systems, Modern Control Solutions including Optimal and Fuzzy Control Systems, AGC, GA and other Optimization Algorithms.

Tohid Moradi Khanshan was born in Urmia, Iran, in 1986. He received his B.Sc. and M.Sc. degrees in Electrical Engineering from Urmia University, Iran in 2008 and 2010, respectively. He is currently with microelectronics research laboratory at Urmia University, Urmia, Iran. His research interests are bioelectronics, analog and digital integrated circuit design, high-speed high-resolution data converters, and high-speed data transceivers.