Spice Simulation of Substrate Potential Shift in HVCMOS Technologies

Camillo Stefanucci, Pietro Buccella, Maher Kayal, and Jean-Michel Sallese

***Abstract*—High voltage CMOS active devices inherently include a parasitic vertical PNP bipolar transistor. When activated it injects holes into the substrate causing a dangerous potential shift. In this work a spice-modeling approach based on transistor layout is presented to simulate substrate de-biasing in Smart Power ICs. The proposed model relies on a parasitic substrate network without the need of a parasitic BJT in HVCMOS compact models. The results are compared with TCAD simulations at different temperatures showing good agreement. Potential shift of the substrate is analysed for different geometrical configurations to estimate the effect of P+ grounding schemes and backside contact.**

***Index Terms*—Smart Power ICs, HVCMOS modeling, vertical bipolar transistor, substrate potential shift**

I. Introduction

HIGH voltage (HV) integrated circuits for power applications require special technologies with lateral diffused MOS devices (LDMOST) [1]. The cross section of typical LDMOST is reported in Fig. 1 where a drift-region below the gate is present with respect to standard MOSFETs. The effect of this region can be added in compact modeling of standard spice models with a JFET [2] or more accurate physics models [3].

In the resulting HVCMOS technology, a deep n-doped well isolates the transistors from the substrate. Inherently this structure introduces a parasitic vertical PNP bipolar junction transistor (BJT). If the P-MOS is considered, the emitter of the vertical PNP corresponds to the drain of the transistor usually connected through an output pad to the load. Since in automotive and power applications the load of HVCMOS circuits is usually inductive, during the switching of power devices the output node voltage can go below the ground voltage or above the supply voltage[4]. The latter configuration activates the vertical BJT injecting hole current into the substrate that can lead to dangerous potential shifts and failures [5].

To simulate the parasitic current effects of the parasitic vertical PNP, this device is usually added in the compact model of the LDMOST. The parasitic BJT model must be calibrated and must be scalable with transistor size (W and L) [6]. However, the simulations of final model accurately predict the injected substrate current but not the local potential shift of the substrate beneath the HVMOS n-wells. For that purpose the substrate resistance should be properly estimated [7].

A general modeling methodology of the substrate is therefore required. A parasitic substrate network composed of diodes, resistors and homojunctions at P+, N+ contacts can be derived from a HV circuit layout to simulate in spice simulators substrate currents due to parasitic BJTs [8]. This substrate model includes minority carriers propagation and it has been demonstrated to be efficient for parasitic BJTs couplings simulations [9]. In this case the deep p-type (DP) well inside the deep n-well (DN) is usually neglected. The vertical PNP is instead automatically taken into account if the DP is included in the substrate network.

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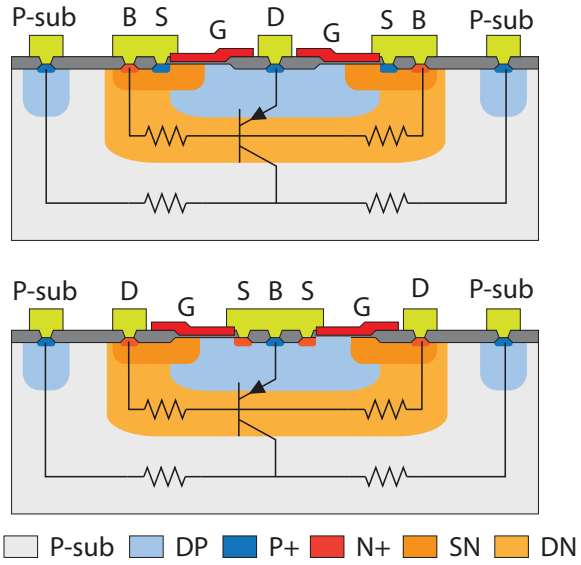

Fig. 1. Cross-section view of LDMOST devices in HVCMOS technology: P-MOS (top) and isolated N-MOS (bottom)

In this work the general substrate model and its lumped components will be used to simulate the parasitic PNP BJT in a p-channel LDMOST. The three-dimensional substrate network extracted from the device layout allows to monitor the substrate potential distribution in three dimensions with spice-like simulators without the need of a parasitic BJT in the compact model of the LDMOST.

This manuscript is structured as follows: in Section II the proposed model for the vertical PNP is presented with numerical simulations at different temperatures. In Section III the substrate de-biasing due to the activation of the vertical PNP BJT is analyzed comparing the model results with device physics simulations. In Section IV different grounding schemes are finally discussed. In particular the effects of different P+ guard ring sizing around the parasitic device, the effects of backside metallization and temperature are reported. Conclusion is drawn in Section V.

II. Vertical PNP Modeling

The vertical PNP Gummel-Poon model is usually added inside the compact model of HV transistors. A substrate network with the EPFL substrate model [9] can be equivalently used for this purpose. In this case there is no more need to include the PNP BJT inside the compact model of the LDMOST.

Following the model developed in [8], the parasitic substrate network is built by instantiating parasitic diodes, resistors and contacts between the various N and P wells of the layout for the entire substrate volume. The back-to-back connection of these diodes propagates minority carriers allowing NPN transistor simulations. In the same way the front-to-front connection of two diodes can simulate parasitic PNP transistor.

In Fig. 2 only the relevant details of the P-MOS device of Fig. 1 are retained for the modeling of the parasitic vertical PNP BJT. The instantiated diodes are of two type: the DP/DN and the DN/P-substrate. All the geometrical effects are included in the substrate network construction since each lumped device has a different area and length. To obtain the equivalent netlist a general algorithm has been implemented to process the layout by meshing the substrate in orthogonal cuboids and by defining electrical nodes along the three cartesian directions in an automatic way [10]. This distributed approach allows to separate the lateral and vertical contribution of the parasitic PNP BJT and to be highly scalable with respect the original transistor geometry. The resulting three dimensional network is equivalent to the Gummel-Poon PNP model and can be attached to the compact model of the intrinsic LDMOST without parasitics (see Fig. 2).

There are two main advantages of this modeling approach. The first one is that the spatial substrate potential distribution can be monitored due to the three dimensional nature of the parasitic network. Secondly, if the lateral NPN transistors result from the layout, they can be properly connected to the vertical bipolar transistor taking into account all the parasitic series resistances. Notice that, due to the injection of minority carriers the series resistances can be substantially differ from the standard RC substrate network [11].

To show the equivalence between the spice model network and the vertical PNP BJT, technology computer aided design (TCAD) simulations of the structure in Fig. 2 were run using Synopsys Sentaurus software [12]. All the geometrical parameters and the average doping concentrations of the wells are reported in the figure. These parameters are used in the spice model implemented in VerilogA and fit properly the more accurate TCAD device where gaussian doping profiles with surface peak concentrations are used. Doping and temperature dependent mobilities (Arora's model [13]) and lifetimes (Sharfetter's relation as in [14]) are also included. A low-doped P-type substrate typical for HVCMOS technologies is considered and a box of 700x700x700 μm^3 is simulated. The width of the structure is around $50\mu m$ emulating a LDMOST with two fingers and total width of $100\mu m$.

TCAD simulations and Spectre circuit simulator [15] results are compared in Fig. 3. For these simulations the collector

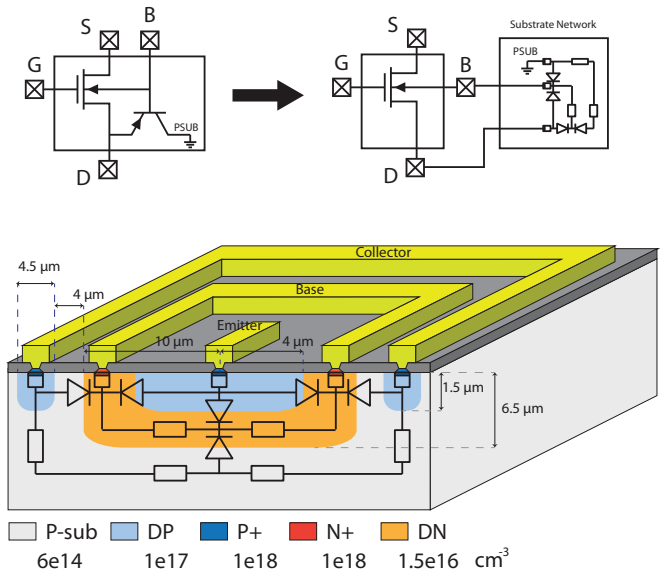

Fig. 2. Modeling approach to separate the parasitic components from the MOS compact model (top). Parasitic vertical PNP with corresponding equivalent circuit (bottom).

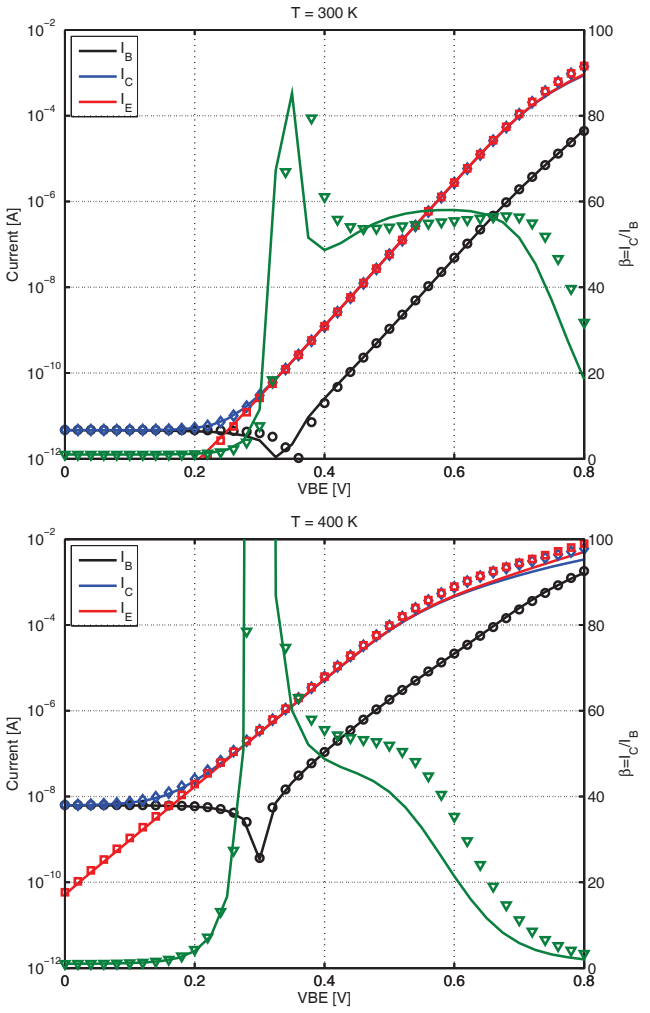

Fig. 3. Gummel plot at different temperatures for the vertical BJT of Fig. 2. Points corresponds to TCAD simulations and continuous lines to spice model.

(p-substrate) is kept at 0 V, the base (DN) at 12 V and the emitter (DP) is swept between 12 V and 12.8 V emulating an above supply bias condition of the drain of a P-MOSFET. A Gummel plot of the vertical PNP BJT with the corresponding current gain is reported for two different temperatures (300K and 400K) showing how thermal effects are properly tracked by the substrate circuit. No temperature fitting coefficients are present in the model and the intrinsic silicon parameters as a bandgap or an intrinsic carriers concentration follow correctly the temperature variation. Notice that for the simulations of the Gummel plot for the 3D device, TCAD requires more that 10 hours for the whole structure while spice 3D netlist only one minute.

III. Substrate De-biasing Simulations

The activation of a vertical PNP BJT and the consequent injection of holes into the substrate leads to a potential shift or de-biasing. In Fig. 4 the substrate potential distribution simulated in TCAD when $V_{BE} = 800mV$ and $I_E = 1.4mA$ is reported. It is possible to notice that for the substrate volume considered without backside contact, the P collector ring around the vertical PNP is keeping only locally the 0 V grounding voltage. When the transistor is highly forward biased the whole substrate will shift up to almost $1V$. This configuration could be detrimental if additional sensitive circuitry is placed around this device.

The potential distribution is even worst beneath the n-well which is the base of the vertical BJT. The cross section of the device along the XZ plane is presented in Fig. 5. In the point P at $18\mu m$ depth in the substrate, the potential rises to almost $2V$. The potential distribution is then spatial dependent. In the same figure also the cross section of the proposed

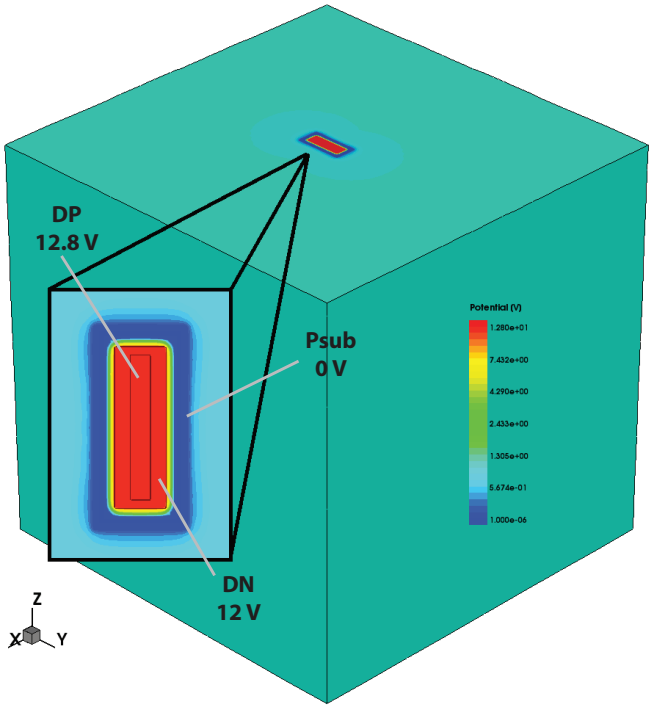

Fig. 4. Potential distribution (TCAD) for an injected current of $I_E = 1.4mA$.

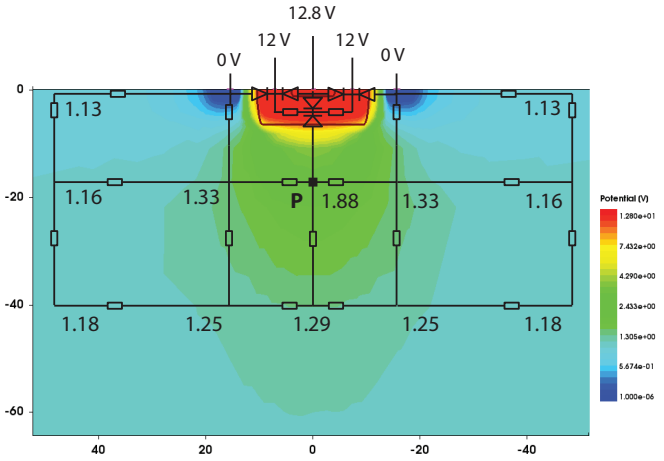

Fig. 5. Comparison between the potential shift simulated with TCAD (color plot) and the circuit results (numbers correspond to simulated node voltages).

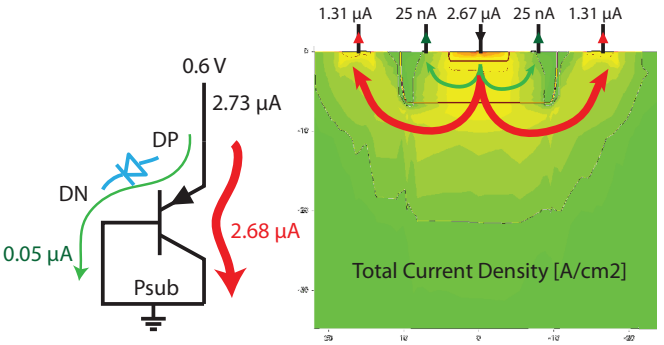

Fig. 6. Currents in diode-connected vertical PNP BJT. Spice simulation (left) and TCAD color plot of total current density (right).

three dimensional circuit network is showed. Monitoring the simulated node voltages there is the possibility to investigate in spice simulators the 3D de-biasing of the substrate which has a point-to-point match with TCAD simulation.

The simulated potential shift is due to the injection of the hole current into the substrate as a consequence of the high value for the beta of the vertical bipolar transistor ($\beta \simeq 55$, see Fig. 3). This is a well known situation for vertical PNP transistors, e.g. when they are used as reverse current blocking diodes in power stages. If a vertical PNP like the one in Fig. 2 is diode-connected to simulate its use as blocking diode the current will always pass through the substrate leading to potential shifts. As shown in Fig. 6 the BJT with the base connected to the collector is electrically equivalent to a diode (the base-emitter junction is indeed forward biased). Nevertheless, in a diode the current is flowing from the DP well (anode) to the DN well (cathode), while in the diode-connected BJT the current is almost flowing inside the P-substrate collector due to the high β. In the simulated example, the substrate de-biasing is only $1mV$ but when the current is further increased it can reach dangerous levels because it can unintentionally forward bias other N-wells with the risk of a latch-up.

IV. Substrate Contacts

The potential of the substrate can be kept under control with additional P contacts and a proper grounding scheme [16]. The simulations reported in Section III clearly show that the $4.5\mu m$ wide P guard ring around the device is not sufficient to maintain at 0V the substrate when the parasitic PNP is activated. Once the substrate potential shift is simulated, the willingness of designer is to modify the layout adding additional substrate contacts to reduce the substrate de-biasing.

A. Effect of Guard Rings

For the substrate biasing P+ contacts are used and they naturally collect holes protecting surrounding circuits from majority carriers injection. If the P contact ring of Fig. 4 is extended from $4.5\mu m$ to $14.5\mu m$ the substrate potential is expected to be lower and better controlled. TCAD simulations (see Fig. 7) showed that the layout modification reduced the substrate de-biasing at $V_E = 12.8V$ from almost $1V$ down to $0.3V$ ($700mV$ of voltage difference) at expense of the cell area. It should be noticed that the modification does not affect at all the currents of the vertical PNP, thus the injected substrate current remains the same and equal to $1.4mA$.

The improvement of the second layout configuration is however spatial dependent and it can be confirmed in spice simulators with the three dimensional substrate parasitic network. In Fig. 8 the results of the VerilogA model are reported monitoring the substrate potential beneath the well which is the region with the highest de-biasing. The difference of the two configurations leads to about $600mV$ improvement to reduce the substrate de-biasing. In conclusion the proposed substrate model can be used to investigate proper grounding scheme around critical parasitic PNP as an advantage with respect to classical BJT compact models and it allows to define the optimal guard ring width depending on the required specifications.

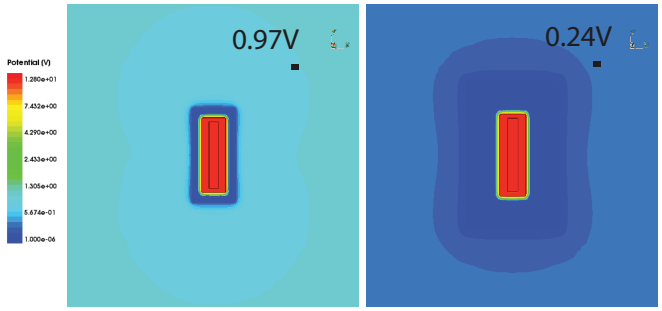

Fig. 7. TCAD surface potential distribution and substrate de-biasing with different guard ring geometries (left $4.5\mu m$ wide, right $14.5\mu m$ wide) for $I_E = 1.4mA$.

B. Effect of Backside Metallization

Another option for designers would be to add a backside contact to the chip. The model can be easily adapted to this technology option [17] if the parasitic Schottky diode present at the backside interface is neglected in first analysis

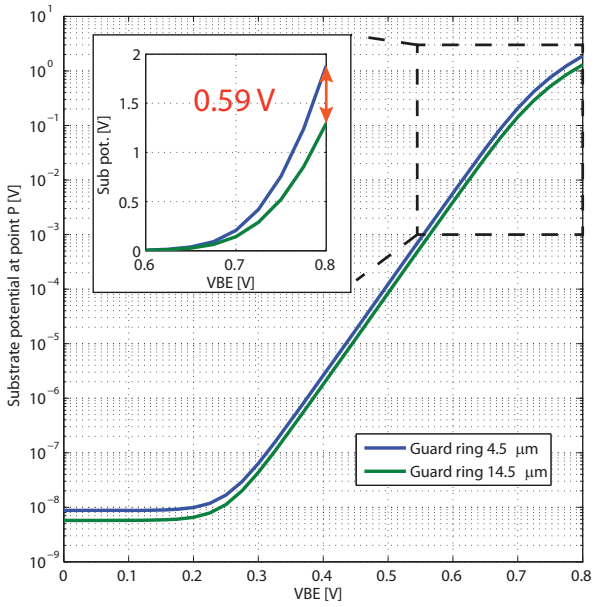

Fig. 8. Substrate potential shift beneath the DN well (point P of Fig. 5) predicted by the model as a function of biasing and guard ring.

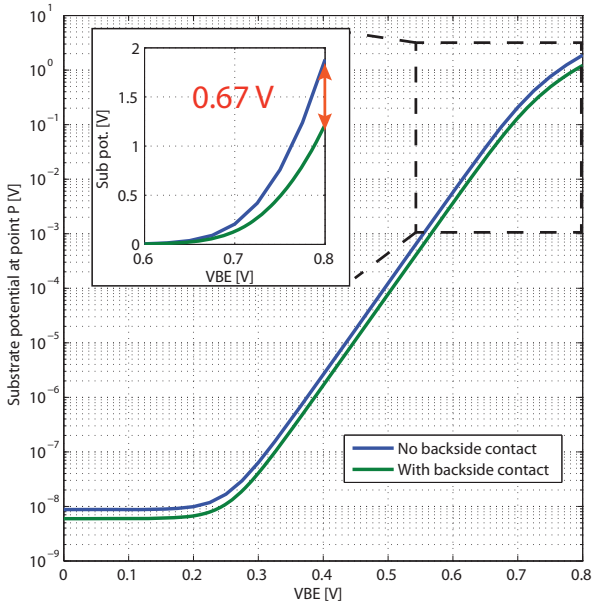

Fig. 9. Substrate potential shift beneath the DN well (point P of Fig. 5) predicted by the model as a function of biasing and backside contact.

[18]. Fig. 9 reports the model simulation of the potential de-biasing for the original structure in Fig. 4 with and without backside contact. Compared to Fig. 8, it can be noticed almost the same improvement of about 700 mV for the high current regime when backside metallization is present. For the selected example with low-doped substrate, this solution is then equivalent to the increment of 10 μm for the contact ring width.

This result can be easily explained because we are monitoring the potential shift under the N-well and the backside contact is 700 μm deep. Comparing the cross-section result of Fig. 10 (both TCAD and spice model) with Fig. 5, it is evident

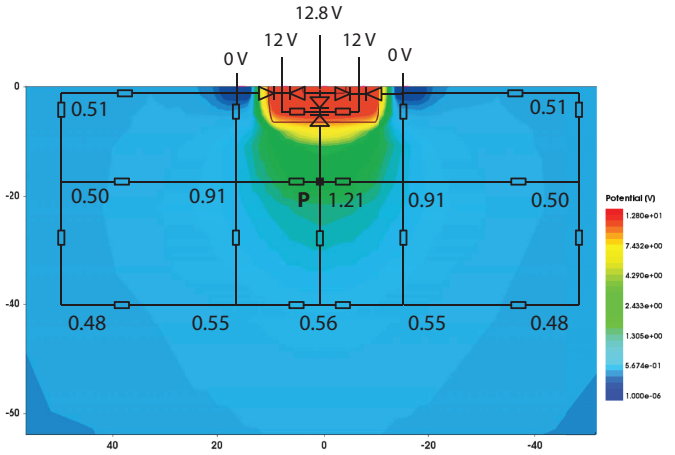

Fig. 10. Comparison between the potential shift simulated with TCAD (color plot) and the circuit results (numbers correspond to simulated node voltages) when the backside contact is present.

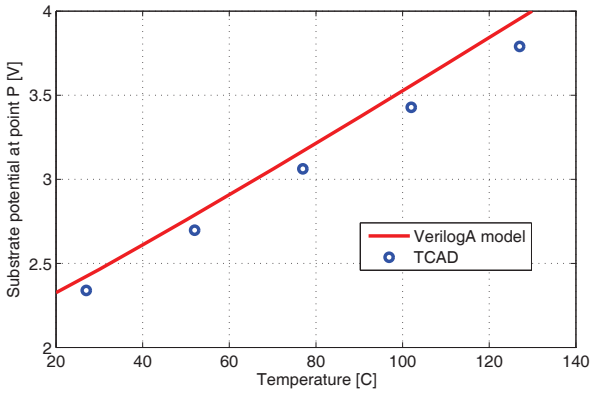

Fig. 11. Substrate potential shift beneath the DN well (point P of Fig. 5) predicted by the model as a function of temperature for $I_E = 2mA$.

that the backside contact maintains the substrate potential to lower values in the bulk of the silicon wafer reaching 0V at 700 μm depth (only the top 65 μm are shown). The top P+ contact rings keep instead the 0V only at the surface and the silicon bulk can reach higher de-biasing in the deeper regions.

C. Effect of Temperature

Also temperature must be investigated for power devices because it can have detrimental effects. As already shown in Fig. 3, the main result of temperature rising is the increase of injected substrate current. As a consequence also the potential shift is expected to increase. Moreover the substrate resistance exhibits a positive temperature coefficient (PTC) leading to even worst results. To validate the effects of temperature, TCAD and VerilogA simulations are compared in Fig. 11 for the potential beneath the N-well when a fixed current of 2 mA is injected into the substrate without backside contact. From about 2V potential shift at room temperature, the substrate de-biasing can double reaching 4V at 120C. It is therefore compulsory to check dangerous potential configurations at high temperatures by estimating the PTC of the substrate resistance. The proposed model is a valid solution for this objective.

V. Conclusion

This work shows how the EPFL substrate model based only on junctions and resistors with minority carriers is able to correctly take into account the vertical PNP BJT in HVCMOS devices. This allows to simulate substrate de-biasing with spice simulators during the design process. TCAD simulations are in good agreement with VerilogA model from low to high current injection levels at ambient and high temperature. The potential shift of the substrate can be in this way properly investigated by inspecting voltages output in the substrate network along the three dimensions. Despite the compact model, the results are layout dependent and allow to exploit also the best guard ring configuration to reduce substrate de-biasing when high-current is injected into the substrate. Finally, also the option of a backside metallization which helps to reduce the de-biasing can be quantified in spice environment and critical temperature variations can be predicted.

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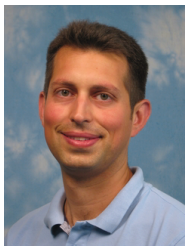

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