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LOW VOLTAGE, HIGH-SPEED FOUR-QUADRANT CMOS TRANSCONDUCTANCE MULTIPLIER

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Summary: The paper presents an analog four-quadrant transconductance multiplier designed in CMOS technology, suitable for low voltage and operating at high-speed. The transconductance multiplier with Gilbert-like architecture uses a cascade of a combination of two linear current dividers implemented by means of the differential pairs to produce a linear dependence between the tail current and the two output currents. To adopt the circuit for low voltage, simple current mirrors have been applied to couple the first- and the second stage of the current dividers cascade. High-speed operation is possible thanks to simple architecture of building blocks using RF CMOS transistors with sufficiently large biasing currents. A complete circuits schematic with input driving peripherials, as well as simulation results of entire multiplier have also been presented.

Keywords: analog VLSI, four quadrant multiplier, CMOS

1. INTRODUCTION

The analog multipliers are versatile building blocks, desired in many applications including continuous time signal processing, automatic variable gain amplifiers, neural networks, and as mixers and modulators in communication systems. They are widely used in contemporary VLSI chips for modulation/demodulation, other non-linear operations including division, square rooting as well as frequency conversion.

The most popular implementation of a four-quadrant multiplier, proposed in the bipolar technology in late 1960's [3], is the famous *Gilbert cell*, which is still the backbone of many different improvement architectures of the contemporary multipliers. The Gilbert cell can be considered as a combination of linear current dividers, implemented by means of a two stage cascode of differential pairs. Each of the differential pairs produces a linear dependence between its tail current and its two output currents. The output currents difference $i_{C1} - i_{C2}$ for bipolar long tail pair is given by:

$$i_{C1} - i_{C2} = I \cdot \mathrm{tgh}(v_X/\varphi_T) \approx I \cdot v_X/\varphi_T \tag{1}$$

where φ_T is the thermal voltage, I is the tail current of the differential pair; for small input differential voltage tgh function may be approximated by its argument itself.

For the bipolar differential pair, linearity with respect to I is guaranteed by the linear dependence g_m versus I (g_m is the transistors' transconductance), which holds with accuracy over an I range of several decades. Linearity with respect to the v_Y port, for the "upper" stage of the Gilbert cell, is obtained by proper pre-distortion of the input voltage.

In contrary to bipolar technology, long channel MOSFETs based Gilbert cell implementations have another features. Using the square law relationships (valid for long channel MOSFETS in strong inversion), the currents difference $i_{D2} - i_{D1}$ is given by:

$$i_{D2} - i_{D1} = \frac{I}{2}\sqrt{\frac{\beta \cdot v_X^2}{I} - \frac{\beta^2 \cdot v_X^4}{I^2}} \approx v_X \sqrt{\beta \cdot I} \tag{2}$$

The approximation used in (2) is also valid only for small differential input voltage. Linearity with respect to I is not guaranteed, because opposite to bipolar devices, a long channel MOSFET's transconductance depends on the square root of the bias current:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W \cdot I_D}{L}} \tag{3}$$

and this relationship points that input signal of the long channel MOSFET counterparts of Gilbert cell is much more limited and the output current swing may be only very small fraction of the bias value. Of course it is possible to use the body driven, or weak inversion MOSFETs structures [7] to imitate bipolar devices, but in this case we obtain significantly worse frequency response, and very small usable output current range.

Contrary to a long channel MOSFET, for the short channel one, the $V_G - I_D$ relationship becomes rather linear than square-type, especially for higher drain current. If the difference $V_G - V_T/L$ becomes significantly larger than E_{sat} (being the field at which carrier velocity drops to half the value extrapolated from low-field mobility, the drain current approaches the value of:

$$I_D = \frac{\mu_n C_{ox}}{2} W (V_{GS} - V_T) E_{sat} \tag{4}$$

and thus short channel MOSFET transconductance is proportional to the drain current:

$$g_m = \frac{\mu_n C_{ox}}{2} W E_{sat} = \frac{I_D}{(V_{GS} - V_T)} = \frac{I_D}{V_{Dsat}} \tag{5}$$

and consequently differential pair comprising such a MOSFETs may have properties similar to that of its bipolar counterpart.

Anyway it should be noted, that CMOS implementation of Gilbert cell architecture – double cascode of differential pairs combination comprise a stock of at least four transistors in the saturation region and therefore its supply requirement usually touches and sometimes even exceeds allowed value for most of contemporary CMOS processes.

In the paper we present four-quadrant transconductance multiplier in Gilbert-like architecture using a two stage cascade of a combination of the differential pairs with short channel MOSFETs. The complete implementation including driving circuits, suitable for low voltage and high speed operation have been also presented.

2. PRINCIPLE OF OPERATION

Fig. 1 shows a block diagram of a four-quadrant transconductance multiplier in Gilbert-like architecture, implemented as a two stage cascade of a small signal transconductors combination. This block diagram follows the idea presented already in [4] more recently used also in [2]. In our solution however, current mirrors have been applied to transfer two output currents of the first transconductor to next stage ones, as tail currents of two differential pairs. The output currents of the first stage fully differential transconductor, I_1 and I_2 in Fig. 1, are related to a common mode current I_{SS} and a differential component $G_m v_Y$, according to:

$$I_1 = \frac{I_{SS}}{2} + \frac{1}{2} G_m v_Y \; ; \; I_2 = \frac{I_{SS}}{2} - \frac{1}{2} G_m v_Y \; . \tag{6}$$

These two outputs currents, coupled by simple current mirrors, create the tail currents for the two small signal transconductors in the next stage of the current divider, which are controlled by v_X input voltage and have transconductances of g_m. From (5) and (6), we easily get the output differential current of the multiplier:

$$\begin{aligned} i_{OUT} &= i_{OUT1} - i_{OUT2} = (I_3 + I_6) - (I_4 + I_5) = \\ &= (I_3 - I_4) - (I_5 - I_6) = \frac{G_m v_Y v_X}{V_{Dsat}} \end{aligned} \tag{7}$$

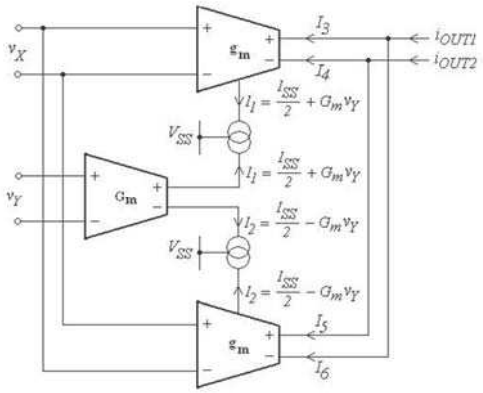

Fig. 1. Block diagram of a four-quadrant transconductance multiplier in Gilbert-like architecture

The block diagram of Fig. 1 has been implemented with transcoductors based on differential pairs with CMOS transistors biased with sufficiently large currents. The schematic of the proposed multiplier circuit is shown in Fig. 2. Because the proposed solution of the multiplier architecture is dedicated rather for high frequency applications, therefore the driving of all the differential pairs should be symmetrical. To achieve this, the additional inverting voltage amplifiers for v_X and v_Y signals have been applied.

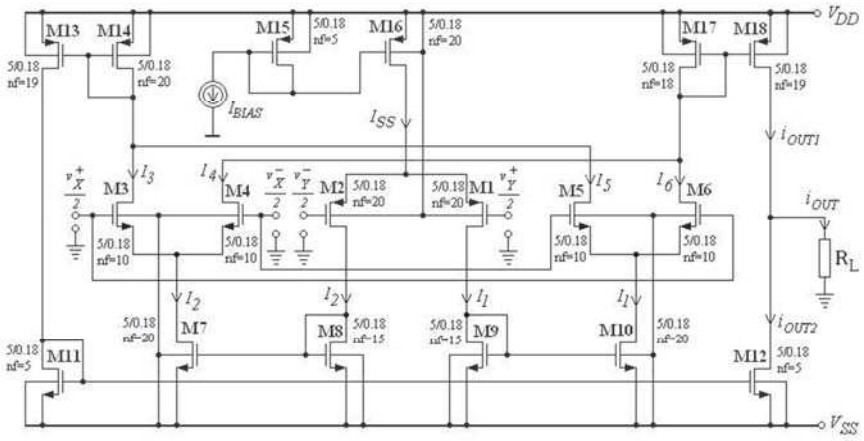

Fig. 2. The schematic of the proposed multiplier circuit

They have the form of simple CMOS inverter (M1, M2) with complementary diode connected transistors load (M3, M4) (Fig. 3). From small signal perspective this circuitry is a transconductor loaded with the same transconductor with shorted input and output ports. Thus resulting voltage gain is –1.

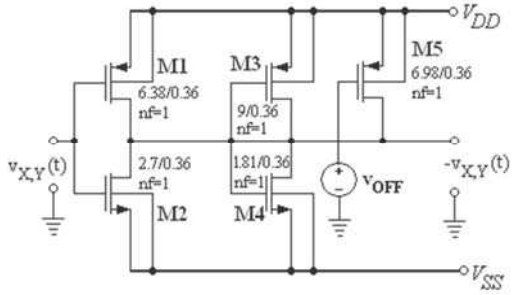

Fig. 3. The schematic of the auxiliary inverting voltage amplifier

It is known that n-MOS conventional long tail pair has better performance (in terms of input swing and linearity) if common mode of the input signal is shifted closer to VDD, especially for lower supply voltages. Therefore M5 transistor has been added (Fig. 3) to perform an appropriate signal conditioning. On the other hand the possibility of aforementioned level shifting may be used for classical offset compensation. The output offset is a consequence of an unmatched threshold voltages of p-MOS and n-MOS in the inverter.

3. SIMULATIONS RESULTS

Circuit-level design and simulation, circuit layout, post-layout verification for UMC's 180 nm CMOS process has been done on the base Foundry Design Kit in the Cadence DF II environment, available via EUROPRACTICE.

Layout of the completely CMOS transconductance multiplier circuit, containing also the input inverting amplifiers, and utilizing the 18RF_NMOS and 18RF_PMOS cells of the UMC's 180 nm CMOS FDK, is shown in Fig. 4. Circuit has been simulated assuming symmetrical +0.9/-0.9 Volt supply (both n- and p-MOSFETs' threshold voltage is about 0.5 Volt). All the presented simulations have been done with postlayout extracted netlist and without I/O cells.

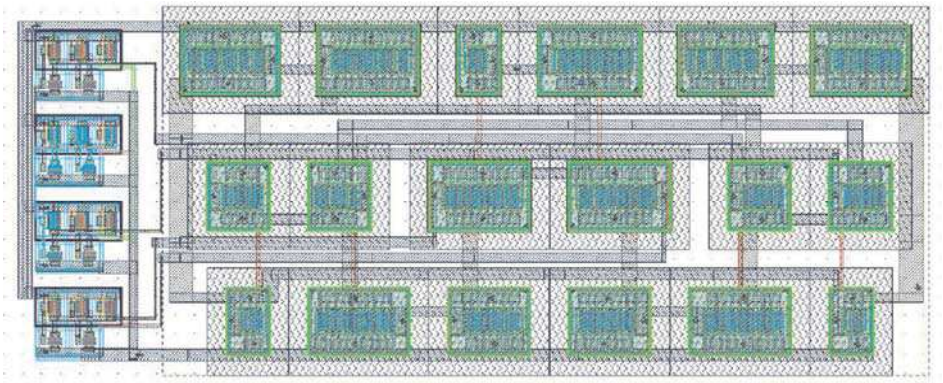

Fig. 4. The entire circuit laid out in UMC 180 nm CMOS technology

Figures 5 and 6 present the DC and small-signal characteristics of the inverting amplifier, respectively. The implementation of such auxiliary yet important building block is no so obvious, so quite satisfactory simulated performance are vital for the rest of the project. From Fig. 5 it can be seen that DC response is linear in the range almost twice wider than required to control the inverting input of the differential pair, while the small signal analysis results indicate relatively wideband response – the 3-dB corner frequency slightly exceeds 3GHz while THD is less than 0.5% at 100 MHz for 200 mV_{P-P} input signal.

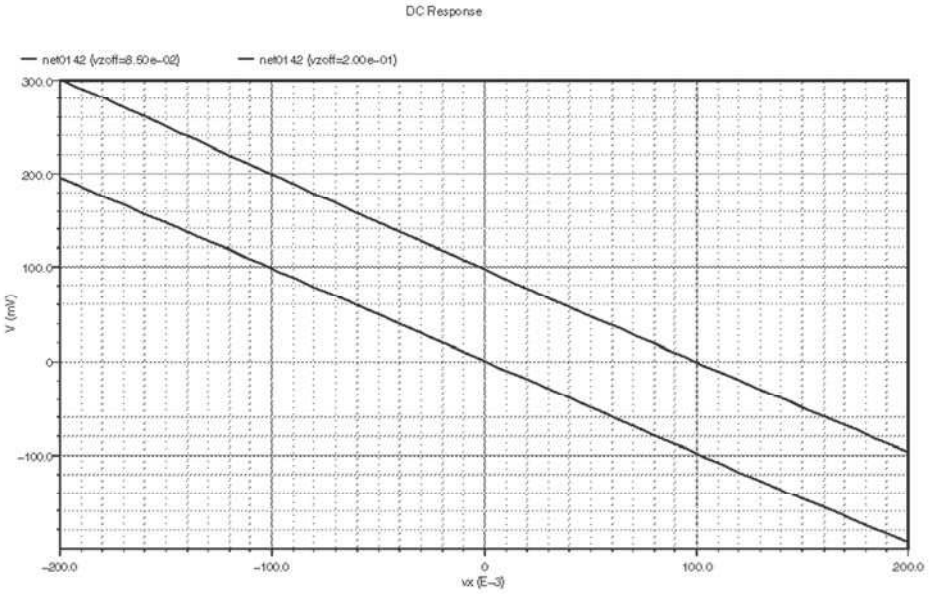

Fig. 5. Simulated DC characteristics of auxiliary voltage inverter

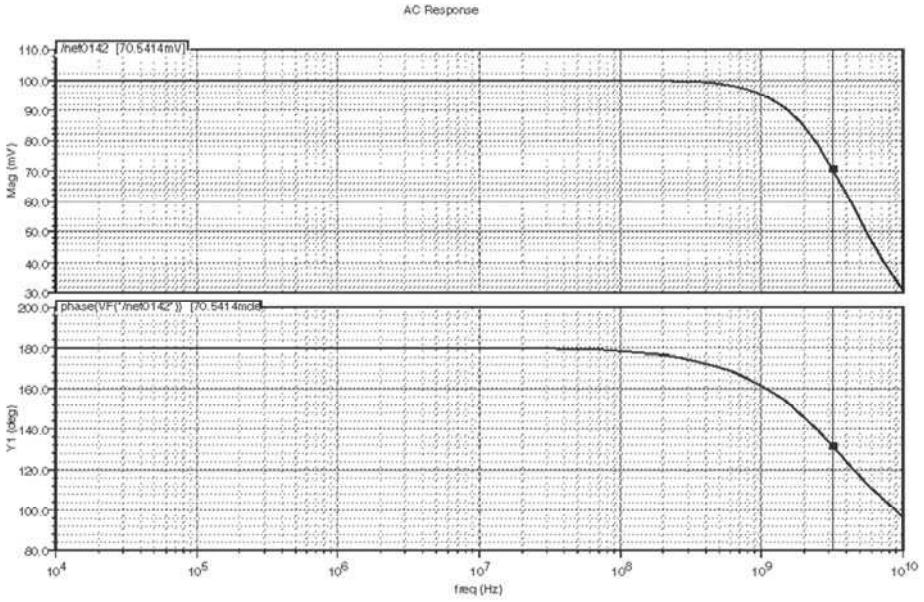

Fig. 6. Small signal characteristics: magnitude and phase of auxiliary voltage inverter

Fig. 7 shows the DC transfer characteristics families for the complete multiplier circuit: $i_{OUT} = f(v_X)$ while $v_Y = \text{const}$ and Fig. 8 $i_{OUT} = f(v_Y)$ while $_X = \text{const}$, respectively. In both cases, one input voltage was swept from –100 mV to 100 mV, while the other one was stepped from –100 mV to 100 mV by 50 mV.

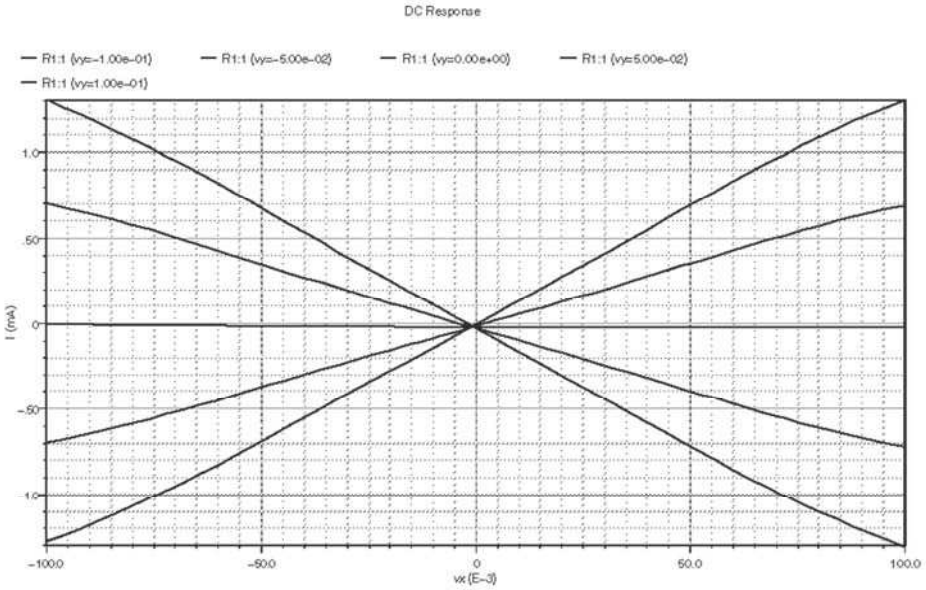

Fig. 7. Simulated DC transfer characteristics families of the complete multiplier circuit: $i_{OUT} = f(v_X)@v_Y = \text{const}$

Comparing this two families of curves, shown in Fig. 7 and 8, we see, that transistor's transconductances of the differential pair for input v_Y signal are proportional to their drain currents and guarantee a linear dependence between the differential pair tail current and its two output currents. To meet this condition, the tail current of the differential pair for input v_Y signal is equal 1.4 mA and RF transistors with minimum channel length L = 0.18 um have been applied.

The transfer characteristics of the multiplier are linear in the range from –100 mV to 100 mV (the full differential pair input signal is 200 mV). For $|v_X|$, $|v_Y| < 100$ mV, the integral linearity error of the multiplier is less than 0.5%. This value increases to about 1.5% for $|v_X|$ and $|v_Y|$ equal to 150 mV; which covers about 16% of the supply voltage.

Total harmonic distortion with 100 mV_{P-P} input signal at either input terminal with ± 50 mV DC-voltage at the other is less than 0.25% up to 100 MHz and increases to 1% at 500 MHz.

In Fig. 9 AC magnitude frequency response of the multiplier are depicted. From simulation in this domain comes that multiplier 3 dB bandwidth reaches almost 1 GHz.

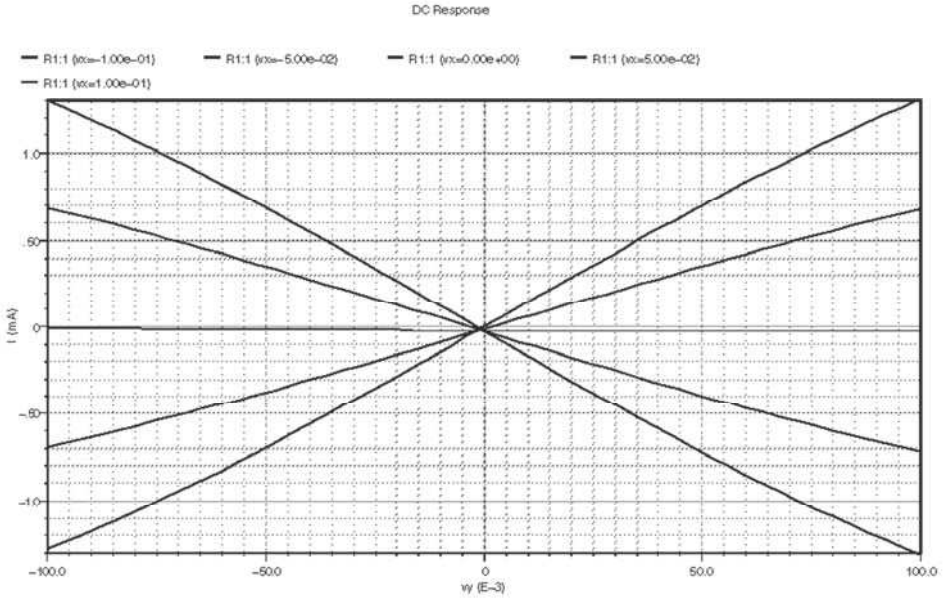

Fig. 8. Simulated DC transfer characteristics families of the complete multiplier circuit: $i_{OUT} = f(v_Y)@v_X = \text{const}$

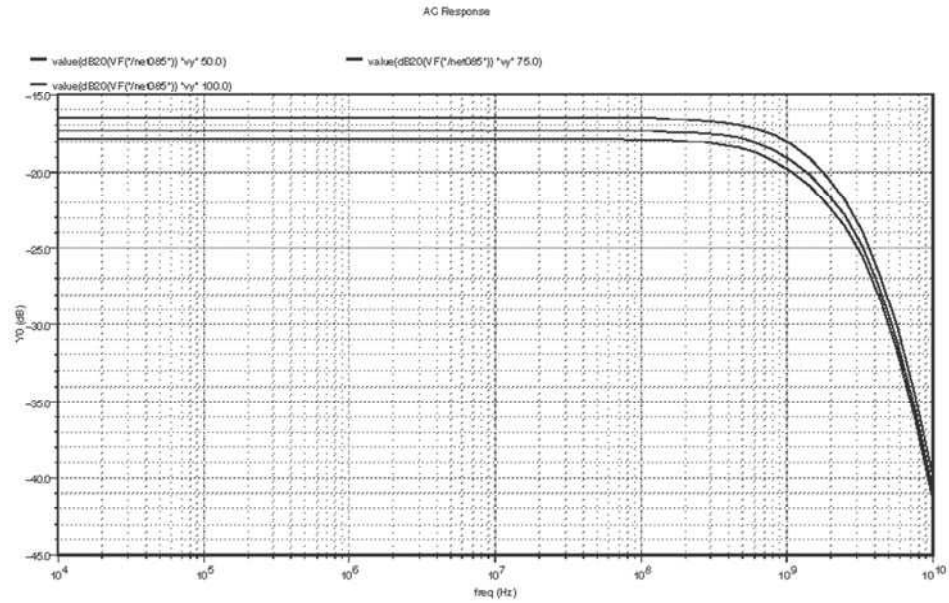

Fig. 9. Simulated AC response of the whole multiplier

Fig. 10 shows transient simulation results for different frequency sinewaves attached to both inputs – and we observe modulation of 100 MHz carrier by 2 MHz signal.

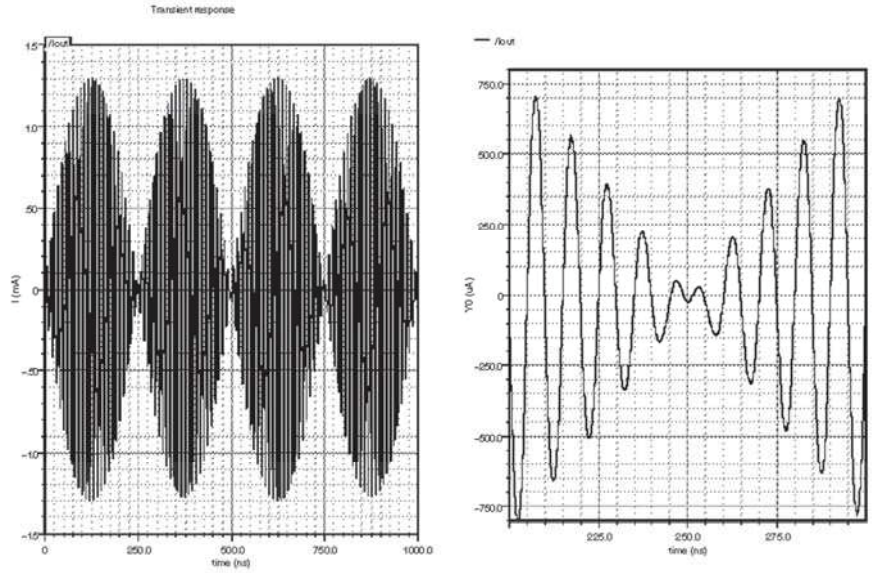

Fig. 10. Transient response for different input frequency AM modulation

Finally Fig. 11 illustrates transients for the mutliplier working in phase-and coincidence detector.

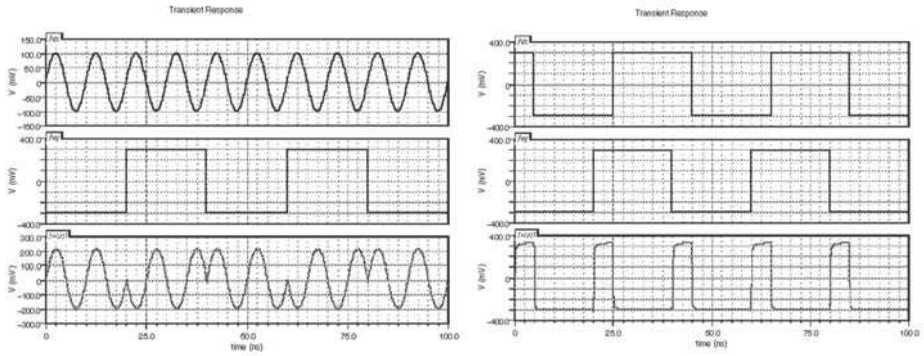

Fig. 11. Simulated transient responses: large signal at one input – phase detector (left) and both inputs overdrive – coincidence detector (right)

4. CONCLUSIONS

An analog four-quadrant CMOS transconductance multiplier in Gilbert-like architecture has been proposed. It is particularly suited for high-speed application due to its cascade architecture composed of very simple building blocks using RF CMOS transistors with sufficiently large biasing currents and may be applicable particularly in RF circuits as mixers, modulators/demodulators in communication systems. The most important benchmarks of the circuit are: quiescent current of 3.5 mA and 3 dB bandwidth

of 1 GHz. The described implementation requires a stock of at most three transistors in saturation region, so it is well suited for low voltage applications.

Both aforementioned features make our proposal an intersting alternative for another already known circuit solutions. The circuit has been sent for manufacturing by Europractice, we received back the fabricated prototypes and preliminary measurements confirm the proper operation of the circuits. An extended test plan including offset, temperature drits as well as HF performance measurements is currently in progress.

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NISKONAPIĘCIOWY SZYBKI CZTEROĆWIARTKOWY TRANS-KONDUKTANCYJNY UKŁAD MNOŻĄCY W TECHNOLOGII CMOS

Streszczenie

W artykule zaprezentowano szybki niskonapięciowy czteroćwiartkowy układ mnożący zaprojektowany w technologii CMOS. Architektura układu oparta jest o strukturę typu Gilberta. W układzie zastosowano kaskadowe połączenie dwóch stopni transkonduktancyjnych zrealizowanych w oparciu o pary różnicowe. Aby układ mógł pracować w zakresie niskich napięć zasilających poszczególne stopnie zostały sprzęgnięte przy pomocy prostych luster prądowych. Duża szybkość działania została osiągnięta dzięki prostej architekturze układu oraz zastosowaniu tranzystorów RF pracujących przy odpowiednio dużych wartościach prądów. W pracy zaprezentowano również wejściowe niskonapięciowe bloki pomocnicze oraz wyniki symulacji kompletnego układu mnożącego.

Słowa kluczowe: analogowe układy VLSI, czteroćwiartkowy układ mnożący, technologia CMOS