Power Electronics and Drives
3(38), No. 1, 2018 DOI: 10.2478/pead-2018-0015

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Power Electronics and Drives

Extended T-type Inverter

Research Article

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Received May 23, 2018; Accepted July 25, 2018

Abstract: This paper presents a new concept for a power electronic converter – the extended T-type (eT) inverter, which is a combination of a three-phase inverter and a three-level direct current (dc)/dc converter. The novel converter shows better performance than a comparable system composed of two converters: a T-type inverter and a boost converter. At first, the three-level dc/dc converter is able to boost the input voltage but also affects the neutral point potential. The operation principles of the eT inverter are explained and a simulation study of the SiC-based 6 kVA system is presented in this paper. Presented results show a serious reduction of the DC-link capacitors and the input inductor. Furthermore, suitable SiC power semiconductor devices are selected and power losses are estimated using Saber software in reference to a comparative T-type inverter. According to the simulations, the 50 kHz/6 kVA inverter feed from the low voltage (250 V) shows $<2.5\%$ of power losses in the suggested SiC metal oxide–semiconductor field-effect transistors (MOSFETs) and Schottky diodes. Finally, a 6 kVA laboratory model was designed, built and tested. Conducted measurements show that despite low capacitance ($2 \times 30\ \mu F/450\ V$), the neutral point potential is balanced, and the observed efficiency of the inverter is around 96%.

Keywords: *Multilevel inverter • T-type inverter • Boost converter • Silicon carbide*

1. Introduction

Power electronic interfaces between low-voltage sources and three-phase loads or supply grids belong to an area of intense research work due to the expanding application fields of renewable energy sources and energy storages (Abu-Rub et al., 2014). Among the various considered topologies, multilevel converters can be found due to lower voltage stress and reduced filter size (Abu-Rub et al., 2014). Limited problems with leakage currents in photovoltaic (PV) systems are also an advantage of the multilevel inverters that include the three-level T-type topology (Schweizer and Kolar, 2013; Uemura et al., 2013). Moreover, new wide bandgap semiconductors are also considered in order to improve system performance in terms of efficiency and power density. As transistors are usually preferable over diodes in SiC-based converters due to the lower voltage drop, a standard neutral point clamped (NPC) topology seems to be outdated and other circuits such as an active NPC with transistors in parallel to diodes or the T-type topology are discussed (Anthon et al., 2016a, 2016b; Furusho and Fuji, 2016; Gurpinar and Castelazzi, 2015; Gu et al., 2015; Shi et al., 2016, 2017). This structure has been selected to design and build a multilevel converter presented by Rąbkowski et al. (2017), wherein extremely good features of SiC transistors were confirmed.

In this paper, the authors propose to combine two multilevel topologies: a three-phase T-type inverter with a three-level direct current (dc)/dc converter (Grbovic et al., 2012; Rąbkowski et al., 2002). The resulting system may be named as the 'extended T-type' (eT) inverter. The basic idea of the system, operation principles, simulation and experimental study of the 6 kVA SiC-based laboratory model is presented. Moreover, an estimation of power losses in SiC metal oxide–semiconductor field-effect transistors (MOSFETs) and Schottky diodes is shown in reference to a standard structure: the T-type inverter and the conventional dc/dc boost converter.

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2. Integration of a three-level dc/dc converter with the T-type inverter

Similarly to other multilevel voltage-fed topologies, the T-type inverter shows step-down characteristics, which means that the DC side voltage is higher than the peak-to-peak line output voltage. Therefore, a transfer of electrical energy from low-voltage sources to the grid or the alternating current (AC) loads requires an additional, boost conversion stage. The most obvious solution is to apply a standard boost converter as presented in Fig. 1 (Furusho and Fuji, 2016; Shi et al., 2016, 2017), but in this paper, a more sophisticated approach is presented. Aiming to include the extended features of the system, a three-level dc/dc converter is applied across the DC side capacitors in the same manner as presented in previous studies (Grbovic et al., 2012; Rąbkowski et al., 2002); see the scheme presented in Fig. 2. The neutral point of the inverter N is connected to the middle point between the two transistors $\mathrm{T_L}$ and $\mathrm{T_H}$, while the negative and positive poles of the inverter are connected to the dc/dc converter output. The additional converter may boost the input voltage U similarly to the dc/dc converter in Fig. 1, but the output voltage may be the sum of two or just one of the two capacitors. Thus, the duty ratio may be lower, and the voltage stress across the input inductor $\mathrm{L_{DC}}$ is also decreased. Moreover, it leads to reduction of the inductance and the size of the inductor. In addition to this, the additional dc/dc converter may choose the capacitor to cooperate with, and balancing of the neutral point potential is possible. With this feature, the size of the capacitors $\mathrm{C_H}$ and $\mathrm{C_L}$ may be seriously decreased.

Finally, a basic version of the eT inverter is unidirectional (Fig. 2), but after replacing the diodes with SiC MOSFETs, the system becomes bidirectional, and energy may be also transferred from the AC output to the DC source U.

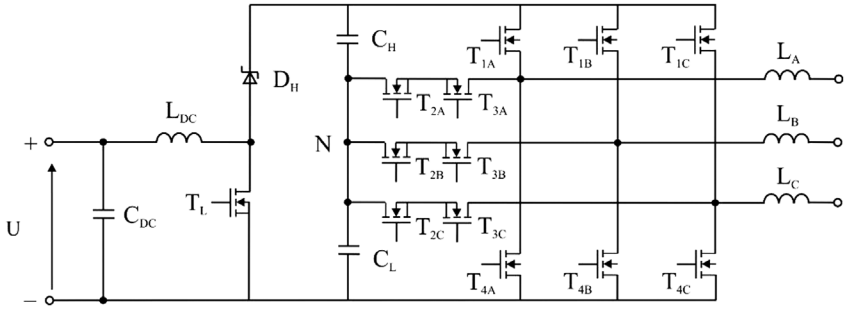


Fig. 1. T-type inverter with the dc/dc boost converter.

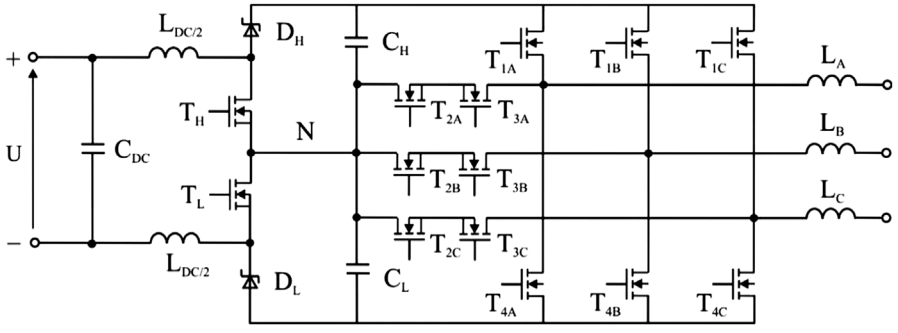


Fig. 2. Extended T-type inverter (unidirectional version).

3. Operation principles

The three-phase T-type inverter may be controlled with the use of any known pulse width modulation (PWM) strategy, while the additional dc/dc converter operates on the basis of four switching states from A to D, shown in Fig. 3 and collectively represented in Table 1. In the switching state A, both $\mathrm{T_H}$ and $\mathrm{T_L}$ are turned on, and the energy

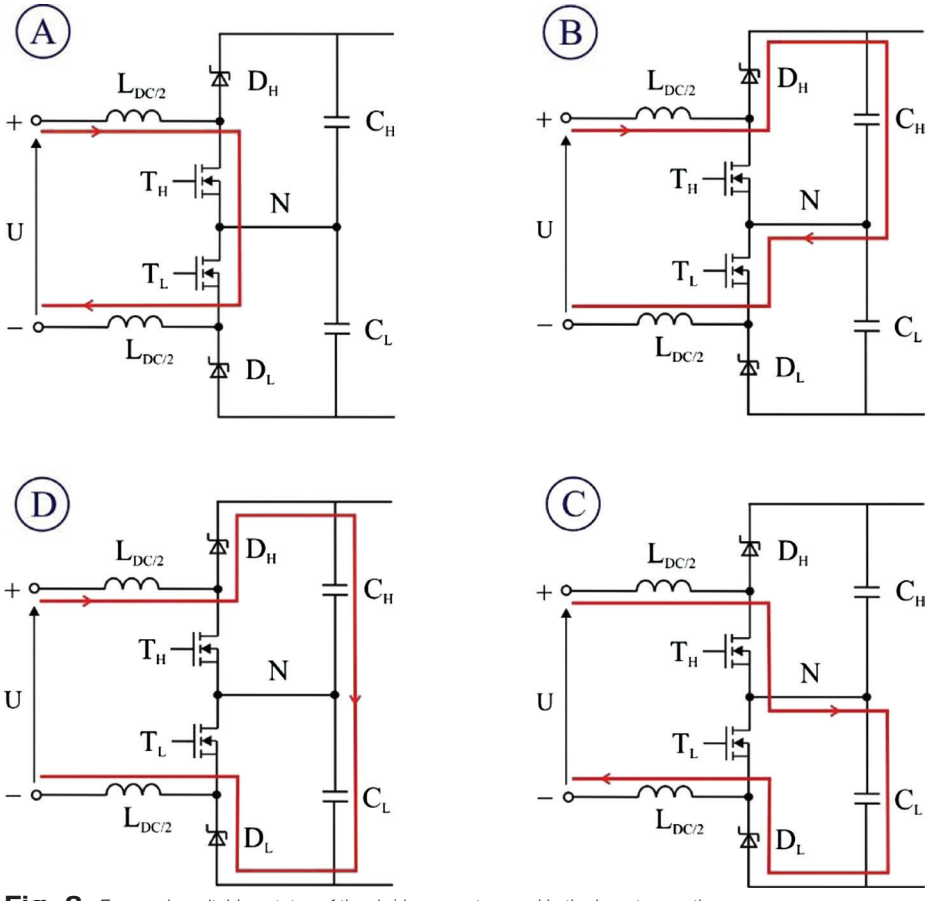


Fig. 3. Four main switching states of the dc/dc converter used in the boost operation.

Table 1. Switching states of the dc/dc converter

State	T_H	D_H	T_L	D_L	Status
A	1	0	1	0	Energy stored in the inductor
B	0	1	1	0	Charging of the capacitor C_H
C	1	0	0	1	Charging of the capacitor C_L
D	0	1	0	1	Charging of the capacitor C_L and C_H

is stored in the input inductor L_{DC} in a similar way as in the standard boost converter. Therefore, the output voltage of the dc/dc converter may be higher than the input voltage source for the eT converter. Then, the dc/dc converter may be switched into one of the three states B, C or D to transfer energy towards the output (DC link of the T-type inverter). During operation modes B and C (either T_H or T_L is turned on: see Table 1), the inductor current is charging either one of the DC-link capacitors C_L or C_H. Thus, alternating operation between these two states enables neutral point voltage balancing. During the fourth possible state D (none of the transistors is conducting – Table 1), the inductor current flows to the series-connected DC-link capacitors; therefore, the output voltage is two times higher than in states B and C. However, it is possible to switch between states A and D, but a crucial feature, namely, neutral point voltage balancing, is not available. Therefore, the proposed operation principle is based on switching between states A and B or C, taking into account the voltages across the DC-link capacitors.

Similarly to the standard boost dc/dc converter, various control schemes may be applied, from hysteresis control to standard PWM with constant switching frequency. Typical switching sequences for the PWM control are shown in Fig. 4. Boost operation in state A is predetermined on a constant duty cycle depending on the input voltage and required DC-link voltage. The second state B or C is chosen according to the voltage levels between the two DC-link capacitors, so that the one with lower voltage is being charged through the transistor and the diode.

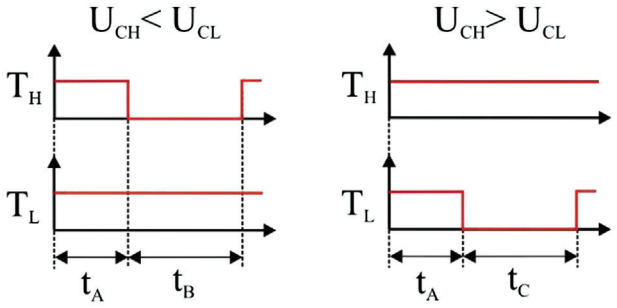


Fig. 4. Possible switching sequences of the dc/dc converter to control the neutral point potential.

The additional dc/dc converter shows boost characteristics (U_{CH} and $U_{CL} > U$) and, without the use of state D, cooperates with one of the two capacitors C_H or C_L. A boost ratio may be defined as follows:

$$B = \frac{U_{CH} + U_{CL}}{U} \tag{1}$$

Using a duty ratio of the dc/dc converter *d* defined as follows:

$$d = \frac{t_A}{T_S} \tag{2}$$

and the well-known equation for boost converter operating at continuous current, the boost ratio may be expressed as follows:

$$B = \frac{2}{1-d} \tag{3}$$

This leads to the following expression:

$$U_{CH} + U_{CL} = \frac{2U}{1-d} \tag{4}$$

and a conclusion that B is always >2 (operation without the state D). Let us assume a maximum duty ratio $d = 0.5$ and typical DC-link voltages of the grid-connected converters (European grid) in the range of 650–800 V. The input voltage U may be in the range of 160–400 V DC. When the input voltage U is expected to be higher (i.e. up to 850 V), the dc/dc converter has to switch into operation without the states B and C. But this may be considered a drawback as the system is losing the neutral point potential balancing feature. Note that the reference system presented in Fig. 1 may operate in a similar operation range, but higher duty ratios are necessary as the output voltage of the dc/dc converter is always equal to the DC voltage of the inverter.

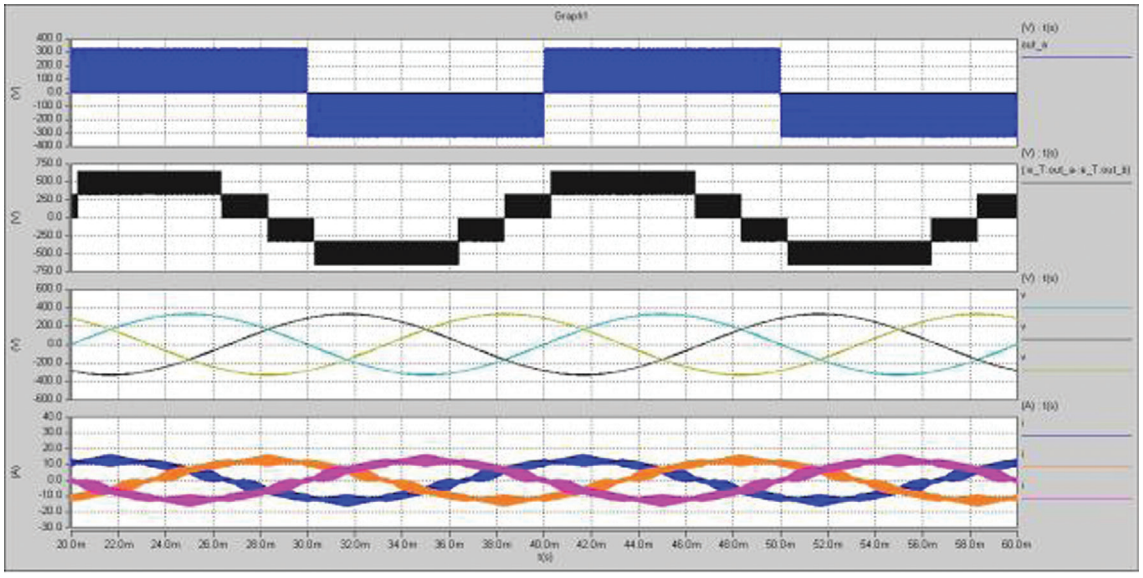
4. Simulation study

The 6 kVA eT inverter connected between the DC voltage source and the three-phase resistive load was simulated using Saber software. As a reference system, the T-type inverter with a dc/dc boost converter was simulated under the same conditions: all transistors were switching at 50 kHz, and suitable parameters of the passive components were selected for both systems (Table 2). While the output LC filter is exactly the same, the passive elements of the dc/dc converter are smaller in the eT inverter, especially, the DC capacitors are one order of magnitude smaller than in the reference solution. This feature can be recognised as one of the main advantages of the discussed system, possibly due to the active neutral point balancing performed by the dc/dc converter. Moreover, the necessary inductor of the additional dc/dc converter (selected to obtain current ripples below 5A peak) is also 2.5 times lower than in the regular dc/dc boost converter (Table 2). A higher amount of semiconductor devices is, therefore, compensated by the significant reduction of the passive components in the eT topology.

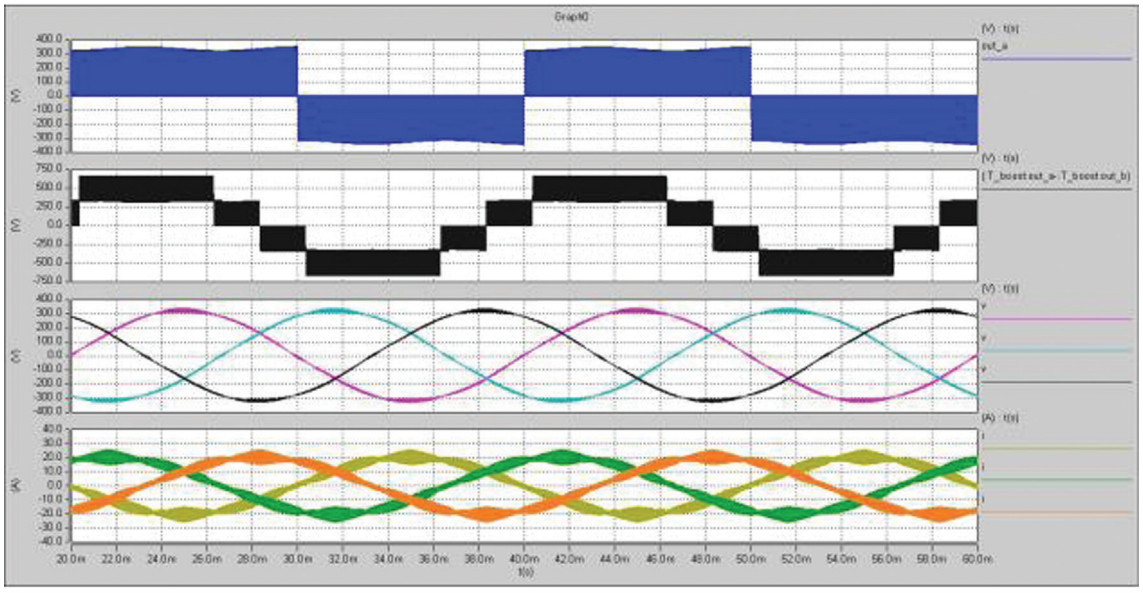
The three-phase T-type section was controlled in an open loop with a standard sinusoidal modulation with addition of the third harmonic component for both compared structures. Specific waveforms recorded during simulation of eT inverter at nominal power of 6 kVA are presented in Fig. 5a. It can be seen that the inverter is

Table 2. Parameters of the simulation model

Parameter	S_N	U	U_{AC}	f_S	L_{DC}	$C_H = C_H$	L_F	C_F
Topology	kVA	V	V	kHz	µH	µF	µH	µF
T+dc/dc	6	250	3 × 400	50	630	420	100	1
eT	6	250	3 × 400	50	2 × 130	30	100	1



(a)

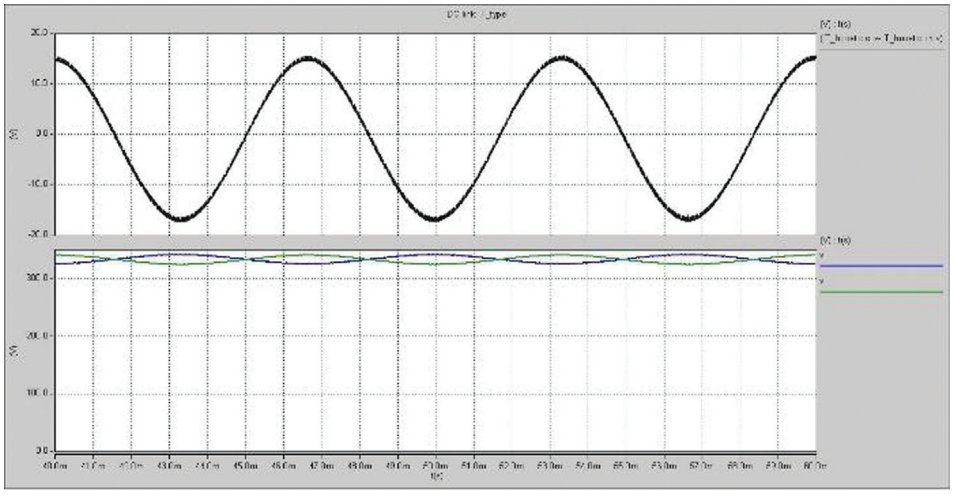


(b)

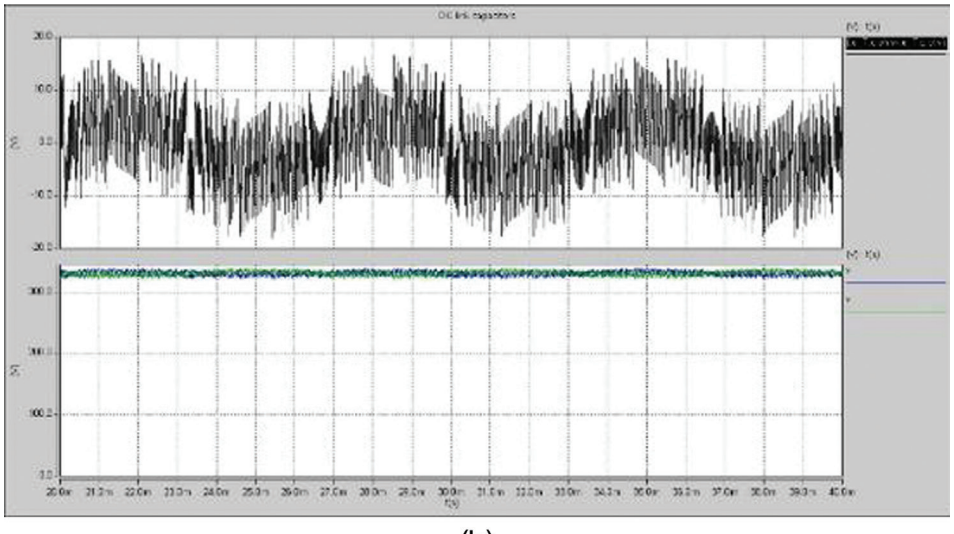
Fig. 5. Simulated output waveforms of the e T-type inverter (a) and standard T-type inverter (b) at $f_S = 50$ kHz and $S = 6$ kVA; from the top, output voltage in reference to neutral point N, phase-to-phase voltage, three output voltages and three inductor currents.

operating correctly and the applied LC filter provides low distortions at the three-phase output: the measured total harmonic distortion (THD) of the output voltages is <1.5%. Exactly the same waveforms were observed in Fig. 5b for the reference system with the boost converter, where modulation method, voltage levels and filter size were similar.

Furthermore, Fig. 6 compares the behaviour of the two systems in terms of the neutral point potential. In the case of the standard T-type inverter, voltages across the DC-link capacitors are changing with the triple fundamental frequency (150 Hz) with amplitude related mostly to capacitance (Fig. 6a). Comparable eT inverter with significantly lower capacitance and active balancing shows similar fluctuation of the neutral point potential (Fig. 6b) but, besides the 150 Hz component, high-frequency ripples are observed due to operation of a simple hysteresis controller. This issue may be better explained on the basis of Fig. 7, which shows operation of the dc/dc converter at the input voltage $U = 250\text{V}$ with a constant duty ratio $d = 0.25$ ($B = 2.5$). Switching signals of the transistors in Fig. 7 show that in every switching period, the controller is changing state due to the low value of the applied capacitance. Thus, after state A, state B or C is being selected alternately.



(a)



(b)

Fig. 6. Neutral point voltage (top) and voltages across the capacitors C_H and C_L (bottom) for the T-type inverter with a dc/dc boost (a) and the e-Type inverter (b): operation at $f_s = 50$ kHz and $S = 6$ kVA.

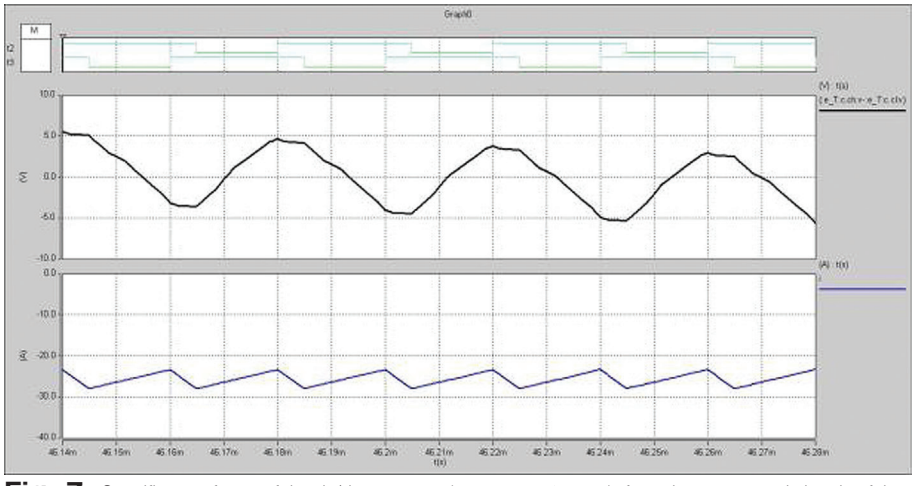


Fig. 7. Specific waveforms of the dc/dc converter ($U = 250$ V, $d = 0.25$); from the top: control signals of the transistors, difference of the capacitor voltages and the inductor current.

5. Power loss estimation

Further simulations were performed on the basis of the 6 kVA eT-type inverter model in order to select semiconductor devices and estimate power losses in these elements. Only SiC power semiconductors were taken into account – MOSFETs and Schottky diodes. For the expected voltage levels (up to 850 V DC), two groups of elements may be distinguished – main bridge transistors (T_{1A}, T_{1B}, T_{1C} and T_{4A}, T_{4B}, T_{4C}), which are rated at 1200 V, and the remaining elements, which may be rated at two times lower voltage due to the multilevel structure of the inverter. Another assumption was not to use anti-parallel diodes in the inverter as MOSFET body diodes perform switching operations quite well and, therefore, the number of devices may be decreased. The reference dc/dc converter was equipped with 1200 V devices, a transistor and a diode. In the first set of simulations for $d = 0.25$ ($U = 250$ V), currents in all semiconductor devices were measured. Then, specific semiconductor devices were selected (Table 3).

After introduction to Saber static and dynamic characteristics of the devices, power losses were measured. It was assumed that all junction temperatures are equal to 100°C. Results of this simulation, presented in Table 4, show that total power losses of the eT inverter and the T-type inverter with the boost converter are very close (both at approximately 145 W). Power losses are slightly higher in dc/dc converters (88 W) than in the T-type bridge (57 W). Taking into account the operating conditions, namely, the two-stage conversion from $U = 250$ V at input current of 24 A, the obtained result (<2.5% power losses) may be considered very promising. Moreover, the amount of power losses per device is, excluding boost diodes (D_H and D_L), rather low, and the junction temperature most likely will be lower than the assumed $T_J = 100°C$. Thus, reduction of the on-state losses is expected in reference to the numbers presented in Table 4, even with quite small heatsink. Moreover, when the input voltage will be increased, power

Table 3. Parameters of the applied semiconductor devices ($T_J = 100°C$)

Elements	Type	On-state resistance	Turn-on energy	Turn-off energy
		T-type inverter		
T_{1n}, T_{4n}	C2M0040120D	54 mΩ	1 mJ	0.4 mJ
T_{2n}, T_{3n}	C3M0065090D	75 mΩ	226 µJ	36 µJ
		Standard dc/dc boost		
T_L	C2M0040120D	54 mΩ	1 mJ	0.4 mJ
D_H	C4D40120D	48 mΩ	-	20 µJ
		Additional three-level dc/dc		
T_H, T_L	2 × C3M0065090D	75 mΩ	226 µJ	36 µJ
D_H, D_L	2 × C5D500650D	16 mΩ	-	11 µJ

Table 4. Estimated power losses in semiconductor devices (6 kW, 50 kHz)

Elements	Switching losses [W]	On-state losses [W]	Total (1 device) [W]	Total [W]
		T-type inverter		
T_{1n}, T_{4n}	1.6	4.53	6.13	36.78
T_{2n}, T_{3n}	2.34	1.05	3.39	20.34
		Standard dc/dc boost		
T_L	33.26	19.85	53.11	53.11
D_H	17.67	17.68	35.35	35.35
		Additional three-level dc/dc		
T_H, T_L	13.6	14.41	28.01	56.02
D_H, D_L	5.1	11.11	16.21	32.42

losses will be decreased. It is also worth noting that the additional dc/dc converter, with higher number of devices than the standard boost converter (six vs. two), shows nearly identical power losses in semiconductors.

6. Experiments

On the basis of the simulation results, a laboratory prototype of the 6 kVA inverter was designed and built with the parameters presented in Tables 2 and 3 using SiC power devices (Fig. 8). In addition to the T-type bridge, the dc/dc converter was added on the same heatsink. The system was controlled via fibre optics in open loop from dSpace DS1006 at a sampling frequency of 50 kHz. During the presented tests, the inverter was supplied from the DC supply and loaded with a resistive load. Due to the limited current of the available supply, the power was limited to 4 kVA at 250 V DC. Then, the input voltage was increased to 330 V at 6 kVA. Scope records presented in Fig. 9 confirm the correct operation of the laboratory model: quality of the input and output waveforms is acceptable, while the neutral point potential is correctly controlled. Due to the influence of sampling and the applied filters on the voltage measurements, changes of the capacitors' voltages are more significant than in simulations but both voltages are kept below 350 V. Efficiency of the eT inverter was also measured with Yokogawa WT1800 (Fig. 10). The obtained results, namely, 96.16% at 4 kVA and 95.8% at 6 kVA, confirms the estimations of the power losses presented in Section 5, as additional losses occur in the passive components.

7. Summary

After a series of simulations and experiments presented in this paper, the eT inverter may be recognised as a very promising topology capable of connecting low-voltage sources to three-phase grids or loads. The additional dc/dc

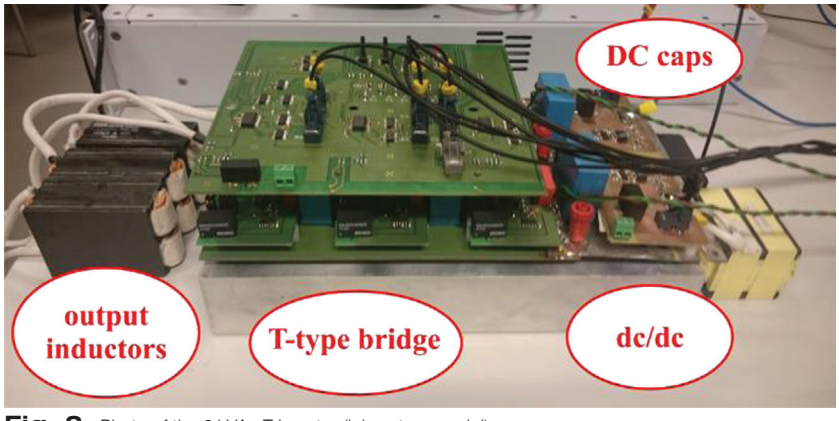


Fig. 8. Photo of the 6 kVA eT inverter (laboratory model).

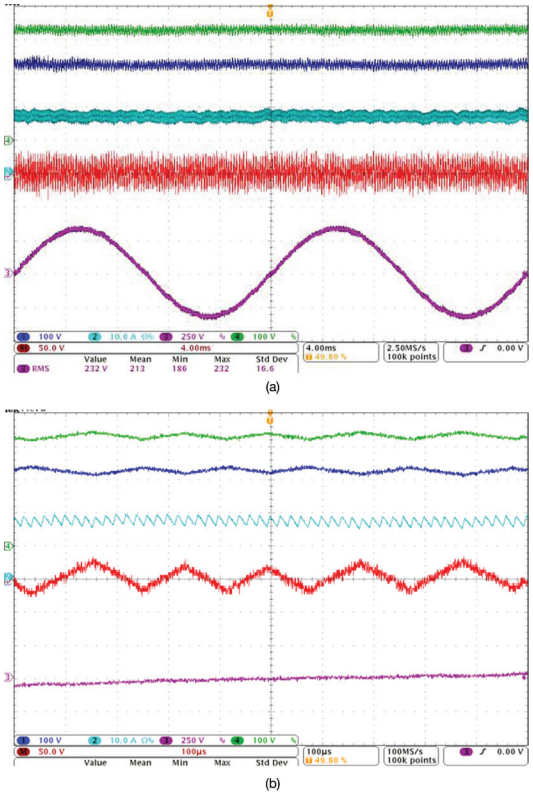


Fig. 9. Specific waveforms observed during experiments at nominal conditions (6 kVA), from the top: voltages across the capacitors C_H and C_L, input current, difference between capacitor voltages and output voltage (phase A).

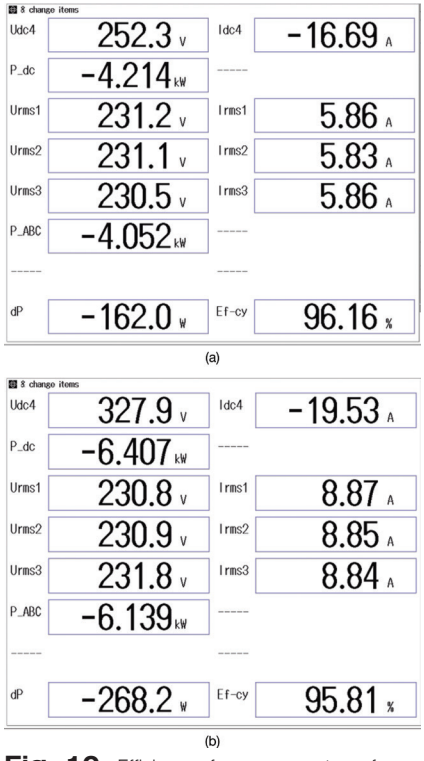


Fig. 10. Efficiency of measurements performed at 4 kVA and $U = 250$ V (a) and 6 kVA and $U = 330$ V (b).

converter, besides boost operation, ensures the neutral point voltage balancing, and DC-link capacitors may be seriously reduced (only $2 \times 30\ \mu F$ for a 6 kVA model). Moreover, the input inductor is also 2.5 times lighter than in the comparable dc/dc boost converter. At the same time, the performed simulations, estimations and measurements prove that the herein-discussed 6 kVA eT inverter with state-of-the art SiC MOSFETs shows around 96% efficiency, while around 2.5% power losses occur in semiconductor devices. This result is similar to that obtained for the reference system, namely, the three-phase T-type inverter with the standard boost converter. Therefore, the eT inverter shows lower number of passive components, with comparable quality of the input and output waveforms as well as comparable efficiency.

References

Abu-Rub, H., Malinowski, M. and Al-Haddad, H. (2014). *Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications*. Hoboken, NJ: Wiley.

Anthon, A., Zhang, Z., Andersen, M., Holmes, G., McGrath, B. and Teixeira, C. A. (2016a). Comparative Evaluation of the Loss and Thermal Performance of Advanced Three-Level Inverter Topologies. *IEEE Transactions on Industry Applications*, 53(2), pp. 1381–1389.

Anthon, A., Zhang, Z., Andersen, M., Holmes, G., McGrath, B. and Teixeira, C. A. (2016b). The Benefits of SiC mMosfets in a T-Type Inverter for Grid-Tie Applications. *IEEE Transactions on Power Electronics*, 32(4), pp. 2808–2821.

Furusho, Y. and Fuji, K. (2016). 1-MW solar power conditioning system with boost converter using all-SiC power module. In: *Proceedings of 9th International Conference on Integrated Power Electronics Systems CIPS 2016*, Nuremberg, Germany: VDE, pp. 1–5.

Grbovic, P., Delaure, P., Le Moigne, P. and Bartholomeus, P. (2012). A Three-Terminal Ultracapacitor-Based Energy Storage and PFC Device for Regenerative Controlled Electric Drives. *IEEE Transactions on Industrial Electronics*, 59(1), pp. 301–316.

Gu, M., Xu, P., Zhang, L. and Sun, K (2015). A SiC-based T-type three-phase three-level grid tied inverter. In: *Proceedings of 10th Conference on Industrial Electronics and Applications (ICIEA)*, Auckland: IEEE, pp. 1116–1121.

Gurpinar, E. and Castelazzi, A. (2015). Single-Phase T-Type Inverter Performance Benchmark Using Si IGBTs, SiC MOSFETs and GaN HEMTs. *IEEE Transactions on Power Electronics*, 31(10), pp. 7148–7160.

Rąbkowski, J., Barlik, R., Matulka, J. and Nowak, M. (2002). An extended structure of NPC three level converter as a universal power compensator. In: *Proceedings of the EPE-PEMEC Conference*, Dubrovnik-Cavtat: PEMC, pp. 1–8.

Rąbkowski, J., Sak, T., Strzelecki, R. and Grabarek, M. (2017). SiC-based T-type modules for multi-pulse inverter with coupled inductors. In: *Proceedings of 11th IEEE International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, Cadiz: IEEE, pp. 568–572.

Schweizer, M. and Kolar, J. W. (2013). Design and Implementation of a Hybrid Efficient Three-Level T-Type Converter for Low-Voltage Applications. *IEEE Transactions on Power Electronics*, 28(2), pp. 899–907.

Shi, Y., Shi, Y., Wang, L., Xie, R. and Li., H. (2016). A 50kW high power density paralleled-five-level PV converter based on SiC T-type MOSFET modules. In: *Proceedings of Energy Conversion Congress and Exposition (ECCE)*, Milwaukee: IEEE, pp. 1–8.

Shi, Y., Xie, R., Wang, L., Shi, Y. and Li., H. (2017). Switching Characterization and Short-Circuit Protection of 1200 V SiC MOSFET T-Type Module in PV Inverter Application. *IEEE Transactions on Industrial Electronics*, 64(11), pp. 9135–9143.

Uemura, H., Krismer, F. and Kolar, J. W. (2013). Comparative evaluation of T-type topologies comprising standard and reverse-blocking IGBTs. In: *Proceedings of 39th IECON 2013 Conference*, 10–14 November 2013, Vienna: Austria Center Vienna, pp. 1288–1295.