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On analog comparators for CMOS digital pixel applications. A comparative study

W. JENDERNALIK*

Faculty of Electronics Telecommunications and Informatics,
Gdańsk University of Technology, 11/12 Narutowicza St., 80-952 Gdańsk, Poland

Abstract. Voltage comparator is the only – apart from the light-to-voltage converter – analog component in the digital CMOS pixel. In this work, the influence of the analog comparator nonidealities on the performance of the digital pixel has been investigated. In particular, two versions of the digital pixel have been designed in 0.35 μm CMOS technology, each using a different type of analog comparator. The properties of both versions have been compared. The first pixel utilizes a differential comparator with the increased size and improved electrical performance. The second structure is based on a very simple non-differential comparator with a reduced size and degraded performance. Theoretical analysis of the comparator nonideality effect on the quality of the image obtained from the digital pixel matrix as well as simulation results are provided.

Key words: CMOS image sensor, CMOS digital pixel, analog comparator, fixed pattern noise (FPN).

1. Introduction

A conventional integrated CMOS image sensor contains a matrix of analog pixels and a set of analog-to-digital (A/D) converters that transform – in real time – the analog signal from the pixels into a digital form [1, 2]. Signal from the pixels is relatively weak and it is easily affected by all kinds of interference and noise [3, 4]. Therefore, there is a tendency to convert it into a digital form as early as possible, before further processing and taking it out of the integrated circuit [5]. Early realizations of the CMOS image sensors contained only one A/D converter that transformed the signal from all the pixels. A drawback of such a solution was the necessity of applying a fast A/D converter (over 10 Msamples/s), which resulted in a significant power consumption. Nowadays, in the most commonly used solution, one A/D converter is used for each pixel column. This reduces the propagation time of the signal between the pixel and the A/D converter and, consequently, improves immunity of the system to the interference. Furthermore, using a larger number of A/D converters allows for reducing their speeds and thus the power consumption.

Research on moving the analog-to-digital conversion into the inside of the pixel has been going on for a number of years [6]. Such a solution has two major advantages. The first one is the possibility of using very slow A/D converters (a few ksamples/s). The second advantage is a considerable reduction of the propagation path of the analog signal from the optical sensor to the A/D converter, leading to the improvement of the signal to noise ratio. On the other hand, the fundamental drawback of such a digital pixel is its relatively large area compared to the analog pixel. The size of a conventional analog pixel is no more than a few by a few micrometers. The sizes of the digital pixels containing a photosensor and a complete A/D converter are larger than 20 μm × 20 μm. This results in degradation of the fill factor, increase of the matrix area, and the increase of the integrated image sensor price. For this reason, development of A/D converter solutions that can be implemented on a small pixel while maintaining sufficiently large bit resolution and high conversion quality becomes of primary importance. One of the most important components of the A/D converter is a CMOS analog voltage comparator. Such a comparator usually consists of a conventional MOS differential pair with a current mirror as an active load, an amplifier stage implemented as a common-source configuration, as well as one or two CMOS inverters which work as an additional amplification stage. The comparator footprint may contribute to as much as 20 to 30 percent of the entire pixel area [7]. In order to reduce the comparator size, one needs to reduce the sizes of its transistors, which leads to degrading the electrical performance of the circuit. Smaller transistor size means larger technological spread of their parameters and the increased offset voltage of the comparator. Moreover, the $1/f$ noise level is also increased.

In this work, we investigate a possibility of applying – in a digital pixel – a simple non-differential analog comparator consisting of four CMOS transistors. Such a comparator is characterized by worse electrical performance compared to a conventional differential comparator; however, it features a considerably smaller footprint. In order to compare the influence of the analog comparator performance on the image quality, two versions of a digital pixel realized in 0.35 μm CMOS technology have been designed. The pixels are only different with respect to the analog comparator. Simulation studies have been performed for the two matrices of the size of 22 × 22 pixels.

The paper is organized as follows. In Section 2, construction and the operation principle of a digital pixel has been briefly recalled. In Section 3, performance parameters of the analog comparators from the point of view of their application in dig-

*e-mail: waldi@ue.eti.pg.gda.pl

ital pixels have been discussed. Sections 4 and 5 contain the theoretical analysis and the simulation results concerning the effect of comparator and photosensors mismatch on the fixed pattern noise (FPN) in the image acquired from the digital pixel matrix. The paper is concluded in Section 6.

2. Digital pixel with analog comparator. Construction and operation principles

2.1 Principle of operation. A number of digital pixel solutions can be found in the literature [7–12]. The major differences between various implementations are in the type of the photosensor, the way of analog to digital conversion applied, the type of the digital memory, the type of the digital code, the type of the pixel reset, etc. Digital pixel can be categorized into two main classes: pixels containing a complete A/D converter and those in which only the initial stages of the analog-to-digital conversion are realized [5, 13]. Regardless of the approach, the pixels always contain an analog comparator which compares the signal from the photosensor to a specified reference voltage. An example realization of the digital pixel which permits easy explanation of its operation principle is shown in Fig. 1. The pixel contains a photosensor in a form of a photodiode and a complete single-slope A/D converter with a digital memory in form of a ripple-counter. In this circuit, the analog comparator compares the photodiode voltage V_D with a reference voltage V_{ref} and determines the time of stopping the digital counter. The output stage of the comparator is kept in the latch circuit, which allows for powering down the comparator in order to reduce its power consumption.

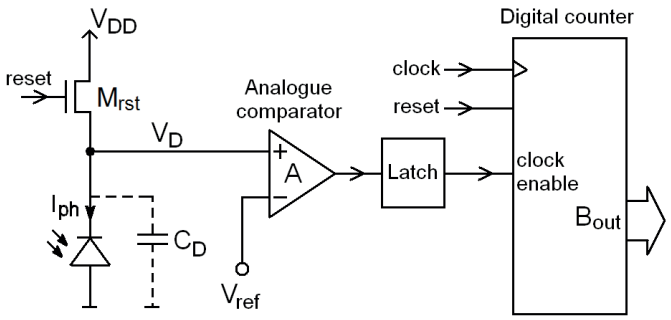

Fig. 1. Diagram of an example CMOS digital pixel

The typical electrical waveforms in the pixel are shown in Fig. 2. The detailed circuit operation is as follows. First, a high state is applied at the reset input. The counter is set into the initial state $B_{out} = 0_{10}$. The n-channel transistor M_{rst} is turned on and the parasitic capacitance C_D at the cathode terminal of the photodiode is charged to the initial voltage V_{D0}.

The value of V_{D0} depends on several factors, in particular on the amplitude and the time length of the reset impulse, the parameters of M_{rst}, as well as the reverse current of the photodiode. It can be estimated as

$$V_{D0} = V_{rst} - V_{GSrst} \approx V_{rst} - V_{THrst}, \tag{1}$$

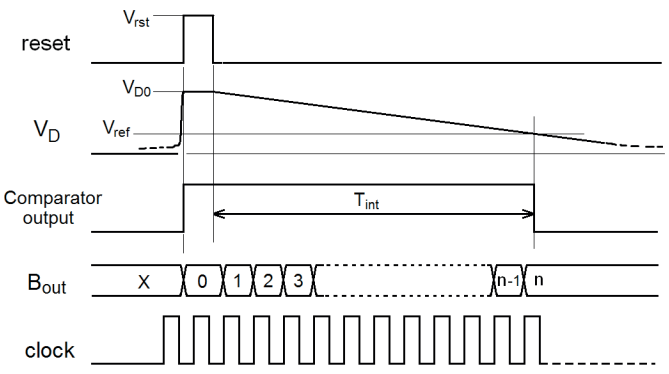

Fig. 2. Signal waveforms in the example pixel from Fig. 1

where V_{rst} is the amplitude of the reset signal, V_{GSrst} i V_{THrst} are the gate-to-source and the threshold voltages of the transistor M_{rst}, respectively.

The voltage V_{D0} is higher than V_{ref} and the comparator output switches into a high state. After changing the reset signal into a low state, the digital counter starts working. The counter counts the clock impulses. During that period, the transistor M_{rst} is cut off and the capacitance C_D is being discharged by the photocurrent I_{ph}. The voltage V_D decreases linearly according to the formula

$$\frac{\Delta V_D}{\Delta t} = \frac{I_{ph}}{C_D}. \tag{2}$$

The A/D conversion process ends when V_D reaches V_{ref}. The, the comparator output switches to the low state and the counter stops. The working time of the counter is denoted in Fig. 2 as T_{int}. Assuming ideal comparator, T_{int} can be calculated using (2) as

$$T_{\text{int}} = \left(V_{D0} - V_{ref}\right) \cdot \frac{C_D}{I_{ph}}. \tag{3}$$

During the period of the length T_{int} the counter counts n clock impulses of the period $T_{clk} = 1/f_{clk}$ so that T_{int} can be expressed as

$$T_{\text{int}} = n \cdot T_{clk} = n / f_{clk}. \tag{4}$$

The photocurrent I_{ph} has two components: a so-called dark current I_{dark} and the photon-generated current I_{light} which is linearly dependent on the photon flux Φ_{light}

$$I_{ph} = I_{dark} + I_{light} = I_{dark} + s \cdot \Phi_{light}, \tag{5}$$

where s denotes photodiode sensitivity.

Using (1–5) one can calculate the number of impulses n corresponding to the light signal

$$n = \left(V_{rst} - V_{THrst} - V_{ref}\right) \cdot C_D \cdot f_{clk} \cdot \frac{1}{I_{dark} + s \cdot \Phi_{light}}. \tag{6}$$

The value of n is output in a binary form into the bus B_{out}.

2.2 Comparator requirements. The analog comparator has to exhibit sufficiently large gain A and a small input-referred offset voltage V_{OS}, determined by the assumed bit resolution of the image sensor. Based on the waveforms in Fig. 2, it can be concluded that the smallest voltage that the comparator has to be able to distinguish is

$$V_{LSB} = \frac{V_{D0} - V_{ref}}{n_{\max}} = \frac{V_{D0} - V_{ref}}{2^N}, \tag{7}$$

where N is the bit resolution of the pixel, i.e., the number of bits of the digital counter. It should be noted that if the output voltage of the comparator can change from 0 to V_{DD}, then the comparator is able to detect the changes in the input voltage of the value

$$V_{in,\min} = V_D \ / A. \tag{8}$$

Considering just a single pixel, a condition $V_{in,\min} < V_{LSB}$ is sufficient for errorless A/D conversion. However, the image sensor consists of many pixels. In this case the offset voltages V_{OS} of the comparators have to be taken into account, being of random nature. V_{OS} does not influence the bit resolution and linearity of a single A/D converter; it only affects the offset error and the gain error of the converter. However, these errors are random and therefore result in fixed pattern noise in the image from the pixel matrix. Consequently, too high V_{OS} may lead to reduction of the bit resolution of the matrix despite the fact that it does not affect the resolution of individual pixels. For example, in a uniformly illuminated matrix, if the differences in the pixel output due to FPN will be larger than ±1 LSB, the effective matrix resolution will be smaller by 1 bit compared to the pixel resolution.

Thus, in order to achieve a required bit resolution of the pixel matrix, the comparator parameters have to satisfy the condition

$$V_{in,\min} + 2|V_{OS}| < V_{LSB}. \tag{9}$$

Using (1), (7) and (8), the condition (9) can be expressed as

$$\frac{V_{DD}}{A} + 2|V_{OS}| < \frac{V_{rst} - V_{THrst} - V_{ref}}{2^N}. \tag{10}$$

In order to estimate the minimum requirements on the comparator performance, typical parameters of the standard 0.35 μm CMOS technology have been assumed, i.e., $V_{DD} = V_{rst} = 3.3$ V, $V_{THrst} = 0.8$ V, $V_{ref} = 0.5$ V. In case of a resolution $N = 8$, the voltage $V_{LSB} = 7.8$ mV, so that, assuming the comparator gain $A > 5000$ V/V, the offset voltage has to satisfy $V_{OS} < 4$ mV. Gain at the level of a few thousand V/V can be easily achieved even in a small-area comparator. However, ensuring that the offset voltage is smaller than 5 mV requires considerable increase of the circuit area.

3. Analog comparators

Input-referred offset voltage is one of the most important parameters of the analog comparator influencing the quality of the image obtained from the pixel matrix. In order to investigate the effect of the offset voltage on the image quality, two versions of the digital pixel have been designed, different with respect to the comparator circuit applied therein. The first version utilizes a rather involved structure characterized by a relatively large area but small offset voltage. The second version is based on a simple comparator of a reduced footprint but a larger offset voltage.

3.1 Comparator I (complex structure). Schematic diagram of the comparator is shown in Fig. 3. This circuit is a modified version of the comparator presented in [14]. The input stage is a conventional NMOS differential pair (M1–M2) loaded by a PMOS current mirror (M3–M4). The circuit contains an additional amplifying stage (M5–M6), a latch (M7–M12) as well as a power-down circuit (M13–M14). The circuit of Fig. 3 exhibits characteristics that are advantageous from the point of view of digital pixel application: (i) easy adjustment of a threshold voltage in the range of about 2.5 V; (ii) reduced influence of the supply voltage and temperature on the threshold voltage of the comparator; (iii) low sensitivity of the circuit on interference from strong digital signals; (iv) lack of the bias current I_{BIAS} changes on the threshold voltage of the comparator (I_{BIAS} only affects the gain and the bandwidth), due to which possible mismatch of M_{BIAS} does not lead to increasing V_{OS}; (v) independence of V_{OS} of relative physical location of the comparators in the pixel matrix (i.e., their distance and orientation). The last feature is a consequence of the fact that V_{OS} is mostly dependent on transistor matching in the particular pairs, M1–M2 and M3–M4. On the other hand, the transistors in these pairs can be allocated close to each other so that their good matching is possible.

An approximate formula for the offset voltage of a multistage comparator of Fig. 3 can be derived having in mind that V_{OS} is mostly determined by the first stage. The mismatch in the transistor pairs M1–M2 and M3–M4 is a result of the threshold voltage mismatch, the gain factor mismatch, and the body factor mismatch. Among the aforementioned factors, the major contributor is the threshold voltage mismatch [15], which can be characterized using a standard deviation s according to the Pelgrom formula [16]

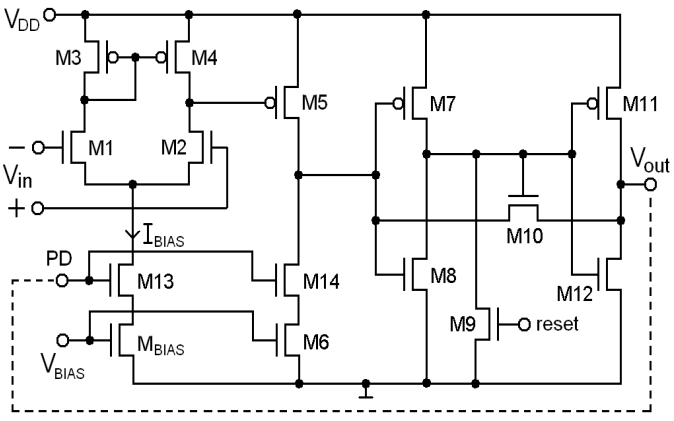

Fig. 3. Comparator I (complex structure)

$$\sigma\left(V_{TH1}-V_{TH2}\right)=\sigma\left(\Delta V_{TH}\right)=\frac{A_{VT}}{\sqrt{WL}}, \quad (11)$$

where V_{TH1}–V_{TH2} represents the difference of the threshold voltages between two identically designed transistors located close to each other, W and L are the transistor channel width and length, whereas A_{VT} is a technology-dependent parameter.

Assuming that ΔV_{TH} is a small-signal variation and using the results of [15] and [17], the input-referred offset voltage of the comparator in Fig. 3 can be expressed as

$$\sigma\left(V_{OS}\right)=\sqrt{\sigma^2\left(V_{TH1}-V_{TH2}\right)+\left(\frac{g_{m3,4}}{g_{m1,2}}\right)^2\sigma^2\left(V_{TH3}-V_{TH4}\right)}, \quad (12a)$$

where $g_{m1,2} = g_{m1} = g_{m2}$ and $g_{m3,4} = g_{m3} = g_{m4}$ are the small-signal transconductances of the transistors M1–M2 and M3–M4, respectively.

As (11) and (12a) show, the reduction of V_{OS} requires application of M1–M4 with an area ($W{\cdot}L$) as large as possible, and additionally keep the ratio of transconductances ($g_{m3,4}/g_{m1,2}$) of the current mirror and the differential pair as small as possible. The changes of the transconductance ratio for different operation regions can be estimated as

$$\frac{g_{m3,4}}{g_{m1,2}}=\begin{cases}\left(\dfrac{K_P\left(W/L\right)_{3,4}}{K_{PN}\left(W/L\right)_{1,2}}\right)^{1/2} & \text{for strong inversion}\\ \approx 1 & \text{for weak inversion}\end{cases}, \quad (12b)$$

where K_{PN} and K_{PP} are the transconductance parameters of the NMOS and PMOS transistors, respectively.

In order to estimate the offset voltage of the considered comparator, calculations have been carried out for the 0.35 µm CMOS AMS (Austria microsystems) technology characterized by K_{PN} = 170 µA/V^2, K_{PP} = 58 µA/V^2, A_{VTN} = 9.5 mVµm, A_{VTP} = 14.5 mVµm. A_{VTN} and A_{VTP} are the mismatch parameters of the NMOS and PMOS transistors, respectively. The following transistor sizes were assumed: $(W/L)_{1,2}$ = 17µm/0.7µm, $(W/L)_{3,4}$ = 14µm/0.7µm. According to (12), the V_{OS} is from 3.7 mV to 5.4 mV, depending on the transistors operation region.

3.2 Comparator II (simple structure). Simplified version of the comparator (cf. Fig. 4) contains two inverters biased by a constant current I_{BIAS}. The advantages of this structure are small size and large gain which is comparable to the gain of the circuit in Fig. 3 for the same I_{BIAS}. Nevertheless, there are limitations: (i) narrow range of threshold voltage adjustment (about 0.2 V), (ii) dependence of the threshold voltage on the transistor sizes, supply voltage variations, bias current variations, as well as the temperature, (iii) sensitivity to the interference signals in the power supply bus and the ground (due to the lack of symmetry), (iv) relatively large V_{OS}, (v) supply current equal to I_{BIAS} in the idle state.

The threshold voltage of the comparator of Fig. 4 is understood as an input voltage $V_{in} = V_{in,th}$ for which the output voltage equals half of the supply voltage, i.e., $V_{out} = V_{DD}/2$. Neglecting the second-order effects in MOS transistors, the comparator threshold voltage can be determined as a gate-source voltage of M1 at which the drain currents of transistors M1 and M3 becomes equal to each other.

$$V_{in,th}=V_{in}\big|_{V_{out}=V_{DD}/2}\cong V_{GS1}\big|_{I_{D1}=I_{D3}} \quad (13)$$

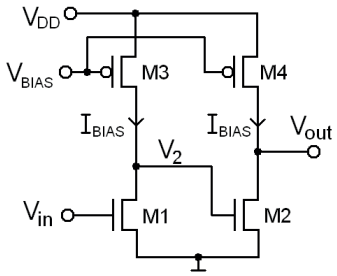

Fig. 4. Comparator II (simple structure)

$V_{in,th}$ voltage can be adjusted by changing the drain current of M3. 100–300 mV change of $V_{in,th}$ can be achieved by changing I_{BIAS} one order of magnitude. The adjustment range of $V_{in,th}$ is limited on one side by speed, and on the other side by power consumption of the comparator. To achieve $V_{in,th}$ much lower than the M1 threshold voltage it is required very small I_{BIAS} which may not allow to obtain the desired speed of ADC. On the other hand, for higher I_{BIAS} and $V_{in,th}$, the total power consumption of the pixel matrix may not be acceptable.

Mismatch of the voltage $V_{in,th}$ is mostly caused by the transistor mismatch in the first stage (M1, M3). Deviations of the threshold voltages ΔV_{TH1} and ΔV_{TH3} cause statistically independent deviations of the drain currents of M1 and M3

$$I_{D1}=I_{BIAS}\pm g_{m1}\left(\Delta V_{TH1}\right), \quad I_{D3}=I_{BIAS}\pm g_{m3}\left(\Delta V_{TH3}\right). \quad (14)$$

As a result, both drain currents are not equal, $I_{D1} \neq I_{D3}$, and the actual value of $V_{in,th}$ is deviated from its original value given by (13). The difference between currents I_{D1} and I_{D3}, referred to the input, gives the deviation of $V_{in,th}$

$$\Delta V_{in,th}=\frac{I_{D1}-I_{D3}}{g_{m1}}=\pm\left(\Delta V_{TH1}\right)\mp\frac{g_{m3}}{g_{m1}}\left(\Delta V_{TH3}\right). \quad (15a)$$

Using (11) and assuming that ΔV_{TH3} are ΔV_{TH1} statistically independent, the input-referred offset voltage can be found as

$$\sigma\left(V_{OS}\right)=\sigma\left(\Delta V_{in,th}\right)=\sqrt{\frac{1}{2}\sigma^2\left(\Delta V_{TH1}\right)+\left(\frac{g_{m3}}{g_{m1}}\right)^2\frac{1}{2}\sigma^2\left(\Delta V_{TH3}\right)}, \quad (15b)$$

where the transconductance ratio g_{m3}/g_{m1} can be calculated by using a formula analogous to (12b). For the transistor sizes of $W = L$ = 1 µm, the offset voltage of the comparator in Fig. 4 is V_{OS} = 9 mV when M1 and M3 work in strong-inversion, and increases to 12.5 mV for weak-inversion region.

3.3 Simulation results. The important parameters of the comparators are gathered in Table 1. For both comparators the input offset voltage is dependent on biasing current, because it

is assumed 0.2 µA to 4 µA current change, the region of transistors operation changes from weak- to moderate-inversion for Comparator I, and from moderate- to strong-inversion for Comparator II. Typical offset voltage values obtained from 500 runs of Monte Carlo analysis are ~3.5 mV and ~10 mV for the Comparator I and II, respectively. Given the values of V_{OS}, an achievable resolution of the pixel matrix is no more than 8 and 7 for the matrices using Comparator I and II, respectively. In this case, the levels of gain (>10^4 V/V) and the 1/*f* noise (<50 μV_{rms}) obtained for both comparators will not be limiting the matrix performance. The total power consumption of the comparator I is about two times greater than that of comparator II under the same biasing current. It is due to greater dynamic power in comparator I, which can be clearly seen when the switching frequency is increased.

Table 1
The simulated parameters of the comparators

	Comparator I (Fig. 3)	Comparator II (Fig. 4)
Technology	CMOS 0.35 µm 4M2P 3.3V AMS	
Threshold voltage	0.6 V– (V_{DD}–0.2 V) independent of I_{BIAS}	0.55–0.75 V at I_{BIAS} = 0.2–4µA
Input offset σ(V_{OS}) without common-centroid	4.9 mV at I_{BIAS}=0.2 µA 4.65 mV at I_{BIAS}=4 µA	11 mV at I_{BIAS}=0.2 µA 9.85 mV at I_{BIAS}=4 µA
Input offset σ(V_{OS}) with common-centroid	3.5 mV at I_{BIAS}=0.2 µA 3.3 mV at I_{BIAS} = 4 µA	not applicable
Input noise, integrated within 1 Hz–100 kHz	23 µVrms	31 µVrms
Total power consumption at 1 MHz, V_{DD}=3.3 V	7–22 µW at I_{BIAS} = 0.2–4µA	0.8–14 µW at I_{BIAS} = 0.2–4 µA
Total power consumption at 100 kHz, V_{DD}=3.3 V	1.9–20 µW at I_{BIAS} = 0.2–4 µA	0.7–14 µW at I_{BIAS} = 0.2–4 µA
Gain	> 10000 V/V	> 10000 V/V
Layout dimensions	38 µm × 13 µm	9.5 µm × 8.5 µm

4. The impact of mismatch on image non-uniformity

One of the major factors leading to degradation of the image from the CMOS sensor is the mismatch of pixel components. Due to the mismatch, various pixels generate electric signals of different values given uniform illumination of the matrix. The mismatch affects not only the comparator but also other analog components, i.e., a photodiode and the resetting transistor (M_{rst}). The parameters that can deviate in the photodiode are its capacitance C_D, dark current I_{dark} and sensitivity *s* [18, 19]. The mismatch of the threshold voltage of M_{rst} leads to different values of the initial voltage V_{D0} on each photodiode in the matrix.

Considering (6) with the additional components related to the mismatches, the formula for the digital signal value of the pixel takes the form

$$n \pm \Delta n = \left(V_{rst} - V_{THrst} \pm \Delta V_{THrst} - V_{ref} \pm V_{OS}\right) \cdot f_{clk} \cdot \frac{C_D \pm \Delta C_D}{I_{dark} \pm \Delta I_{dark} + (s \pm \Delta s)\Phi_{light}} \quad (16)$$

where ΔV_{THrst}, ΔC_D, ΔI_{dark} and Δs are deviations of, respectively, the threshold voltage of the transistor M_{rst}, as well as the capacitance, dark current, and sensitivity of the photodiode. Figure 5 shows the influence of these deviations on the pixel characteristics. In order to improve readability of the plots, 1/*n* is plotted versus the light intensity. As indicated in Fig. 5 (a), deviation of the dark current ΔI_{dark} only results in shifting the characteristic towards the *y* axis (dark FPN). Sensitivity deviation Δs leads to changing the slope of the characteristic (gain FPN), see Fig. 5 (b). The offset voltage V_{OS} of the comparator and the deviations ΔV_{THrst} and ΔC_D have the same qualitative influence on the pixel characteristics. The deviations result in both shifting the characteristic towards the *y* axis (dark FPN) and changing its slope (gain FPN) as shown in Fig. 5 (c).

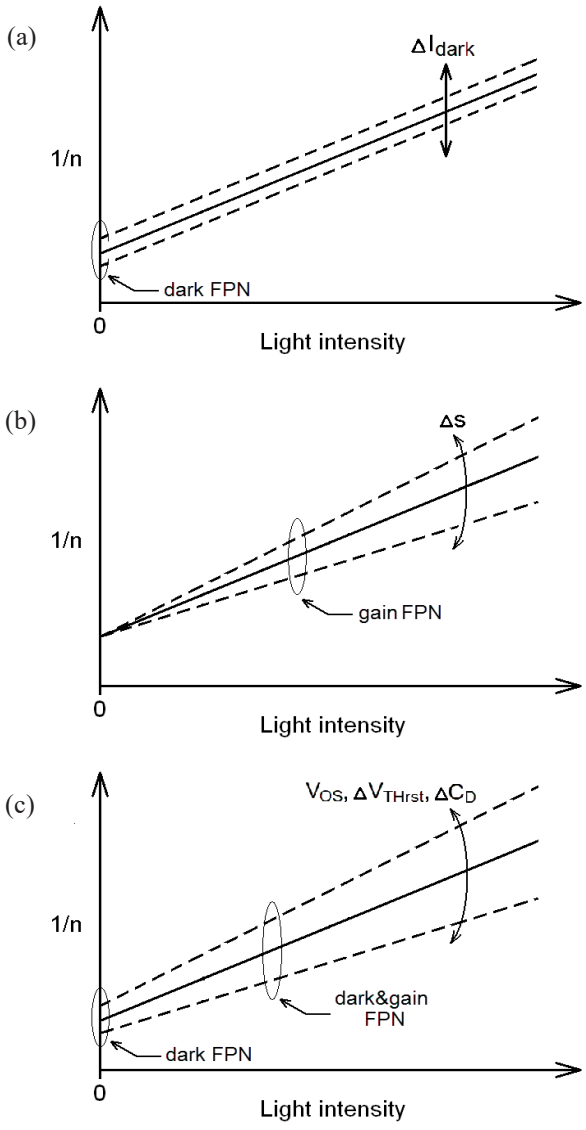

Fig. 5. Pixel characteristic and the effects of deviations: (a) ΔI_{dark} only, (b) Δs only, and (c) V_{OS}, ΔV_{THrst}, ΔC_D

Based on (16), one can estimate the quantitative influence of particular deviations on the pixel signal. Non-uniformity of the pixel matrix is most often determined for the two cases, i.e., without illumination, and for a particular light intensity. Considering only these two cases, the relative deviations of the pixel signal can be calculated from (16). Assuming no illumination ($\Phi_{light} = 0$) we get

$$\left(\frac{\Delta n}{n}\right)_{dark} = \pm\frac{V_{OS}}{V_{DR}} \pm \frac{\Delta V_{THrst}}{V_{DR}} \pm \frac{\Delta C_D}{C_D} \pm \frac{\Delta I_{dark}}{I_{dark}}, \tag{17}$$

where V_{DR} is a full range of variability of the photodiode voltage

$$V_{DR} = V_{rst} - V_{THrst} - V_{ref}. \tag{18}$$

In case of a specific light intensity for which $I_{dark} << s \cdot \Phi_{light}$, the relative deviation of the pixel signal is

$$\left(\frac{\Delta n}{n}\right)_{light} = \pm\frac{V_{OS}}{V_{DR}} \pm \frac{\Delta V_{THrst}}{V_{DR}} \pm \frac{\Delta C_D}{C_D} \pm \frac{\Delta s}{s}. \tag{19}$$

The formulas (17) and (19) indicate that the relative deviation of the pixel signal is a sum of the relative deviations of the particular pixel components. Assuming that these deviations are statistically independent, the value of FPN is

$$FPN_{dark} = \left(\frac{\sigma(\Delta n)}{n}\right)_{dark} = \sqrt{\frac{\sigma^2(V_{OS})}{V_{DR}^2} + \frac{\sigma^2(\Delta V_{THrst})}{V_{DR}^2} + \frac{\sigma^2(\Delta C_D)}{C_D^2} + \frac{\sigma^2(\Delta I_{dark})}{I_{dark}^2}} \tag{20a}$$

$$FPN_{light} = \left(\frac{\sigma(\Delta n)}{n}\right)_{light} = \sqrt{\frac{\sigma^2(V_{OS})}{V_{DR}^2} + \frac{\sigma^2(\Delta V_{THrst})}{V_{DR}^2} + \frac{\sigma^2(\Delta C_D)}{C_D^2} + \frac{\sigma^2(\Delta s)}{s^2}} \tag{20b}$$

Based on available technological data and the values of the offset voltage obtained in Section 2, one can initially estimate the influence of the comparator parameters as well as the remaining pixel components on the matrix non-uniformity. For the standard 0.35 µm CMOS technology, the following typical voltage value can be assumed: $V_{rst} = 3.3$ V, $V_{ref} = 0.5$ V, and $V_{THrst} = 0.8$ V. Consequently, $V_{DR} = 2$ V. A deviation of the threshold voltage of the transistor M_{rst} with the channel width and length of 1 µm is about $\sigma(\Delta V_{THrst}) \approx 7$ mV. Thus, the contribution of M_{rst} to the overall FPN noise is about 0.4%. A relative deviation of the capacitance C_D in a standard n+/p-substrate photodiode is no larger than 2%. The dark current I_{dark} is characterized by a relative large spread; its contribution to FPN is typically 2 to 20% [18, 20]. Based on simulation, the values of $\sigma(V_{OS})$ were found to be 3.5 mV and 10 mV, for Comparator I and II, respectively. Due to this, the contribution of the comparators to FPN is at the level of 0.2 to 0.5 percent.

The aforementioned estimations indicate that the analog components of the pixel limit the image quality at least as or more than the comparator.

5. Pixel design and simulation results

Figure 6 shows topography of the two version of the 8-bit pixel designed in 0.35 µm CMOS AMS technology. The pixel size is 61.6 µm × 61.6 µm. The size of Comparator I (complex version) is 38 µm × 13 µm (three times larger than the size of the photodiode). Comparator II (simple version) is over five times smaller than Comparator I. Even though the contribution of the Comparator I in the total area of the pixel is small (13%), the application of Comparator II enables even further reduction of a pixel area. In the presented pixel, the digital counter occupies most of the area, because triggered D-type flip-flops were used to facilitate simulations. In digital pixels optimized in terms of area, only dynamic counters and memories are used [7, 9, 12]. As a result, the contribution of the comparator in total area of the pixel becomes important.

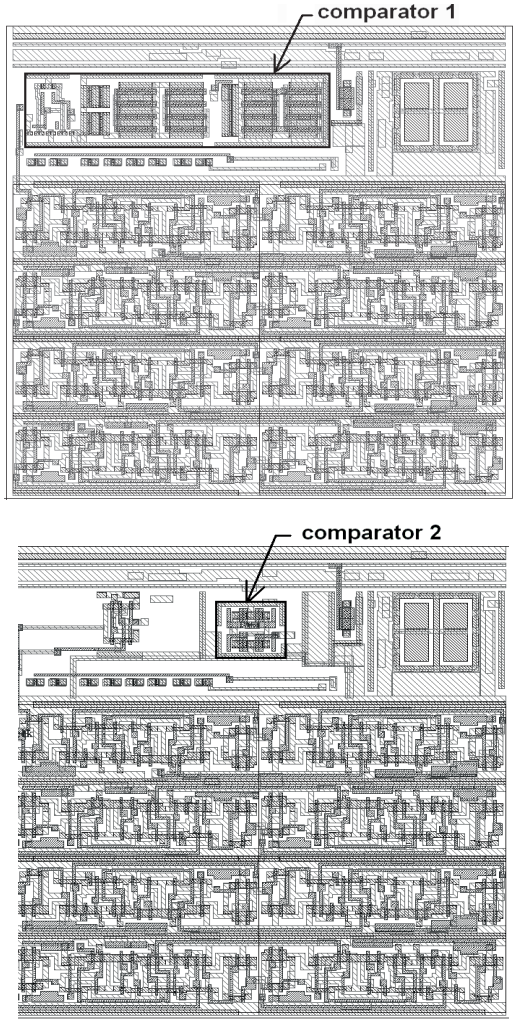

Fig. 6. Topography of the digital pixel: (a) using a complex comparator (Comparator I), and (b) using a simplified comparator (Comparator II). The pixel size if 61.6 µm × 61.6 µm

Using the pixels designed as above, the two optical matrices have been developed of the size 22 × 22 pixel each. Subsequently, 500 Monte Carlo analyses have been executed. Because of a high computational cost of the simulations, the assumed matrix dimensions constitute a trade-off between the simulation time and a random data set size. The photodiode has been modeled as a current source, taking into account the dark current and sensitivity. The photodiode model did not contain any parameters related to the random noise because of missing technological data. Even without the noise parameters, the conclusions concerning the influence of the comparator parameters on the image quality remain correct. All other passive and active components of the pixel have been described using the models provided by AMS. For simulations the supply voltage V_{DD} = 3.3 V and the current biasing comparators I_{BIAS} = 1 μA were assumed.

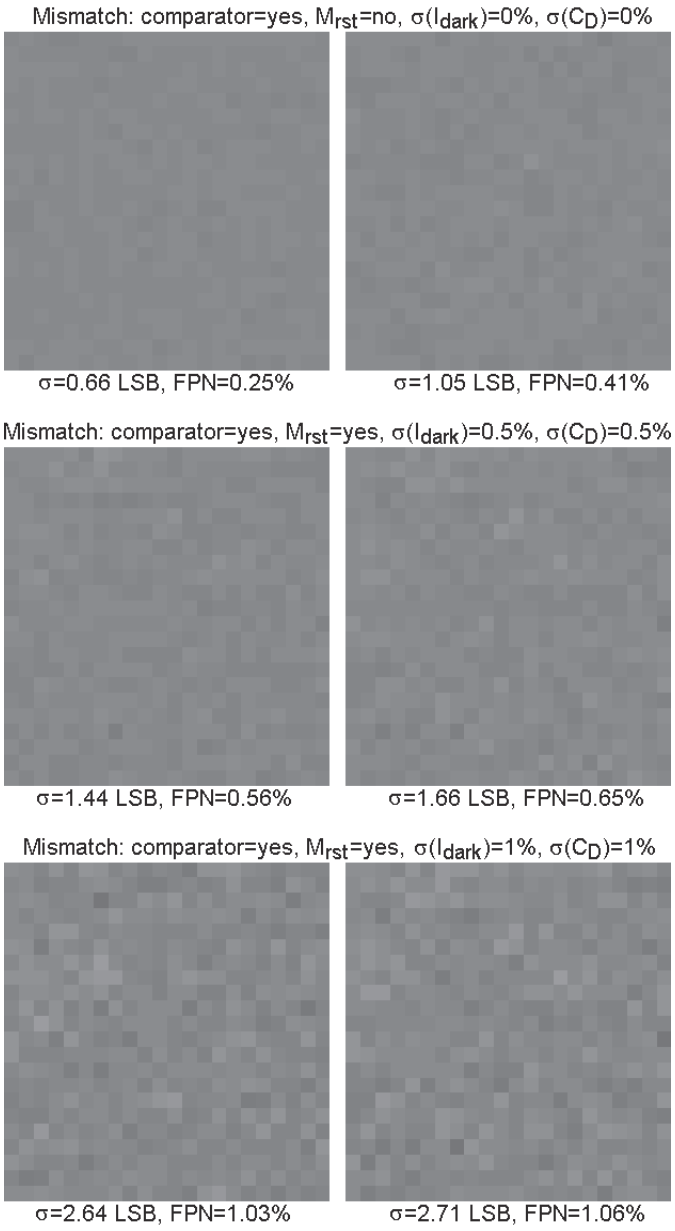

Fig. 7. Dark FPN noise in digital pixel matrices. Left column: pixels with complex comparators (Comparator I); right column: pixels with simplified comparators (Comparator II). Brightness and contrast of the images have been enhanced for the sake of better visualization

Figure 7 shows the images obtained from the two matrices without any illumination. The contrast and brightness of the images have been increased in order to visualize the FPN noise. The given values of FPN have been calculated using the commonly used definition [21]: FPN = $\sigma(\Delta n)/n_{\max} \cdot 100\%$ = $\sigma(\Delta n)/2^8 \cdot 100\%$.

Simulations have been carried out for various values of mismatch for specific pixel components. In the ideal situation, i.e., with no deviations of the dark current I_{dark}, the capacitance C_D and parameters of the transistor M_{rst}, but assuming mismatch of the comparator parameters, FPN is 0.25% and 0.41% for the matrix with Comparator I and II, respectively. This case is illustrated in the top panel of Fig. 7, where the difference in noise is clearly visible.

If the mismatch is present not only in the comparators but also in the transistor M_{rst} and when $\sigma(I_{dark}) = \sigma(C_D) = 0.5\%$, the difference in FPN for both matrices is negligible as shown in the center panel of Fig. 7. In reality, the mismatch of I_{dark} is much larger than 0.5% as already mentioned in Section 4. This is because I_{dark} is a combination of the reverse current of the photodiode and the leakage currents of the transistor M_{rst}. As a result, for very low light intensity, mismatch in analog comparators will have limited influence on the FPN noise.

Similar results are obtained for illuminated matrix. Because $I_{dark} << s \cdot \Phi_{light}$, the mismatch of the photodiode dark current does not affect FPN. Assuming $\sigma(s) > 0.5\%$, FPN is the same for both versions of the matrix (with Comparator I and Comparator II). In an integrated circuit, the mismatch of the photodiode sensitivity is a result not only of the p-n junction parameter mismatch, but also of other factors – among others, reflections in the glass layer covering the silicon structure of the diode. Consequently, the sensitivity mismatch 3s (s) can be as large as 50% and, similarly as for the dark image, the mismatch of the analog comparators will have minor influence on FPN of the illuminated matrix.

6. Conclusion

In the work, a possibility of using a simple analog comparator (consisting of just four transistors) in a digital CMOS pixel has been investigated. Compared to a differential comparator, a simplified version is significantly (by over a factor of five) smaller but exhibits three times as large offset voltage and considerably (by a factor of 5) smaller range of adjusting the turn-on threshold. Simulation studies indicate that degraded electrical performance parameters of the comparator do not significantly affect the image quality, assuming that the pixel matrix is realized in a standard CMOS technology. Application of a comparator with small-size transistor and non-optimal matching is feasible because the image quality is mostly limited by mismatch of other analog components of the pixel.

Nevertheless, the above conclusions may not hold for CMOS technologies that are modified and optimized for applications in light sensors. With these technologies, it is possible to achieve better parameters of the light-voltage converters, for example by minimizing the dark currents of the photodiodes as well as the leakage currents of the MOS transistors, leading to higher sensitivity and better matching of the light-sensitive components. In such cases, non-idealities of the analog comparator may have significant impact on the image quality, as a result the application of CDS (correlated double sampling) reducing the influence of non-idealities is necessary.

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