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FPGA EMULATOR OF SWITCHED RELUCTANCE MOTOR IN A FIL STRUCTURE

The use of FPGA platform in power section emulation of switched reluctance motor is presented in the article. Emulation of the power part gives many advantages in the means of rapid prototyping. Power section of the electric drive is expensive and thus need to be protected from damage. Evaluating of complicated control algorithms gives a risk to damage in the real system even if some simulation tests were made before. Introducing FPGA in the loop gives opportunity to minimize such a failure. FIL system would be time efficient when using new features of CAD/CAM simulation systems that are able to convert selected part of the system model to the FPGA environment. The article presents this process in the example of SRM drive. Model equation and its block structure are introduced. Then the way to the FIL implementation in details is shown with appropriate IDE configuration, block model adaptation and run example.

KEYWORDS: FPGA, FIL, rapid prototyping, modelling, SRM, HDL coder, control system, electric drive, cosimulation

1. INTRODUCTION

1.1. FIL in fault tolerant control

FPGA in the loop (FIL) is a structure, where some elements of the more complex system is emulated in the FPGA. The rest of the system can be simulated in PC software or can be handled by another hardware solution [6]. Usually, FIL is used in rapid prototyping, but reduced evaluation time amount is not the only advantage of FPGA in the loop.

On the Figure 1 there is presented a novel, global idea of fault tolerant switched reluctance motor drive evaluation process. There are three main bases of the concept which defines uniqueness of it: a methodology, where SIL (software in the loop), FIL and HIL (hardware in the loop) is used for drive testing, a new construction – where in cost-effective way power inverter redundation of selected elements is used and new control system that is based on advanced fault tolerant control in MRAS (model reference adaptive

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structure) structure. The reference model may be used in many control problems solution: object linearization, sensorless control, high dynamics, fault detection/control. FIL is an important part of that conception.
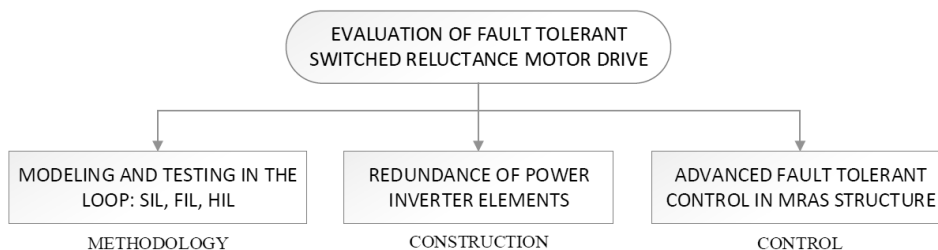

Fig. 1. Bases of switched reluctance motor drive fault tolerant novel system evaluation

1.2. FPGA in the loop system

FPGA platform can emulate any part of the drive model in general, but emulation of the power section gives many advantages in the means of rapid prototyping [6]. First of all, power part of the electric drive is very expensive - this part dominates in the all drive costs nowadays and need to be protected from damage. There is a non-negligible risk of damage of the real system when evaluates complicated control algorithms, even if some simulation tests are made before. Introducing FIL gives opportunity to minimize such a failure. This is because FPGA emulator can work either with software environment (when developing control algorithms) and with embedded controller in real time, so algorithms can be validated in a secure way before tests on real object. In the opposite to this solution (emulation of high current circuits) there may be implemented only a controller [9] or some part of it (e.g. estimator based on neural network [8]).

Proposed research methodology can be divided in four stages: PC simulation, FPGA in the loop simulation (FIL with PC software), real-time simulation with emulator and experimental run on real system. This methodology would be time efficient when using new features of CAD/CAM simulation systems that are able to convert selected part of the system model directly to the FPGA structure. Such a tools which integrate PC simulation environment with hardware platform are new in general (especially for Altera chips) – the only found publications with the SRM in scope, where the motor model is emulated in FPGA are: [5, 7] – but assumed another analytic model based on the FEA (finite elements analysis).

On the Figure 2 standard control closed loop is shown in a general way (in the field of electric drive automation). The blocks are: CON – control system, INV – power inverter, SRM – switched reluctance motor (control object). **X** is a

vector of set points (e.g. speed set point) , **S** – control signals (e.g. that control power transistors in the asymmetric bridge), **U** – excitations of motor phases, **D** – disturbances (e.g. load torque), **Y** – feedback control signals (e.g. motor phases currents, rotor speed when no sensorless control applied).
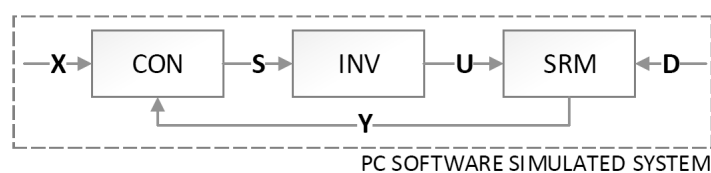

Fig. 2. Standard control loop structure in PC simulation enviroment

When starting with the system evaluation all the Figure 2 system is modelled and simulated in PC environment.

When simulation verification is positive ended, then system power section (inverter and motor) would be emulated in FPGA incorporating FIL structure. Then, the computations of system when testing is divided into two platform: PC and FPGA by dedicated (usually high-speed) interface (Figure 3).
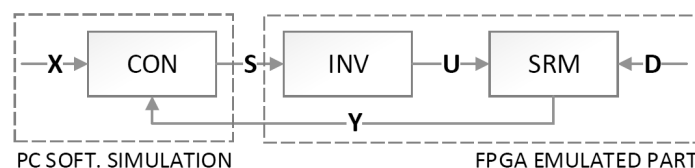

Fig. 3. FIL emulation of system power part connected with PC software simulated controller

The power of the presented solution is shown on the Figure 4 which means that there is very simple way to replace PC software with embedded controller (which is a hardware thus the system is called HIL – hardware in the loop). The system works in real time with target controller so the code bugs can be detected and fixed before test run on motor (thus minimising hard and expensive faults risk). On the Figure 5 there is presented last stage structure: embedded control system connected to the real object.
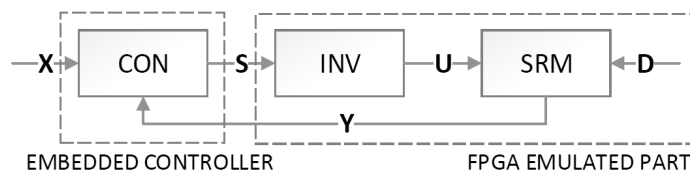

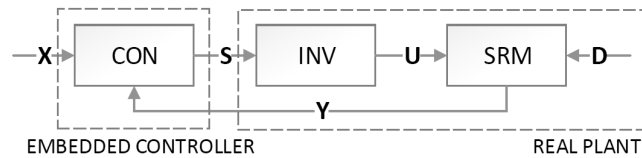Fig. 4. HIL system FPGA emulator connected with real, embedded controller

Fig. 5. Last stage structure of drive system evaluation in safe way

1.3. SR motor modelling

The motor emulation in the FIL structure bases on the mathematical equations comprising the model. That model is quite unique and dynamically developing for use in real-time computing able to auto-adaptation in reference model control structure. SR motor is nonlinear thus its modelling that complies with operating in wide speed and torque generation ranges is complicated. To make the closer view to this interesting control object, on the Figure 6 there are presented examples of motor made from different material [1]. The used model is a construction called 12/8 (12 stator poles and 8 rotor teeth). Those features are introduced in a clear way as motor cross-section on the Figure 7.
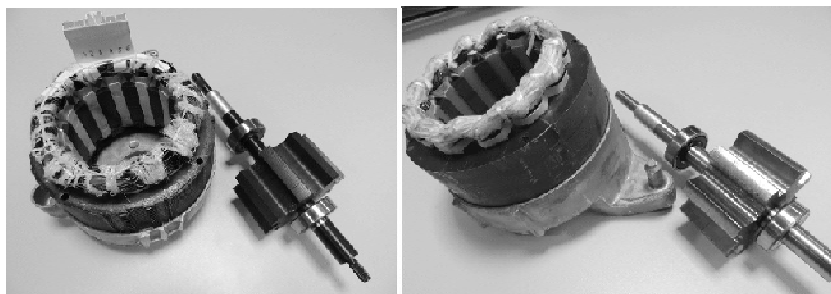

Fig. 6. Example pictures of SR motor made of stack of metal sheets (on the left)
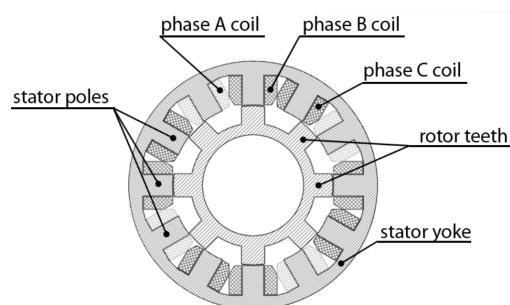and powder material (on the right)

Fig. 7. Cross-section of 12/8 SR motor construction

1.4. Motor model equations

As the presented SR model equations are explained in other referenced publications [2, 3], it will be mentioned in a very generalized way that the equations begins with the phase voltage as follows:

$$\upsilon = iR + \upsilon_F \tag{1}$$

Where phase induced voltage is:

$$\upsilon_F = \frac{d\Psi}{dt} \tag{2}$$

and in more details:

$$\upsilon_F = \frac{d\Psi(i,\theta)}{dt} = \frac{\partial\Psi(i,\theta)}{\partial i}\frac{di}{dt} + \frac{\partial\Psi(i,\theta)}{\partial\theta}\frac{d\theta}{dt} \tag{3}$$

It is assumed, that the phase magnetic flux linkage is modelled as a product of two independent functions of one variable as follows:

$$\Psi(\theta,i) = L(\theta)sat(i) \tag{4}$$

When introduced a D (derivative) operator:

$$D(F(x)) = \frac{\partial F(x)}{\partial x} \tag{5}$$

the phase voltage equation has a form of:

$$\upsilon = iR + L(\theta)D(sat(i))\frac{di}{dt} + D(L(\theta))sat(i)\omega \tag{6}$$

what gives finally the electromagnetic part of the motor equation:

$$\frac{di}{dt} = \frac{u - iR - D(L(\theta))sat(i)\omega}{L(\theta)Dsat(i))} \tag{7}$$

with the phase currents taken in the role of the state variables.

When consider the function of electromagnetic torque generation as an derive of the:

$$T_e(\theta,i) = \frac{L(\theta)}{d\theta}\int\limits_{\tau=0}^{i}(sat(\tau))d\tau \tag{8}$$

with the integrator operator S as follow:

$$S(F(x)) = \int\limits_{\tau=0}^{x}(F(\tau))d\tau \tag{9}$$

the electromagnetic torque generation is based on the equation:

$$T_e(\theta,i) = D(L(\theta))S(sat(i)) \tag{10}$$

2. FIL SYSTEM ARCHITECTURE

The Cyclone EP4CE115 - FPGA (structure of the development board used in the experiment) features 114,480 logic elements (LEs), the largest offered in the Cyclone IV E series. The board (Figure 8) is equipped with up to 3.9-Mbits of RAM and 266 multipliers. In addition, it delivers interfaces to support mainstream protocols including Gigabit Ethernet (GbE) – important from the article subject.
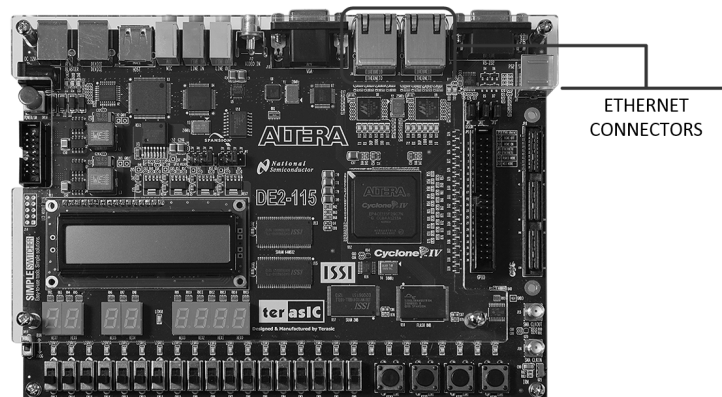
Fig. 8. FPGA test platform - terasIC Altera DE2-115 with marked ethernet connectors

Fig. 9. FIL system general structure

On the Figure 9 there is presented FPGA in the loop general structure. It bases on the two platform – PC software (Matlab/Simulink IDE) and DE2-115 FPGA evaluation platform. Systems are conntected together with gigabit ethernet.

3. FIL IMPLEMENTATION

3.1. Startup settings

To made the FIL system works, some start-up configuration need to be done. Unfortunatelly, there is very little references about FIL interfacing with Altera FPGAs in Matlab. In general dominates implementation in Xilinx chips [4, 5, 9], NI PXI platform [7] or NI CompactRIO [8].

On the Figure 10 there is shown general settings of the FPGA platform that complies with the board documentation. Proper settings determines the correct compilation of FPGA code and ethernet communication. On the Figure 11 detailed pins configuration of RGMII controller of FPGA board is presented. It is important to use proper PHY (physical) address number: 16.

Fig. 10. Matlab FIL platform general settings

Fig. 11. Detailed interface pins configuration for ethernet RGMII

To use embedded HDL tool in Matlab enviroment it is necesary to define path to the HDL compiler. It may be done by the following instruction:

```
hdlsetuptoolpath('ToolName','Altera Quartus II', 'ToolPath',
'C:\altera\13.0sp1\quartus\bin\quartus.exe');
```

where 'C:\altera\13.0sp1\quartus\bin\quartus.exe' is a path to the compiler IDE thus may vary in the specific computer.

3.2. FPGA in the Loop Model

When use embedded in Matlab environment HDL advisor there would be a lot of errors on the beginning stage of checking model compability with HDL coder. First of all, there is no possibility of use variable step simulation or continuous time domain models (elements). Simulation must be set on fixed step and all the system need to be discretized (in the scope of FIL implemented blocks).

On the Figure 12 there is presented general structure of the simulated environment ready to compile to HDL code in the range of section S3 (motor model). It not differs from the SIL (software in the loop – a version dedicated for a fully software PC simulation) besides section S2. Usually used double precision floating point variables as data containers, in SIL is not allowed by HDL coder. Thus, middleware S2 is added by grouping data converters from double to fixed point (eg. 32/16 format – 32-bits overall, 16-bits of fractional part) and back.

Fig. 12. General structure of control system model

The next restriction is that when used lookup tables it is necessary to use one dimension in the input and output each (data vectors are not allowed here). Computations of phase current based on the equation (7) and torque generation (10) require to use each kind of look-up table for each phase even if those tables for defined for each phase are the same. In FIL structure, S3 part which is SRM block (Figure 12) looks inside for each of three phase like presented on Figure 13. It may be seen, that look-up tables are separated from the signal processing block. This separation can be understood when consider standard SIL model structure of the phase current generation presented on the Figure 14 with same part in FIL (HDL generator) compatible structure on the Figure 15.
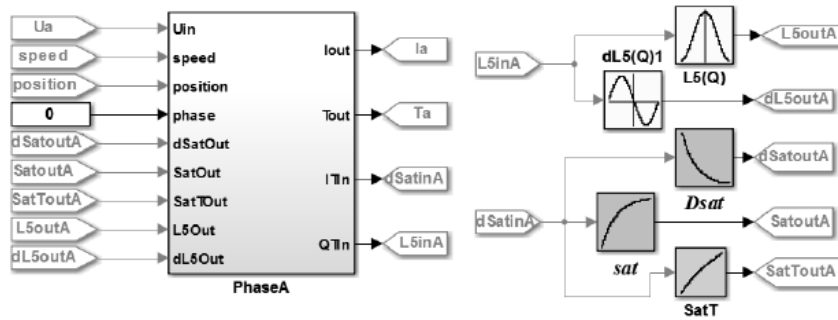
Fig. 13. SRM block inside view - one of three phases computation part
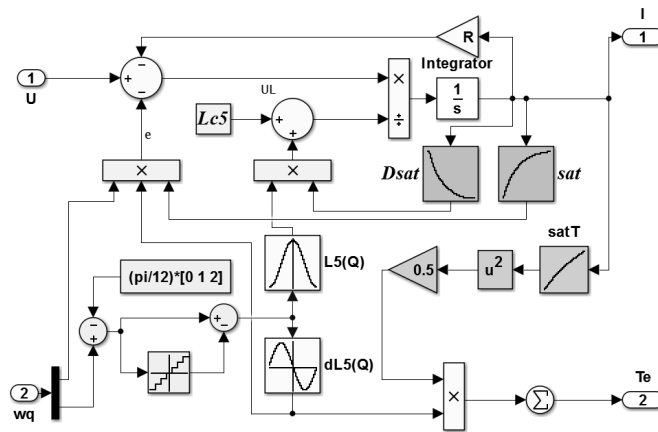

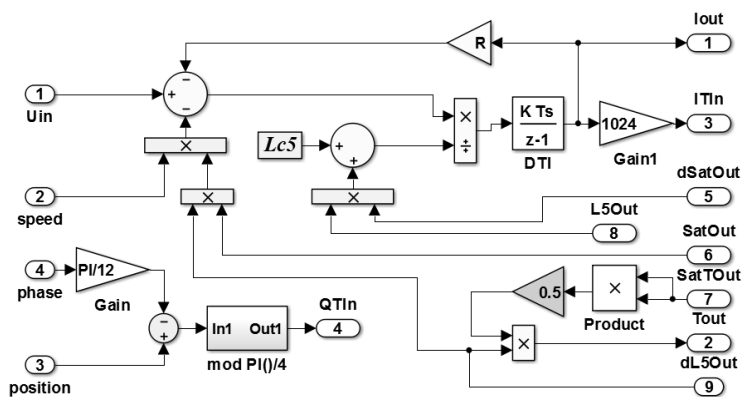Fig. 14. Electromagnetic part of the SR motor (phase current generation) in SIL structure

Fig. 15. Electromagnetic part of the SR motor (phase current generation) in FIL structure
with look-up tables moved outside the bock (higher model level)

Another restrictions are: not supported mathematical square function (easy to comply by adding product block of same two inputs signals). This is also not possible to use product block of more than two inputs. Rotor angle position quantitizer (equivalent of the incremental encoder signal or position estimation limited resolution) that can be seen on the left bottom section of Figure 14 is replaced by unique use of modulo operator.

3.3. FIL test run results

When all errors in model compatibility are corrected, the result of the Matlab HDL Advisor Workflow should appear like the structure from Figure 16. A few new elements are added that spreads signals of SRM model by SIL loop and FIL emulator, what makes possible to run parallel tests. Bigger number of inputs and outputs in *SRM_fil* block is only the reason of splitting all the grouped signals (vector signalling is not allowed in FIL).
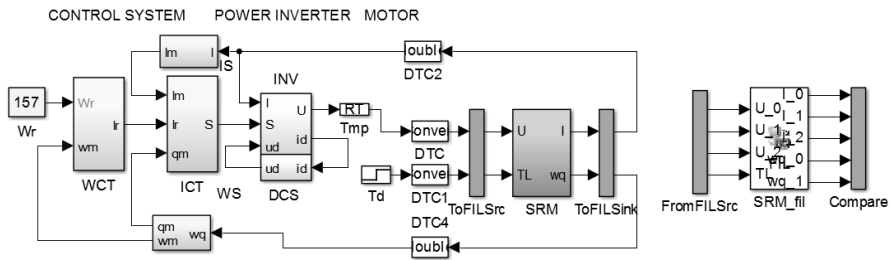

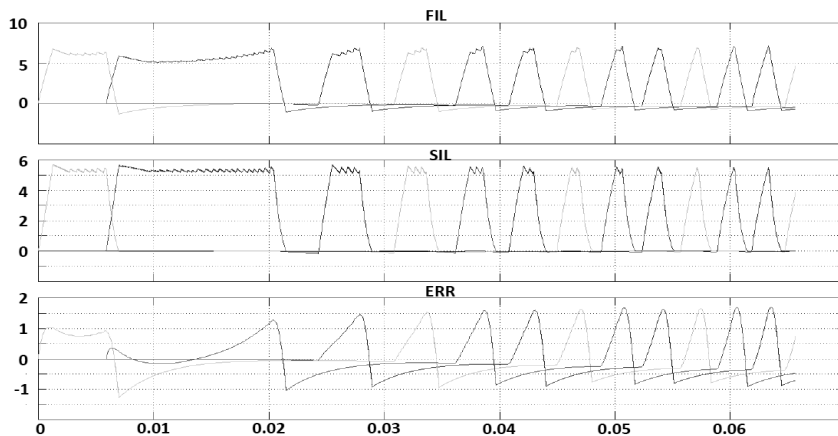Fig. 16. FIL cross-compilation result ready to test run

Fig. 17. Motor phases currents waveforms in FIL (top) and SIL (middle) structure with error signal (ERR - bottom) as an result of signals difference operation; horizontal axe X - time domain [s], vertical axe Y - current value [A]

4. SUMMARY

In the article there was presented FPGA in the loop solution for emulation purposes of selected elements of switched reluctance motor drive system. The FIL implementation was justified in the way of importance in fault tolerant control evaluation methodology that reduced overall research time and minimizes the risk of expensive hardware faults. SR motor model equations were introduced in general way to provide a reference for the presented model in Matlab/Simulink environment. FIL hardware system architecture (used evaluation board) was described with details about necessary start-up configuration: functional pinout affiliation to the RMII ethernet interface controller and dedicated instruction of HDL compiler binding.

All the necessary model adaptation for FIL usage was presented with several general and detailed restrictions pointed out. Finally, the FIL system compliance test results were presented in the way of motor phases current waveforms comparison to the SIL structure. The comparison shows general compliance of the systems, but some significant errors could be found – especially in dynamic states. Such a system could be used in preliminary control algorithm tests, but if precision required the FIL model should be reviewed. The proposed changes for the further research are: changing definition of fixed point variables to obtain higher computation accuracy, adding synchronization signal to the rotor position between SIL and FIL systems (aggregating computational errors of rotor position computation takes significant role in current waveforms comparison), look-up tables may be replaced by mathematical approximations – it is currently in the research scope as the part of parameterized self-adapting control system.

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