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Opto-Electronics Review

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# Two-step etch in n-on-p type-II superlattices for surface leakage reduction in mid-wave infrared megapixel detectors

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**Article info**

*Article history:*
Received 11 Oct. 2022
Received in revised form 9 Dec. 2022
Accepted 18 Dec. 2022
Available on-line 24 Feb.. 2023

*Keywords*:
Infrared detector; surface leakage; type-II superlattice; megapixel; n-on-p.

**Abstract**

This work investigates the potential of p-type InAs/GaSb superlattice for the fabrication of full mid-wave megapixel detectors with n-on-p polarity. A significantly higher surface leakage is observed in deep-etched n-on-p photodiodes compared to p-on-n diodes. Shallow-etch and two-etch-step pixel geometry are demonstrated to mitigate the surface leakage on devices down to 10 µm with n-on-p polarity. A lateral diffusion length of 16 µm is extracted from the shallow etched pixels, which indicates that cross talk could be a major problem in small pitch arrays. Therefore, the two-etch-step process is used in the fabrication of 1280 × 1024 arrays with a 7.5 µm pitch, and a potential operating temperature up to 100 K is demonstrated.

## 1. Introduction

Type II superlattice (T2SL) based on III-V materials has been proven to be a good solution for industrialisation of infrared (IR) detectors [1–5]. This technology is tunable from the extended short-wave infrared (eSWIR) to the longwave infrared (LWIR) region [6], and has enabled the reduction of the size, weight, and power consumption of IR imaging systems by increasing the operating temperature of the detectors [2, 7]. Recently, operating temperatures up to 150 K have been demonstrated for 640 × 512 focal plane arrays (FPAs) using an F/5.5 optical aperture designed for a full mid-wave infrared (MWIR) detection [8]. The maximum operating temperature of a detector is approximately set by the temperature at which the thermally generated current (dark current) is equal to the photo-activated current. These two magnitudes depend on both the intrinsic properties of the material and the fabrication process.

The fabrication process plays an important role in defining the operating temperature. On one hand, the absorption and, ultimately, the photocurrent in the diode can be increased above the intrinsic level by smart pixel designs implemented by processing of the material. This has been demonstrated, for instance, by reducing the reflection at the detector surface through the addition of antireflective coatings [9], by increasing the optical path length of the photons inside detector pixels using a double-pass configuration [10, 11] and by using structures to confine the light inside the pixels [5, 12]. On the other hand, the etching process to isolate individual diodes of the array can cause an increase of the dark current density by adding surface leakage. Surface leakage can be described with a trap-assisted recombination density at the mesa edge of the device [13] and results in dark current activated by majority carrier drift, tunnelling, generation-recombination (GR), or diffusion [13, 14]. For all these cases, the dark current degradation increases as the perimeter to the diode area ratio increases. Thus, it is crucial to tailor the fabrication processes to minimize any surface leakage current for high operating temperature and high-resolution arrays with small pixel sizes (> 1280 × 1024).

There are several ways of reducing the surface leakage from a design point of view. The first one consists of including a unipolar barrier in the structure to block the current flow of accumulated electrons on the detector sidewall. This solution has demonstrated to effectively reduce the majority carrier drift component of surface leakage [15, 16]. Another option is the use of absorbers

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https://doi.org/10.24425/opelre.2023.144556
1896-3757/ Association of Polish Electrical Engineers (SEP) and Polish Academic of Sciences (PAS). Published by PAS

with an n-type doping. With this choice of majority carriers, the band structure of the photodiode after etching is less impacted by the accumulation of electrons at pixel sidewalls, which results in less band bending across the structure [17, 18]. The n-type absorbers in InAs/InAsSb SL, combined with the longer minority carrier lifetimes of these superlattices, have led to exceptionally low dark current densities in MWIR detectors [3, 18], however, both barrier detectors and n-type structures can still suffer from surface leakage [16, 19, 20].

Finally, by design, the p-n junction of the photodiodes can be placed on the top of the absorber. In this configuration, the diodes can be isolated by a shallow mesa etch [21, 22], which minimizes the surface exposed. Planar- or shallow-etched detectors reduce the surface leakage and do not compromise the active area fill factor; however, the lateral transport of carriers can result in electrical cross talk between pixels [21–23]. The lateral diffusion length is an intrinsic characteristic of the material, but its effect on the total carrier collection increases as the diodes become smaller. This compromises the image quality of high-density pixel arrays with a small pixel pitch. To reduce the cross talk, full reticulation of the pixels is needed. In this case, it is better to place the p-n junction at the bottom of the structure to avoid a long exposure time to the etch process, which can induce more surface leakage [20, 23].

In the industrialization of T2SL detectors, the position of the p-n junction, however, cannot always be chosen only from a manufacturability perspective. The polarity of T2SL structure needs to be designed for assembly (DFA), as the detector arrays need to be hybridized to read out integrated circuits (ROIC) available. DFA is increasingly important since the design flexibility of T2SL has enabled the growth of bias selectable dual band structures [24, 25]. To fabricate the next generation detectors using dual polarity stacks, it is fundamental to develop fabrication techniques compatible with megapixel arrays to minimize the surface leakage regardless of the cut-off wavelength and position of the p-n junction.

In this work, we experimentally study the surface leakage dependence on the detector polarity for an MWIR InAs/GaSb p-type T2SL detector. Additionally, for the n-on-p structure, the effect of the pixel geometry on the current density is studied by fabrication of deep-etched, shallow-etched, and two-step etched pixels. The latter process scheme is a geometrical approach presented in Ref. 26 to reduce the surface leakage by blocking the surface carriers from the top contact. Originally, it was developed for LWIR detectors, and it was demonstrated to reduce the surface leakage on photodiodes with sizes down to 160 µm. In this work, its effectiveness on MWIR detectors and for pixels sizes compatible with megapixel FPAs is demonstrated. First, on photodiodes with sizes down to 10 µm, and second, implementing it in a fabrication of 1280 × 1024 detector arrays with a 7.5 µm pitch that showed a potential operating temperature up to 100 K.

## 2. Experimental section

The InAs/GaSb T2SL detectors studied were grown on Te-doped GaSb wafers by molecular beam epitaxy (MBE). The T2SL period thickness composing the p-type absorber was adjusted to achieve an energy bandgap of 248 meV (5 µm) at 77 K using eight-band **k·p** simulations [27] for full mid-wave detection. This design uses a double heterostructure configuration for GR and tunnelling dark current suppression to achieve the low dark current without blocking the photocurrent [28]. The corresponding band diagram is shown in Fig. 1(a).

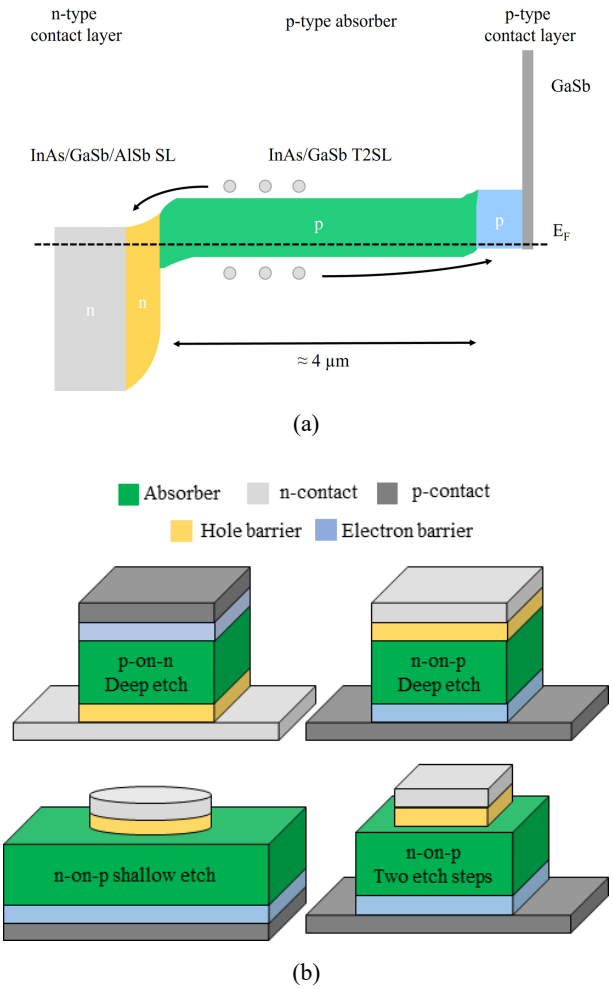


**Fig. 1.** Energy band diagram of the detector (a). 3D schematic view of the device with the regions composing the structure for the four geometries studied: p-on-n single deep etch, n-on-p single deep etch, n-on-p single shallow etch, and n-on-p two-etch steps (b).

Two different epi-wafers were grown using the same design, one with a p-on-n polarity and another with n-on-p. In the p-on-n structure, the absorber is grown on top of the junction, therefore, the photodiode needs to be fabricated by etching down to the bottom contact. To compare the surface leakage current on both structures, photodiodes with the sizes ranging from 10 to 223 µm were fabricated by etching down to the bottom contact for both epi-wafers. Photodiodes with the same sizes were fabricated on the n-on-p wafer with a shallow-etch and a two-step-etch process schemes to analyse the impact of the pixel geometry on the current density. Figure 1(b) shows a 3D schematic of the four configurations used for this study. For the shallow-etched devices, the top mesa etch is circular to avoid the corners effect in the extraction of the lateral diffusion length. For the two-step-etch samples, the top part of the pixel is etched down to the hole barrier with a 2 µm offset with respect to the mesa etch to block the surface current

[26]. The devices were not treated with an antireflection coating and were only used for dark current measurements.

## 3. Dark current analysis in p-on-n and n-on-p deep-etch devices

To evaluate the influence of detector polarity on detector performance, the dark current densities of deep-etched p-on-n and the n-on-p photodiodes are compared. Figure 2 shows the measured dark current density as a function of bias for pixel sizes ranging from 10 to 223 µm at 110 K for both polarities. The measurements were carried out inside a cryochamber with samples covered with a foil cap to prevent thermal irradiation from the background. The diode voltage for the n-on-p devices is presented as $-V_D$ for a direct comparison. For both configurations, the dark current density increases with decreasing pixel size, which indicates that surface leakage current is a dominating source of dark current in the detector. The dark current density level and the spread of dark current density with pixel size is much higher in the n-on-p photodiodes, indicating a higher impact of the surface leakage current in the n-on-p devices.

In the next step, the dominating dark current generation mechanisms are identified by analysing temperature dependence of the dark current density. Figure 3 presents the Arrhenius plot of the dark current measured from 90 to 200 K for 223 µm and 10 µm pixels of each design at the operating bias ($|V_D| = 0.1$ V). In the same figure, the Arrhenius plots with activation energies corresponding to the bandgap (dotted lines, Fig. 3) and half bandgap (dashed lines, Fig. 3) of the detector material are presented.

For the p-on-n structure, a good fit is obtained with the GR and diffusion activation energies at low and high temperatures, respectively [Fig. 3(a)]. The transition temperature between these two regimes is 130 and 150 K for 223 and 10 µm devices, respectively. For both regimes, the current density of the small pixel is higher than in the large pixel because of the increasing contribution of surface leakage current as pixel size decreases. The activation ener-

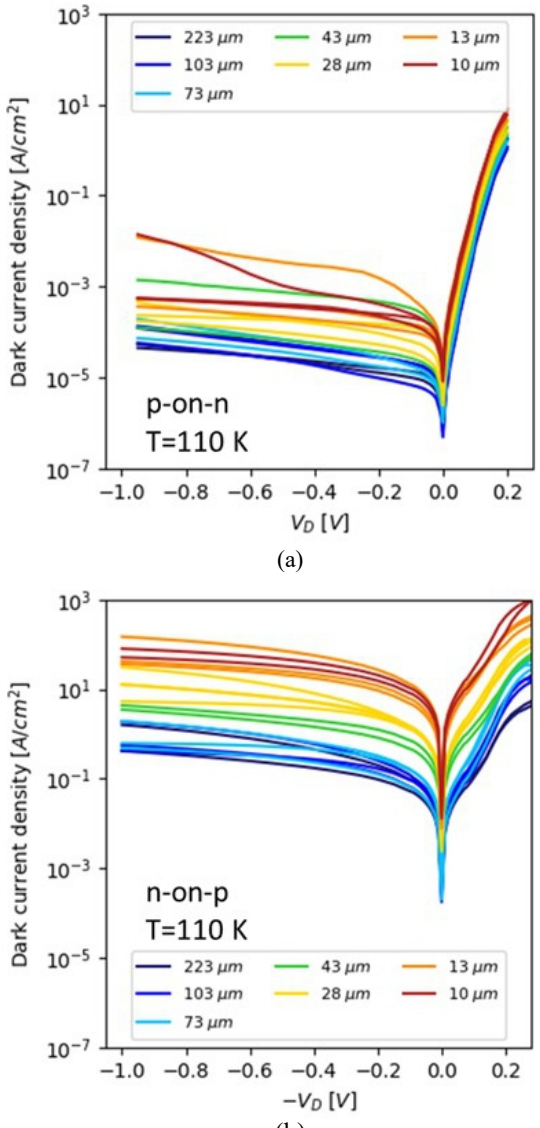


**Fig. 2.** Measured dark current density at 110 K for different pixel sizes of p-on-n (a) and n-on-p (b) configuration as a function of $V_D$.

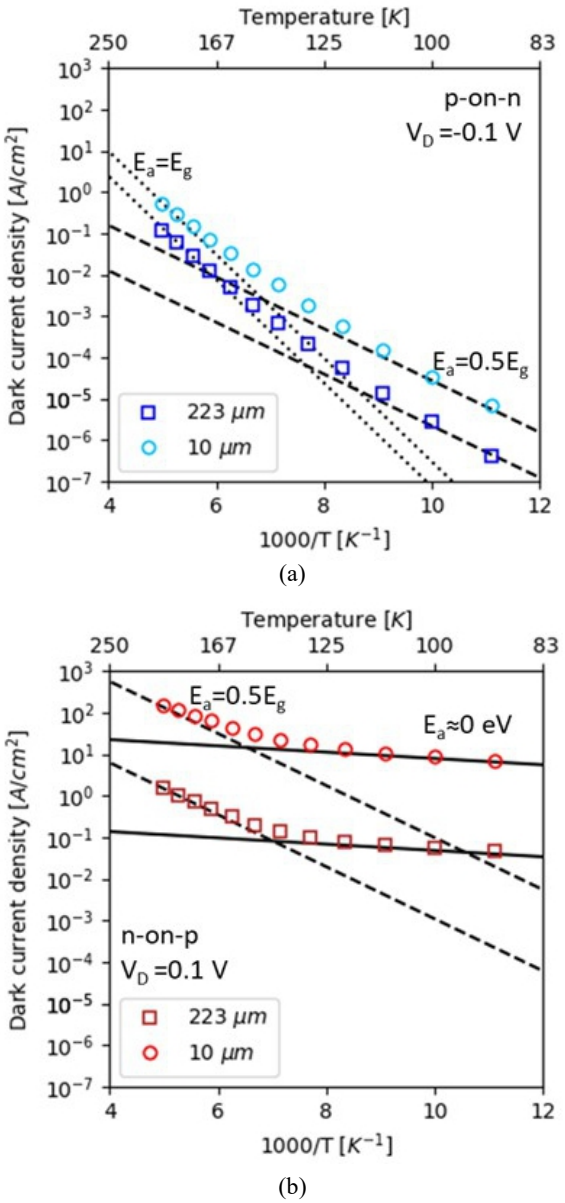


**Fig. 3.** Measured dark current density at $|V_D| = 0.1$ V of 223 µm and 10 µm sized diodes for p-on-n (a) and n-on-p (b) structure as function of the inverse temperature.

gies of the surface leakage components are $E_{\mathrm{a,surf}} = 1/2E_g$, $E_{\mathrm{a,surf}} = E_g$ indicating that surface current densities in this case emanate from GR and diffusion mechanisms [13, 14, 20].

In the n-on-p structure, the dark current density in the devices have activation energies corresponding to half bandgap in the high temperature range, while the dark current density in the low temperature range is almost independent from the temperature, with an activation energy of 0.015 eV [Fig. 3(b)]. This dark current mechanism is not originating from the minority carrier flow in the intrinsic material, instead it corresponds to a majority carrier drift at the surface (inverted to n-type) which shunts the device [14, 16, 19]. At higher temperature, the n-on-p devices show a GR activation energy as the minority carrier current dominates over surface drift current. The surface nature of both the GR- and the surface-drift mechanisms in these n-on-p diodes is the reason why the smaller pixel has a higher dark current density than larger pixels while the activation energies stay the same ($E_{\mathrm{a,surf}} = 1/2E_g$, $E_{\mathrm{a,surf}} \approx 0\ eV$ [13, 14, 16, 19].

The strong surface degradation observed in n-on-p devices is attributed to that the p-n junction is being more exposed during the etching process compared to p-on-n devices when the barrier is positioned below the absorber [19–21]. This makes the fabrication of detectors with n-on-p polarities (with p-type absorbers) challenging.

## 4. High resolution FPA using n-on-p detectors

To investigate if the elevated dark current density in the n-on-p devices can be mitigated by changing the photodiode geometry, shallow-etched and two-step-etched geometries are compared to the deep-etched photodiodes. The offset between the two-etch steps (2 µm) results in a step-like profile diode with a reduced top area [Fig. 1(b)]. This configuration makes it difficult to include a metal pad for wire bonding. Instead, and to avoid the physical damage of wire bonding on the diode, the authors probed directly on the top of the pixels. The measurements on the three samples were, therefore, carried out with a cryoprobe station. Figure 4 shows the measured current density as a function of bias for pixel sizes ranging from 10 to 223 µm at 80 K for the three-etch geometries. As the samples in the cryoprobe are also affected by thermal irradiation from the background, the current density is dominated by a photocurrent in the cases when the dark current density is very low.

As shown in the previous section, deep-etched devices suffer from surface leakage with $E_{\mathrm{a,surf}} \approx 0\ eV$ which results in a high current density with large spread in size [Fig. 4(a)]. In this case, the measured current density at 80 K is above the photocurrent level (set by the background flux) for all device sizes.

For the shallow-etch geometry, the measured current [Fig. 4(b)] is lower than for deep-etch detectors for all the diode sizes (the measurement is, however, limited by the photonic flux). Decrease of the current density is attributed to that the sidewalls of the photodiodes are not exposed to etching and, thereby, protected against surface leakage [23]. The measured current density also increases for the smaller pixels, however, in this case, a higher current is not

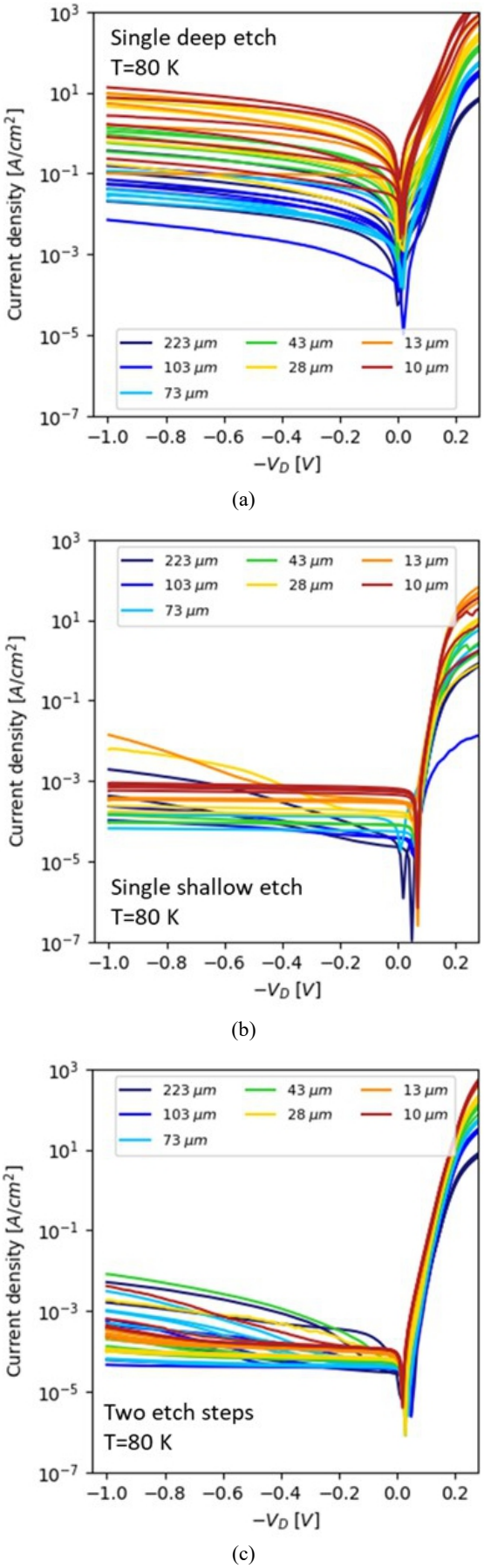


**Fig. 4**. Measured current density at 80 K for different pixel sizes on the n-on-p structure for a single deep etch (a), single shallow etch (b), and two-etch-step geometries as a function of $V_D$.

a result of surface leakage. Indeed, the higher current density in the small pixels originates from the lateral contribution of the minority carriers as the active volume exceeds the one defined by the shallow etch [21–23]. The lateral diffusion length of the material can be extracted by considering the total area contributing to the current measurements according to (1) [21, 23]

$$A_{total} = \pi\left(\frac{1}{4}\rho^2 + \rho L_{\parallel} + L_{\parallel}^2\right), \quad (1)$$

where $\rho$ is the diode diameter and $L_{\parallel}$is the lateral diffusion length. Figure 5 shows the measured current for the shallow-etch pixels at $V_D = 0.1$ V as a function of the diode mesa size. The inset in the figure includes a schematic lay out of a circular mesa diode with an additional surface area created by $L_{\parallel}$. Under the assumption that the total current is proportional to the active area from (1) [21, 23], the quadratic fit of the current in front of $\rho$ yields to the extraction of the lateral diffusion length of $L_{\parallel} = 16$ µm, which is in line with what other groups have reported [21–23]. Since the lateral contribution can lead to electrical cross talk, especially when the pixel size reduces to sizes comparable to $L_{\parallel}$, the shallow etch is not a suitable process for fabrication of HD FPAs as pixels are required to be small and close to each other (< 10 µm pitch) to achieve a high fill factor.

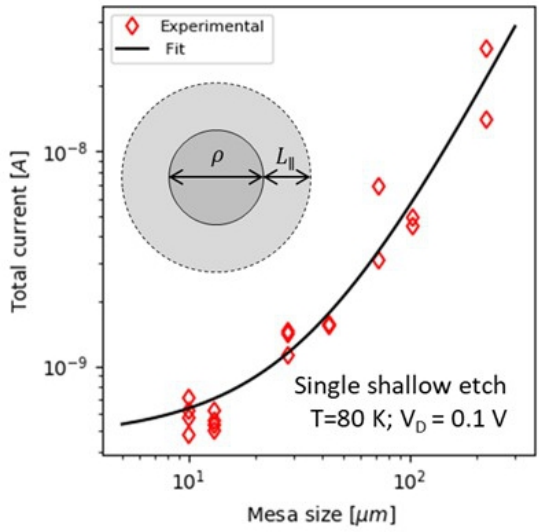


**Fig. 5.** Measured (symbols) and fitted (solid line) current at $V_D = 0.1$ V as a function of the shallow-etch mesa size at 80 K. The inset shows a diagram of the area contribution to the current for a circular diode of size $\rho$ and lateral diffusion length $L_{\parallel}$.

For the devices fabricated by the two-etch-step process [illustrated in Fig. 1(b)], the current measurements are presented in Fig. 4(c). A significant reduction of the current compared to the single deep etch devices is observed, with current values comparable to the shallow-etch devices (here limited by the photonic flux). This reduction in current is attributed to an extended barrier blocking surface carriers [26]. This methodology was previously demonstrated in Ref. 26 for LWIR and pixel sizes down to 160 µm, while here the efficiency of the two-step etch is demonstrated for MWIR T2SL detectors, for pixels sizes compatible with megapixel FPAs (10 µm).

Figure 4(c) also shows that some of the large devices have a higher current density in the high reverse bias regime ($-V_D < -0.5$ V). In this regime, the current is limited by the GR component which is a current component emerging from the depletion region, i.e., electric field region. With the two-etch-step configuration, the depletion region volume is reduced, compared to a standard pixel configuration, as it gets confined in the volume defined by the first etch. For a constant etch offset like the one used in this work (2 µm), this reduction is more important for smaller diodes as the etched volume relative to the total diode volume is higher. The confinement of the depletion region in a volume smaller than a total pixel volume can result in a reduced GR component, especially for small pixels.

The full isolation of the absorber and the low current density achieved with single pixels fabricated with a two-etch step made this approach an appropriate processing scheme for continued fabrication of 1280 × 1024 detector arrays with a 7.5 µm pitch using n-on-p polarity on the detector side. The result of the fabrication process is shown in Fig. 6 with a scanning electron microscopy (SEM) image of the detector cross section before hybridisation with an indium bump on each photodiode. To illustrate the final detector structure, a diagram of detector different regions is superimposed in one of the pixels from the array.

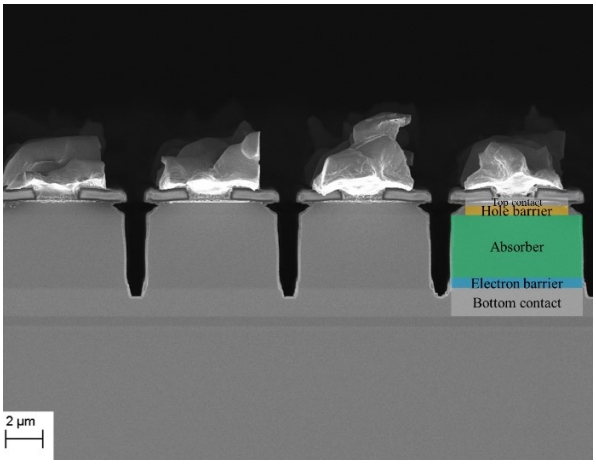


**Fig. 6.** SEM image of the fabricated detector array using two-etch steps before hybridization operation.

As in the single pixels, the top contact and hole barrier were etched first. However, in the array configuration and for such small pitches, the width of the first etch is limited as a remaining minimum top pixel surface is required for the hybridisation to the ROIC. For the FPAs, 850 nm of semiconductor material were etched on each side of the pixel. The second etch was performed down to the bottom contact to fully reticulate the pixels. High fill factor of the absorber region is achieved thanks to the vertical sidewalls achieved by the dry etching.

The detector was hybridized to a silicon fan-out board with metal pads connecting to pixels of the array. Figure 7(a) shows the measured dark current density as a function of bias for the test 7.5 µm pitch pixel on the array for temperatures ranging from 70 K to 200 K. For this measurement, the pixel had the contacts on the fan-out board, so the measurements could be carried out inside a cryochamber with a hybridized chip covered with a foil cap

to prevent thermal irradiation from the background. By reducing the surface leakage compared to deep-etched devices, dark current densities at the operating bias as low as $1.2\,10^{-5}$ and $8.8{\cdot}10^{-5}$ A/cm$^2$ at 90 K and 100 K are achieved. Figure 7(b) presents the Arrhenius plot corresponding to the dark current values at $V_D = 0.1$ V for the FPA pixel compared to the single deep-etch 10 µm diodes with p-on-n and n-on-p polarities. The photocurrent level corresponding to an optical aperture of F/2.75 is plotted to estimate the maximum operating temperature of the FPAs.

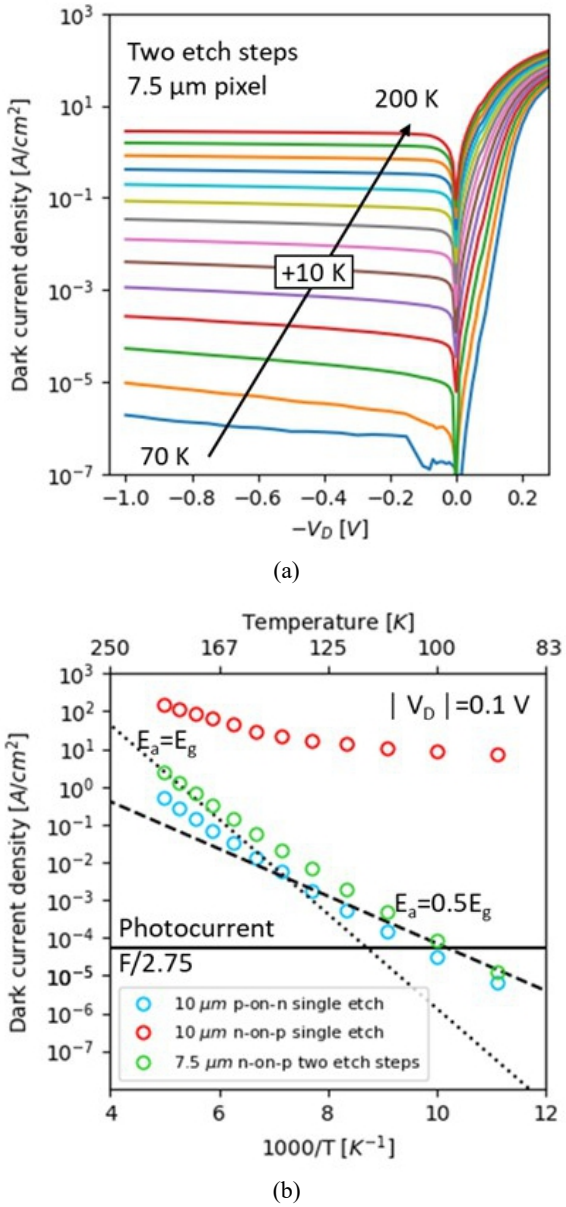


**Fig. 7.** Measured dark current density: of a test pixel on the n-on-p 1280×1024 detector array for different temperatures ranging from 70 to 200 K as a function of $V_D$ (a); Measured dark current density at $|V_D| = 0.1$ V of the FPA test pixel and the single deep etch n-on-p and p-on-n 10 µm diodes as function of the inverse temperature (b).

The dark current density fits to the activation energies corresponding to bandgap for temperatures higher than 140 K and half bandgap of the detector absorber below that. The profile offset in the two-etch step process successfully blocks the drift component of the current identified in the single etch n-on-p devices. This is achieved without compromising the operating bias of the detector as it is a result of extending the barrier only for the surface carriers [26]. Additionally, the surface GR and diffusion current components are reduced to a level comparable to a 10 µm p-on-n device, showing a current density less than three times higher at 100 K with a smaller diode size. As a result, the dark current density level obtained is low enough to enable the operation at 100 K of 1280×1024 FPAs with a 7.5 µm pitch assuming F/2.75. This demonstrates the two-step etch as an appropriate process scheme for the reduction of surface leakage and feasibility of megapixel FPAs using the n-on-p polarity.

## 5. Conclusions

In this work, we have presented an experimental study of the surface leakage dependence on the detector polarity and photodiode geometry for the MWIR InAs/GaSb p-type T2LS detector with diodes sizes compatible with megapixel FPAs. In the n-on-p fully etched devices, higher dark current densities are observed than in the p-on-n counterparts. This is a result of an additional GR and drift surface leakage components observed in the n-on-p devices. The strong surface degradation is attributed to a long exposure of the p-n junction to the etch process, during deep etching of the devices. To circumvent this effect, we fabricated n-on-p diodes with different geometries: shallow-etched and two-step-etched which demonstrated a reduction of the current density compared to the single deep-etched devices. Finally, for the first time, the two-etch-step pixel geometry is applied in the fabrication of a 1280×1024 FPA with a 7.5 µm pitch that showed a significantly reduced dark current density and a potential operating temperature up to 100 K assuming F/2.75.

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