The Microcontroller Implementation of the Basic Fractional-Order Element

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Abstract: The paper presents the implementation of the basic fractional order element s^γ, $\gamma \in \mathbb{R}$ on the STM32 microcontroller platform. The implementation employs the typical CFE and FOBD approximations, the accuracy of approximation as well as duration of calculations are experimentally tested. Microcontroller implementation of fractional order elements is known; however, real-time tests of such implementations have been not presented yet. Results of experiments show that both methods can be implemented at the considered platform. The FOBD approximation is more accurate, but the CFE one is faster. The presented experimental results prove that the STM32F7 family processor could be used to develop the embedded fractional-order control systems for a broad class of linear and nonlinear dynamic systems. This is crucial during the implementation of the fractional-order control in the hard real-time or embedded systems.

Keywords: fractional-order systems, microcontroller, STM32, FOBD, CFE approximation

1. Introduction

Fractional calculus is not a new idea. It was mentioned first time in 1695 in a letter from L'Hopital to Leibniz [12]. L'Hopital asked a question about the *n*-th derivative of the linear function – what would happen if *n* would be ½.

With the increasing computational speed of computers, we can solve more and more difficult mathematical problems. One of those is fractional order calculus, which requires a lot of computing power. Many papers deal with this subject in various aspects, e.g. adaptive control [30], chaotic systems [7, 31], Kalman filter [27], PID controller [29].

The use of fractional calculus in digital control requires to implement the basic element s^γ at a digital platform. It can be done in different ways and using different hardware platforms. The PLC implementation is discussed, i.e. in [16]. The microcontroller implementation using the discrete ORA approximation is thoroughly discussed [1, 2, 25, 28]. However, unlike this article, the mentioned papers do not deal with performance analysis of microcontroller implementations of fractional calculations. Such an analysis is necessary to the industrial, microcontroller-based implementation of fractional-order controllers, for example, fractional-order PID controller. Based on this paper, it will be possible to conclude whether the complicated calculations for a controller with a fractional-order calculus can be performed on microcontrollers for real-time systems.

This paper deals with the classic discrete approximations: Continuous Fraction Expansion (CFE) and Fractional Order Backward Difference (FOBD), basing on the Grünwald-Letnikov definition. It is analysed with details, for example, in the book [23]. The main difference between those approximations (CFE and FOBD) consists of memory length necessary to obtain the reasonable accuracy and form of discrete transfer function describing it [13]. The CFE requires us to use much less memory and is faster convergent, but its accuracy is generally a little bit worse than FOBD. Furthermore, it requires us to use past values of both output and control signals. On the other hand, the FOBD assures better accuracy, but the memory length necessary to achieve this accuracy is relatively much bigger.

This paper is devoted to discussing both the accuracy and speed of calculations. The paper is organised as follows. In the beginning, elementary ideas from discrete fractional calculus are recalled. Particularly the discrete version of the Grünwald-Letnikov definition and CFE approximation are given. Next, the experimental system is presented, and results of experiments are given and discussed.

2. Preliminaries

A presentation of elementary ideas is started with a definition of a fractional-order, integro-differential operator. It was given, for example by [6, 11, 26]:

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Definition 1. (The elementary fractional-order operator) The fractional-order integro-differential operator is defined as follows:

$$ {}_aD_t^{\gamma} f(t) = \begin{cases} \dfrac{d^{\gamma} f(t)}{dt^{\gamma}} & \gamma > 0 \\ f(t) & \gamma = 0 \\ \int\limits_a^t f(\tau)(d\tau)^{\lambda} & \gamma < 0 \end{cases} \qquad (1) $$

where a and t denote time limits for operator calculation, $\gamma \in \mathrm{R}$ the non-integer order of the operation.

Next, the complete Gamma function needs to be recalled:

$$ \Gamma(x) = \int\limits_0^{\infty} t^{x-1} e^{-t} dt. \qquad (2) $$

The fractional-order, the integro-differential operator can be described by different definitions, given by Grünwald and Letnikov (GL definition), Riemann and Liouville (RL definition) and Caputo (C definition). In further consideration, GL definition will be used. It is as follows [4, 23]:

Definition 2. (The Grünwald-Letnikov definition of the FO operator)

$$ {}_0^{GL}D_t^{\gamma} f(t) = \lim_{h \to 0} h^{-\gamma} \sum_{l=0}^{\left[\frac{t}{h}\right]} (-1)^l \binom{\gamma}{l} f(t - lh). \qquad (3) $$

In (3) $\binom{\gamma}{l}$ is the binomial coefficient:

$$ \binom{\gamma}{l} = \left\{ \begin{matrix} 1, & l = 0 \\ \dfrac{\gamma(\gamma-1)\ldots(\gamma-l+1)}{l!}, & l > 0 \end{matrix} \right\}. \qquad (4) $$

The GL definition is the limit case for $h \to 0$ of the Fractional Order Backward Difference (FOBD), commonly employed in discrete Fractional Order (FO) calculations (see for example [23], p. 68):

Definition 3. (The Fractional Order Backward Difference-FOBD)

$$ (\Delta^{\lambda} x)(t) = \frac{1}{h^{\gamma}} \sum_{l=0}^{L} (-1)^l \binom{\gamma}{l} x(t - lh). \qquad (5) $$

Denote coefficients $(-1)^l \binom{\gamma}{l}$ by d_l:

$$ d_l = (-1)^l \binom{\gamma}{l}. \qquad (6) $$

The coefficients (6) can also be calculated with the use of the following, equivalent recursive formula (see for example [4], p. 12), useful in numerical calculations:

$$ d_0 = 1 $$

$$ d_l = \left(1 - \frac{1+\gamma}{l}\right) d_{l-1}, \quad l = 1, \ldots, L. \qquad (7) $$

It is proven in [3] that:

$$ \sum_{l=1}^{\infty} d_l = 1 - \gamma. \qquad (8) $$

From (7) and (8) we obtain at once that:

$$ \sum_{l=2}^{\infty} d_l = 1. \qquad (9) $$

The expression (5) with coefficients calculated using (7) can be directly implemented at microcontroller to calculate fractional-order difference or integral.

An alternative formula to calculate FO operator is to use CFE approximation. It has the form of Infinite Impulse Response (IIR) filter containing both poles and zeros. It is faster convergent and easier to implement due to its relatively low order, typically not higher than 5. It has the form of the discrete transfer function $G_{CFE}(z^{-1}, \gamma)$, obtained after discretisation of the fractional-order element s^{γ}, $\gamma \in \mathbb{R}$ with the use of the so-called generating function $s \approx \omega(z^{-1})$. The new operator raised to power γ has the following form (see for example [5], [24, p. 119]):

$$ \left[w(z^{-1})\right]^{\gamma} = G_{CFE}(z^{-1}, \gamma) = \left(\frac{1+a}{h}\right)^{\gamma} CFE\left[\left(\frac{1 - z^{-1}}{1 + az^{-1}}\right)^{\gamma}\right]_{M,M} = $$

$$ = \frac{P_{\gamma M}(z^{-1})}{Q_{\gamma M}(z^{-1})} = \left(\frac{1+a}{h}\right)^{\gamma} \frac{CFE_N(z^{-1}, \gamma)}{CFE_D(z^{-1}, \gamma)} = \frac{\sum\limits_{m=0}^{M} w_m z^{-m}}{\sum\limits_{m=0}^{M} v_m z^{-m}}. \qquad (10) $$

In (10) a is the coefficient depending on approximation type (for example: $a = 0$ for Euler approximation, $a = 1$ for Tustin approximation), h denotes the sample time, M is the order of approximation. If the Tustin approximation is considered ($a = 1$) then $CFE_D(z^{-1}, \gamma) = CFE_N(z^{-1}, -\gamma)$ and the polynomial $CFE_D(z^{-1}, \gamma)$ can be given in the direct form (see [5]). Examples of polynomial $CFE_D(z^{-1}, \gamma)$ for $M = 1, 3, 5$ are given in Table 1.

Table 1. Coefficients of CFE polynomials CFEN,D(z–1, γ) for Tustin approximation based on [5]

Tabela 1. Współczynniki wielomianów CFE CFEN,D(z–1, γ) dla aproksymacji Tustina na podstawie [5]

Order M	wm	vm
$M = 1$	$w_1 = -\gamma$	$v_1 = \gamma$
	$w_0 = 1$	$v_0 = 1$
$M = 3$	$w_3 = -\gamma/3$	$v_3 = \gamma/3$
	$w_2 = \gamma^2/3$	$v_2 = \gamma^2/3$
	$w_1 = -\gamma$	$v_1 = \gamma$
	$w_0 = 1$	$v_0 = 1$
$M = 5$	$w_5 = -\gamma/5$	$v_5 = \gamma/5$
	$w_4 = \gamma^2/5$	$v_4 = \gamma^2/5$
	$w_3 = -(\gamma/5 + 2\gamma^3/35)$	$v_3 = -(-\gamma/5 - 2\gamma^3/35)$
	$w_2 = 2\gamma^2/5$	$v_2 = 2\gamma^2/5$
	$w_1 = -\gamma$	$v_1 = \gamma$
	$w_0 = 1$	$v_0 = 1$

Finally, the analytical formula of the step response for the basic FO element s^{γ} should be recalled. It is as follows [4]:

$$y(t) = \frac{t^{-\gamma}}{\Gamma(1-\gamma)}. \tag{11}$$

where $\Gamma(..)$ is the complete Gamma function (2). The above formula will be employed as the reference to estimate the accuracy of approximations implemented at a microcontroller.

3. The experimental microcontroller platform

The diagram of the embedded system used in experiments is shown in Figure 1. The STM32F767ZI device is based on the high-performance Arm Cortex-M7 32-bit RISC core operating at up to 216 MHz frequency. The Cortex-M7 core features a floating-point unit (FPU) which supports Arm double-precision and single-precision data-processing instructions and data types. It also implements a full set of digital signal processor(DSP) instructions. The embedded system was tested using the following peripheral blocks integrated in the structure: static random-access memory (SRAM) memory for storing data tables, timers/counters units capable of interrupts and a serial port universal asynchronous receiver-transmitter (UART). The processed data are duly transmitted (via UART port), monitored and uploaded to a PC.

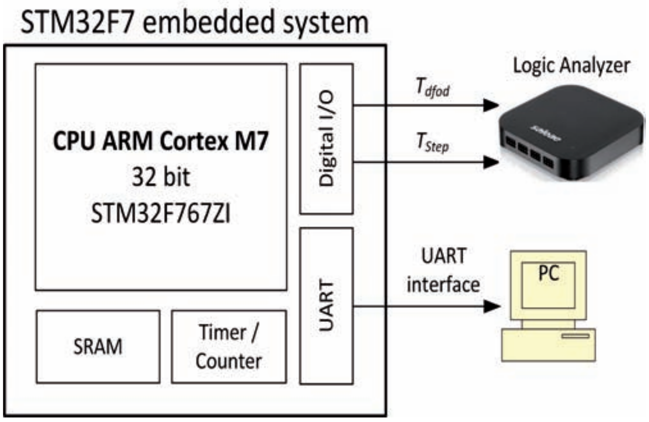

Fig. 1. The experimental system
Rys. 1. Układ eksperymentalny

Logic Analyser of the Logic Pro 16 (Saleae Corporation) is used to monitor and collect digital information from a digital I/Os of the embedded system. Two digital output pins of STM32F767ZI processor are used to measure the duration of calculations using the approximation of the digital fractional-order differentiator/integrator $T_{df\ od}$ and one step time duration of the differentiator/integrator unit step response T_{Step}. The accuracy of time measurement is 20 ns (50 MSample/s). All the data is saved to specific log files to be analysed off-line.

4. Implementation

The application running on STM32F7 processor is generally divided into two parts. The first part contains the code responsible for the hardware configuration and algorithm for calculating fractional-order operator parameters. This algorithm is activated after processor power-on reset and on demand, e.g. when a user changes the parameters of the approximating model (M, a, etc.) or fractional order of the operation. The two fractional modules: differentiator s^{α} and integrator $1/s^{\alpha}$ are implemented in the form of timer interrupt service routine. A selected STM32F7 timer device generates one interrupt every 0.02 s. Notably, the time the interrupt-driven procedure is incorporating a code of two approximation methods: CFE and FOBD (but only one can be active at a time). All data necessary for the correct operation of the calculation procedure (transfer function parameters for CFE, historical data for CFE and FOBD methods, etc.) are stored in the processor RAM. Input signals used to perform functional tests of CFE and FOBD methods are generated by software (e.g. step, square wave, sine wave). It is also possible to use external input signals, connected, for example, to A/D converter, PWM digital input or set via a selected serial interface.

The input (control) and output (results) data are transferred to the PC (MATLAB application) by using a serial UART interface. The source files of all elements of the application are written with the use of C language.

5. Cost functions

Cost function describes a difference between analytical step response (11) and approximated step responses using CFE and FOBD. They are calculated at the same time mesh with the sample time h. In this paper two cost functions were employed.

The first one is the MSE (Mean Square Error) cost function:

$$MSE = \frac{1}{K_s}\sum_{k=1}^{K_s}\left[y_e(k) - y(k)\right]^2. \tag{12}$$

In (12), K_s is the number of samples collected during the experiment. The analytical response in k-th time moment calculated using (11) is denoted by $y(k) = y(kh)$, $k = 1, ..., K_s$ and the approximated response calculated at microcontroller in the same moment is denoted by $y_e(k)$.

The next considered cost function is the fitting function (13):

$$FIT = \frac{\left\|y - y_e\right\|}{\left\|y - \overline{y}_e\right\|}. \tag{13}$$

In (13) $\overline{y}_e$ is the average value from experimental result y_e.

6. Experiments

Experiments were executed for different parameters of CFE and FOBD methods. Recorded data are sampled with the frequency of 50 Hz (the periodical interrupt-driven function of STM32 processor). The duration of the experiments was set to 20 s or 40 s. Measurement data were recorded, analyzed and processed using a PC with MATLAB/Simulink package. The CFE method parameters applied in experiments were following: sample time was equal: $h = 0.02$ s, the order of CFE approximation was equal $M = 5$, $a = 0$ (the Euler method was applied). In FOBD, the memory was $L = 100$ samples long. As the reference the analytical step response (11) was employed. It is worth noting that all calculations on the STM32F7 processor carried out using double precision data type.

Figure 2 presents experimental frequency characteristic of the fractional differential unit of the CFE method with parameter γ set as 0.5. Similar results are presented in Figure 3 for experimental frequency characteristic of the fractional integral unit of the CFE method with parameter γ set as –0.5. The same plots were obtained for FOBD method. Figure 4 presents the experimental frequency characteristics of the fractional dif-

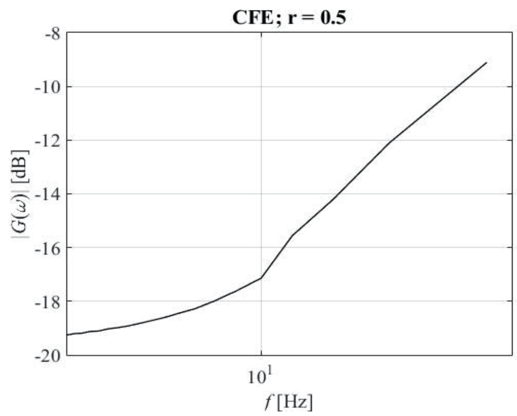

Fig. 2. Experimental frequency characteristic of the derivative element, CFE approximation
Rys. 2. Eksperymentalna charakterystyka częstotliwościowa części różniczkującej, aproksymacja CFE

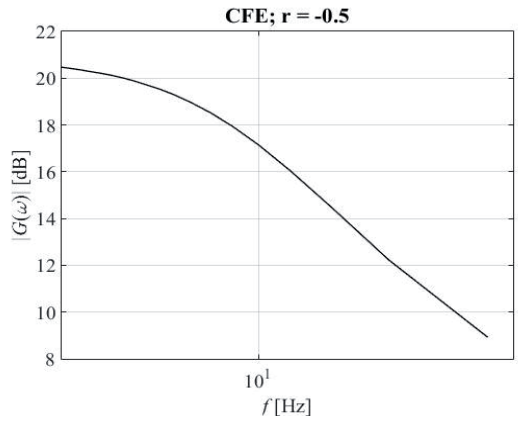

Fig. 3. Experimental frequency characteristic of the integral element, CFE approximation
Rys. 3. Eksperymentalna charakterystyka częstotliwościowa części całkującej, aproksymacja CFE

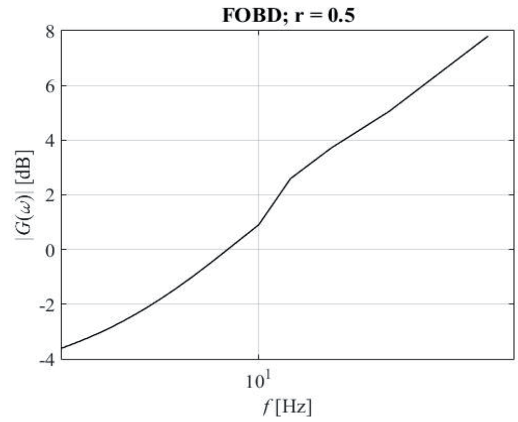

Fig. 4. Experimental frequency characteristic of the derivative element, FOBD approximation
Rys. 4. Eksperymentalna charakterystyka częstotliwościowa części różniczkującej, aproksymacja FOBD

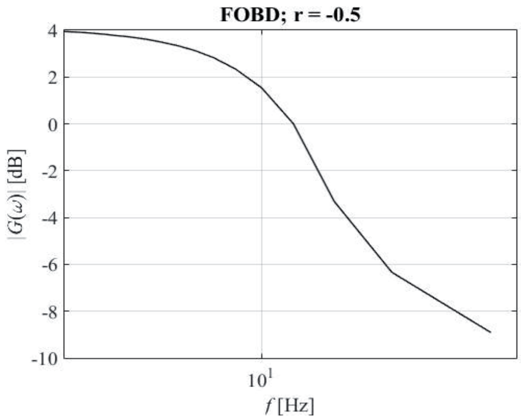

Fig. 5. Experimental frequency characteristic of the integral element, FOBD approximation
Rys. 5. Eksperymentalna charakterystyka częstotliwościowa części całkującej, aproksymacja FOBD

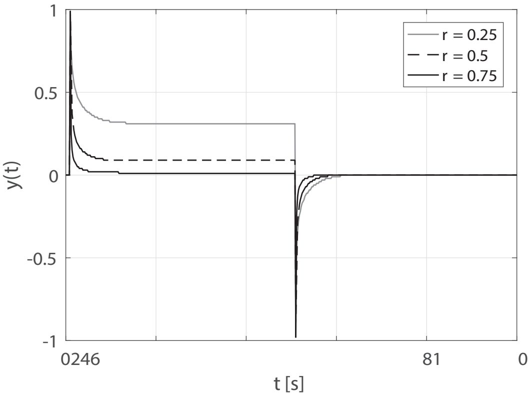

Fig. 6. The step responses of the derivative element, CFE approximation
Rys. 6. Odpowiedź skokowa części różniczkującej, aproksymacja CFE

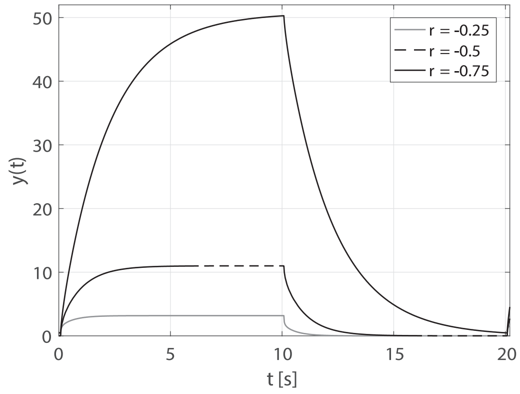

Fig. 7. The step responses of the integral element, CFE approximation
Rys. 7. Odpowiedź skokowa części całkującej, aproksymacja CFE

ferential unit of the FOBD method with parameter GAMMA set as 0.5. Similar results are presented in Figure 5 for experimental frequency characteristics of the fractional integral unit of the FOBD method with parameter GAMMA set as –0.5. The results were obtained for the frequency range from 2.5 Hz to 50 Hz (both CFE and FOBD method).

Figure 6 presents the step responses of the fractional differential unit for the three values of parameter γ of the CFE method: 0.25, 0.5 and 0.75. The output values are not scaled by the factor k. Figure 7 compares the step responses of the fractional integral unit for the three values of parameter γ of the CFE method: 0.25, 0.5 and 0.75. The output values are not scaled by the factor k. Figures 8 and 9 show the use of the FOBD approximation. Figure 7 compares the step responses of the fractional integral unit for the three values of parameter γ of the CFE method: 0.25, 0.5 and 0.75. The output values are not scaled by the factor k. The performance of both approximations in the sense of cost functions (12) and (13) is

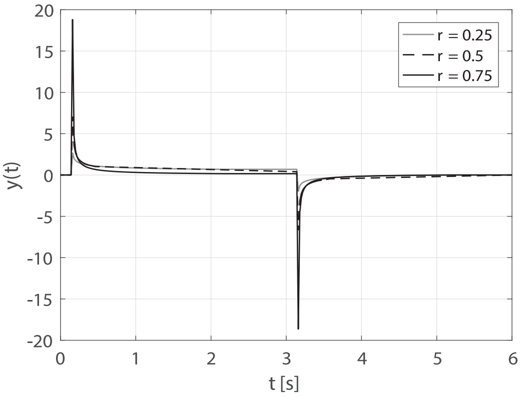

Fig. 8. The step responses of the derivative element, FOBD approximation
Rys. 8. Odpowiedź skokowa części różniczkującej, aproksymacja FOBD

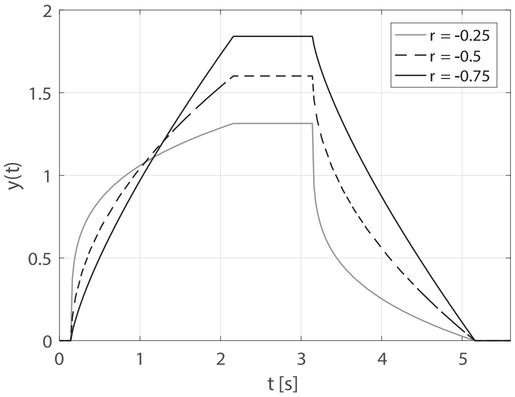

Fig. 9. The step responses of the integral element, FOBD approximation
Rys. 9. Odpowiedź skokowa części całkującej, aproksymacja FOBD

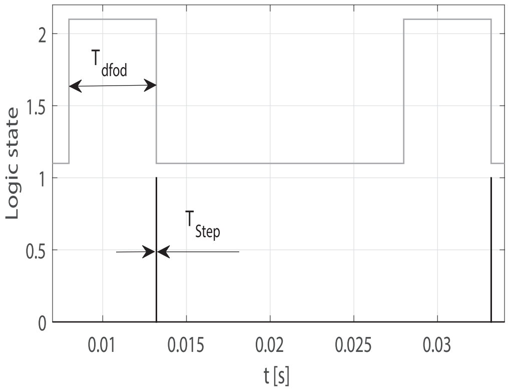

Fig. 10. The sequence of tests during real-time measurements
Rys. 10. Sekwencja testów podczas pomiarów w czasie rzeczywistym

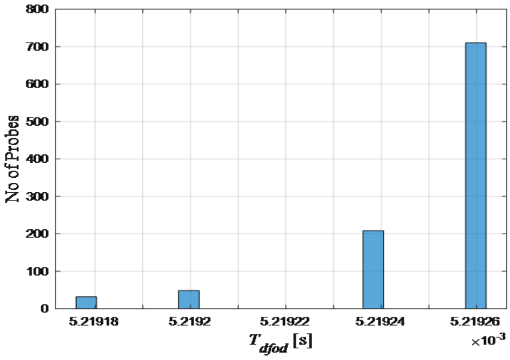

Fig. 11. Histogram of the duration Tdf od for CFE
Rys. 11. Histogram czasu trwania Tdf od dla CFE

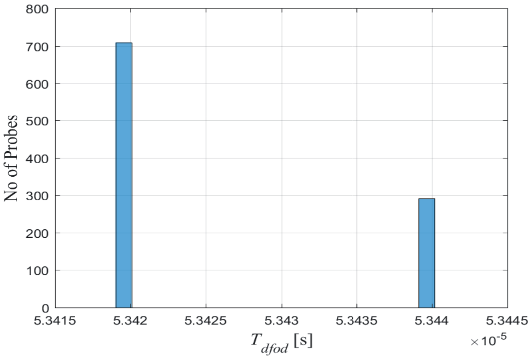

Fig. 12. Histogram of the duration Tdf od for FOBD
Rys. 12. Histogram czasu trwania Tdf od dla FOBD

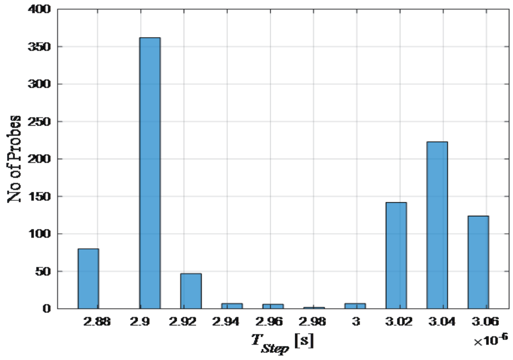

Fig. 13. Histogram of the duration TStep for CFE
Rys. 13. Histogram czasu trwania TStep dla CFE

presented in Tables 2 and 3. The analysis of both tables allows concluding that generally the use of FOBD allows obtaining an approximation more accurate in the sense of examined cost functions. The only exception is observed for $\gamma = 0.75$ when the CFE is more accurate than FOBD. Generally, this conclusion is not surprising.

The next important problem during tests of the proposed solution is meeting the real-time requirements. Tests of calculation speed should be done during calculation of coefficients as well as of the step response. Figure 10 shows trends of logic states for two STM32F767ZI processor digital outputs employed during measuring of the duration of coefficients calculation $T_{df\ od}$ and step response calculation T_{Step}. The total number of probes was equal to 1000.

The logic state of the output was reset before the execution of the analysed code section and then reset after task completion. The limits of the measurement procedure: $T_{df\ od}$ and T_{Step} are marked with arrows in Figure 10. Both durations

$T_{df\ od}$ and T_{Step} for CFE approximation are illustrated by histograms 11 and 13, and for the FOBD method use are given in Figures 12 and 14.

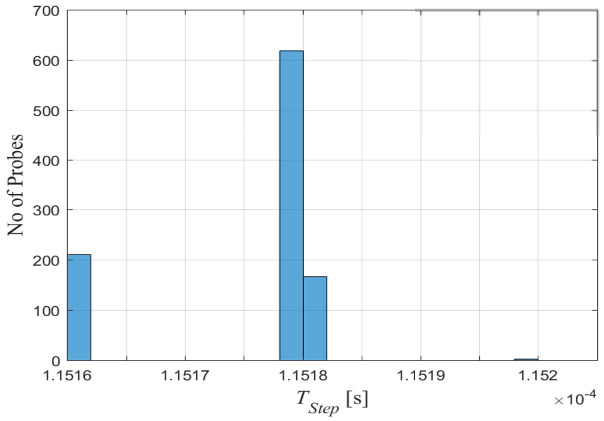

Fig. 14. Histogram of the duration TStep for FOBD
Rys. 14. Histogram czasu trwania TStep dla FOBD

In histograms 11 and 12 we can see that the coefficients of the CFE approximation are calculated 100 times longer than for FOBD although their number is much smaller. Their higher computational complexity causes this (see Table 1). The coefficients of FOBD are computed according to a simple formula (7). It should be noted that in a real-time system, the approximation coefficients are calculated only once when the fractional order is changed.

Simultaneously, the computing of the step response, illustrated by histograms 13 and 14, is 100 times shorter using CFE than in case of the analogical computing using FOBD. This is caused by the smaller complexity of CFE approximation and shorter length of memory.

Finally, the differences in the performance of the STM32F7 processor with FPU enabled (hardware double precision) and disabled (software double precision) were tested. Particularly the mean values of $T_{df\ od\ F}$ and T_{Step} obtained for FOBD method were compared. The mean value of $T_{df\ od}$ is approximately 64.6 times shorter for FPU enabled (53.4 μs vs. 3.372 ms) while T_{Step} is approximately 5 times shorter (0.1307 ms vs. 0.66 ms). This means that the most significant benefits are obtained for complex numerical algorithms related to the FOBD approximation parameters. Also, the use of the STM32F7 FPU enables efficient, multiple determination of FOPID controller parameters, depending on the CFE and FOBD approximation parameter set.

As mentioned before, the clock frequency set for the STM32F767 processor was 96 MHz while the maximum frequency value given by the vendor is 216 MHz. Thus, the CFE or FOBD calculation durations can be further reduced. The unit experiments carried out at $f = 216$ MHz have enabled an approximately two-fold reduction in both durations $T_{df od F}$ (24.2 µs vs. 53.8 µs, FOBD) and T_{Step} (78.8 μs vs. 0.1307 ms, FOBD), which is a direct result of the difference in frequency between 96 MHz and 216 MHz.

7. Conclusions

The main conclusion from the research is that the elementary fractional element $s\gamma$ can be implemented at the considered microcontroller platform using typical, discrete approximations. The performance of approximation in the sense of the MSE and FIT cost functions is satisfying as well as duration of calculations.

From the first experiments a conclusion could be drawn that generally the use of FOBD allows obtaining more accurate approximation in the sense of examined cost functions in this paper. In the next experiments, data was collected showing that calculation of $T_{df\ od}$ is much slower for CFE than for FOBD approximation. However, computation of step response for CFE approximation is much faster than for FOBD. In the last experiment, it was proven that when FPU is enabled on the STM32F7, the calculations were much shorter, significantly for more complex numerical algorithms.

It is worth to add that the duration of calculations executed with the use of the microcontroller is much shorter than analogic calculations implemented at PLC (see [16]). Thus, it allows running a single fractional order PID algorithm operating at a sampling frequency of up to 10 kHz.

The proposed solution is planned to be used during implementation of the self-tuned FOPID controller on this platform. The results of time tests allow concluding that the proposed implementation can be employed in hard real-time control systems.

Acknowledgement

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Table 2. Values of the cost functions (12) and (13) for CFE approximation and different orders
Tabela 2. Wartości funkcji kosztów (12) i (13) dla aproksymacji CFE oraz różnych rzędów

γ	**–0.25**	**–0.50**	**–0.75**	**0.25**	**0.5**	**0.75**
MSE (12)	0.0067	0.0097	0.0047	0.0244	0.1117	0.1141
FIT (13)	1.0054	1.0462	1.0907	0.9281	0.9205	0.9064

Table 3. Values of the cost functions (12) and (13) for FOBD approximation and different orders
Tabela 3. Wartości funkcji kosztów (12) i (13) dla aproksymacji FOBD oraz różnych rzędów

γ	**–0.25**	**–0.50**	**–0.75**	**0.25**	**0.5**	**0.75**
MSE (12)	4.0130e-05	2.3069e-05	7.5951e-06	0.0029	0.1024	1.8874
FIT (13)	0.0305	0.0129	0.0056	0.2122	0.6061	2.0450

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Implementacja podstawowego elementu ułamkowego na mikrokontrolerze

Streszczenie: W pracy przedstawiono implementację podstawowego układu ułamkowego rzędu s^{γ}, $\gamma \in \mathbb{R}$ na platformie mikrokontrolera STM32. Implementacja wykorzystuje typowe aproksymacje CFE oraz FOBD. Dokładność aproksymacji oraz czas trwania obliczeń testowane są eksperymentalnie. Implementacja układów ułamkowych na mikrokontroler jest znana, jednak ich testy w czasie rzeczywistym nie były jak dotąd omawiane w literaturze. Wyniki wskazują, że obie metody można wdrożyć na rozważanej platformie. Aproksymacja FOBD jest dokładniejsza, z kolei CFE jest szybsza. Przedstawione rezultaty eksperymentów dowodzą, że procesor z rodziny STM32F7 może zostać wykorzystany do opracowania wbudowanych ułamkowych układów sterowania dla szerokiej klasy liniowych i nieliniowych układów dynamicznych. Zaprezentowane wyniki są istotne z punktu widzenia implementacji algorytmów ułamkowych w twardych systemach czasu rzeczywistego lub w systemach wbudowanych.

Słowa kluczowe: układy ułamkowe, mikrokontroler, STM32, FOBD, aproksymacja CFE

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