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A novel two-phase interleaved parallel bi-directional DC/DC converter

BAOGE ZHANG, DEYU HONG, TIANPENG WANG, ZHEN ZHANG, DONGHAO WANG

Lanzhou Jiaotong University
China
e-mail: 846691017@qq.com, zhangz0914@163.com

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Abstract: The energy storage system (ESS) is an important way to improve the power quality of renewable energy sources (such as solar energy and wind energy). A bi-directional DC/DC converter is an essential part of the ESS to achieve bi-directional energy transfer. According to the characteristics of the low-voltage gain and high-voltage stress of switches in the existing bi-directional DC/DC converter, this study proposes a novel two-phase interleaved parallel bi-directional DC/DC converter. The converter can effectively combine the advantages of a Z-source network and interleaved parallel structure. The working principle, the boost mode and buck mode of the converter are analyzed in detail. In addition, the voltage conversion ratios under the two modes are deduced. The control strategy of the two-phase interleaved parallel bi-directional DC/DC converter is introduced in detail. Furthermore, the main working waveforms of the system under each working mode are verified by building a simulation experiment model using MATLAB/Simulink. The simulation results show that the system has advantages of high-voltage gain, low-voltage stress of switches and automatic current sharing between inductors.

Key words: bi-directional DC/DC converter, energy storage system, interleaved parallel structure, voltage stress, Z-source network

1. Introduction

A renewable energy source (RES) (such as solar energy and wind energy) is going to be an inevitable trend in the future development of power systems [1, 2], but its output power is intermittent and random, which brings new challenges to the safe and stable operation of power systems [3]. Energy storage technology is an effective way to solve the power quality of RES power generation and a key technology to ensure the safe and stable operation of power grids [4].

The ESS is mainly composed of two parts: a bi-directional DC/DC converter and energy storage unit [5]. Among them, the bi-directional DC/DC converter can realize bi-directional energy transfer, which is an indispensable part of the ESS [6]. A cascaded bi-directional DC/DC converter can realize the purpose of high power and high current, but the cost should be considered [7]. Some researchers have studied the topology and control strategy of the interleaved parallel bi-directional DC/DC converter [8, 9]. Although the converter can provide a high current and high power, it has the disadvantages of a low-voltage gain and high-voltage stress of switching devices. A Z-source DC/DC converter has been presented, which has a higher voltage conversion ratio [10, 11]. Unfortunately, it has the disadvantage of high-voltage stress of switches. Interleaving and parallel technology have been reported, which shows that the technology is well applied in the fields of electric vehicles, micro-grid and distributed generation, and can improve the output power level, reduce the voltage and current ripple [12–14]. A pulse-width modulated (PWM) Z-source dc-dc converter has been suggested by [15, 16], the authors analyzed its steady-state operation process in a continuous conduction mode, especially to present the output voltage ripple analysis of the PWM Z-source dc-dc converter. It also presents the ac small-signal modeling of the power stage of the pulse width-modulated Z-source converter in a continuous conduction mode by the circuit-averaging technique. Finally, the validity is verified by building simulation and a physical model, they effectively prove the possibility of the combination of the Z-source converter and DC–DC converter, which are beneficial to the development of the DC–DC converter and energy storage technology plays here an important role.

A novel two-phase interleaved parallel bi-directional DC/DC converter is proposed to solve the problems of low-voltage gain, high-voltage stress and poor current sharing between inductors in the traditional interleaved parallel bi-directional DC/DC converter. This study analyzes an interleaved parallel bi-directional DC/DC converter based on the battery energy storage system (BESS) in detail. The specific arrangement is as follows: section 2 exhibits the topological structure and working principle of the proposed converter, section 3 displays the control strategy of the system, section 4 introduces the simulation results and analysis of the system. Finally, section 5 summarizes the article.

2. System configuration and working principle

2.1. System configuration

The traditional and the novel interleaved parallel bi-directional DC/DC converters are shown in Fig. 1 and Fig. 2, respectively. The differences between them are that the proposed topology adds the switching capacitor C_f, transforms the position of S_2, and adds a Z-source network and a diode D to prevent reverse current. In Fig. 2, U_b and U_d are, respectively, the voltages of the battery and the DC bus; The Z-source has the characteristics of single-stage voltage rise and fall, no dead zone and high reliability [17]. Meanwhile, due to the presence of C_f and the change of S_2 position, the voltage stress of switches in topology becomes low. Therefore, the proposed topology is not only provided with high-voltage gain, but also displays low-voltage stress of switches.

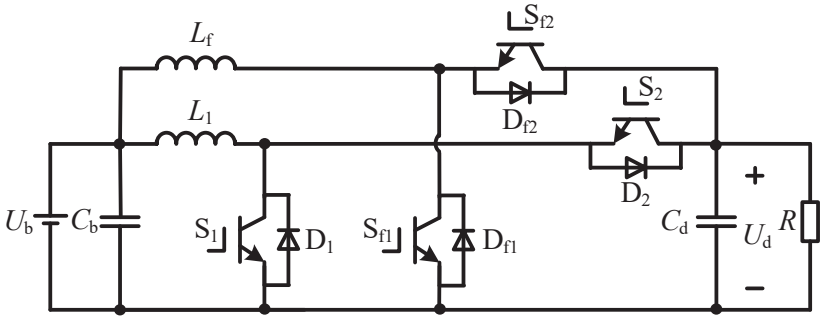

Fig. 1. Traditional two-phase interleaved parallel bi-directional DC/DC converter

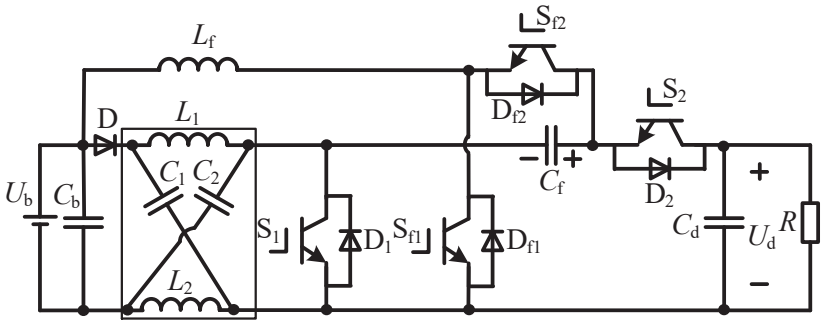

Fig. 2. Novel two-phase interleaved parallel bi-directional DC/DC converter

2.2. Working principle

The novel two-phase interleaved parallel bi-directional DC/DC converter has mainly two working modes: the boost mode and the buck mode.

Case 1. The boost mode

When the DC bus voltage of the ESS decreases, the bi-directional DC/DC converter starts to work in the boost mode, to stabilize the bus voltage at the DC side. Meanwhile, the antiparallel diodes S_2 and S_{f2} of S_2, S_{f2}, S_1 and S_{f1} work alternately. S_1 and S_{f1} are controlled by carrier phase-shift pulsewidth modulation (PWM). The duty cycle is d_1 and d_2, respectively, and $0.5 < d_1 = d_2 = d < 1$. It is advisable to define S_1, S_2, S_{f1} and S_{f2} as follows:

$$S = \begin{cases} 1 & \text{the switch turn on} \\ 0 & \text{the switch turn off} \end{cases}. \tag{1}$$

Therefore, the boost mode has three combinations in the switching cycle T_s, namely, $S_1S_2S_{f1}S_{f2} = 0010$, $S_1S_2S_{f1}S_{f2} = 1010$ and $S_1S_2S_{f1}S_{f2} = 1000$. The equivalent circuit diagram of each combination mode corresponding to the working state is shown in Fig. 3.

1. Working state 1 $[t_0-t_1]$: as shown in Fig. 3(a), $S_1S_2S_{f1}S_{f2} = 0010$. In the Z-source network, the inductors L_1 and L_2 start to discharge, and the diode D is turned on due to the reduction of cathode potential. Meanwhile, U_b, L_1 and L_2 will charge the capacitors C_1 and C_2 of

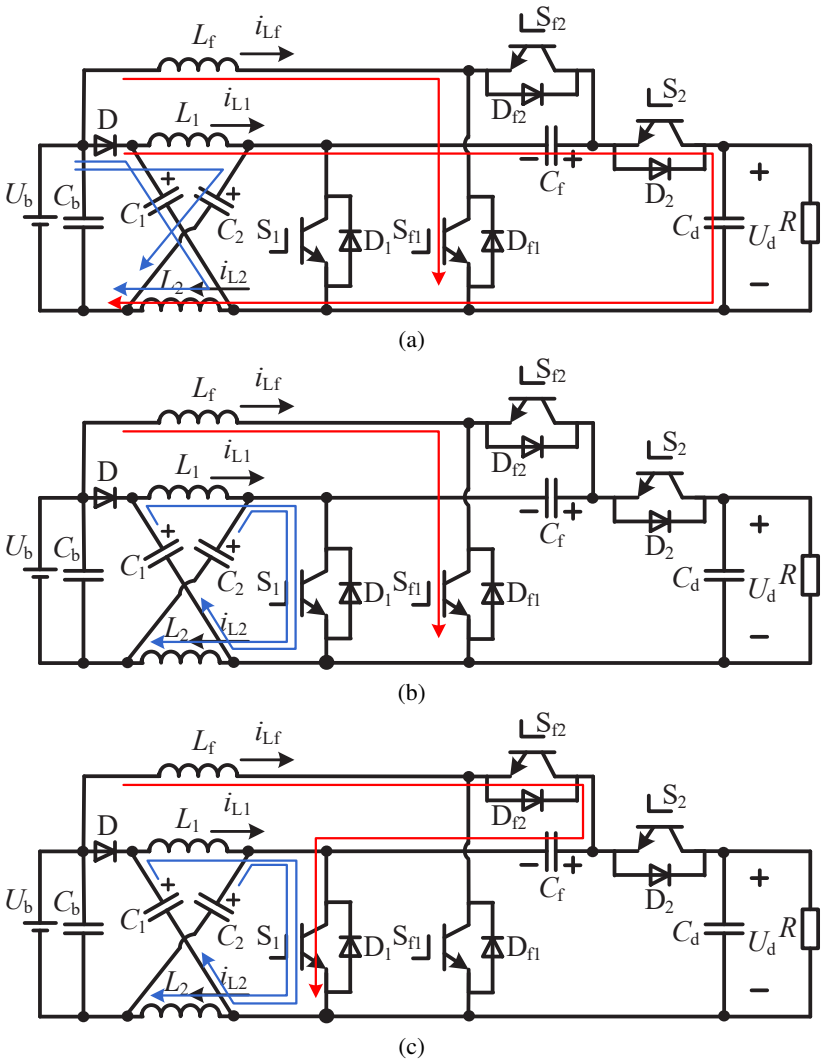

Fig. 3. Equivalent circuit diagram of working states in the boost mode: working state 1 (a); working state 2 (b); working state 3 (c)

the Z-source network, and U_b, L_1, L_2 and C_f will supply power to the DC bus voltage. In addition, U_b charges L_f, i_{Lf} increases, i_{L1}, i_{L2} and U_{Cf} decrease.

2. Working state 2 $[t_1 - t_2]$: as shown in Fig. 3(b), $S_1S_2S_{f1}S_{f2} = 1010$. The diode D is cut off due to the rise of cathode potential, the capacitor C_1 and C_2 start to discharge, and the inductors L_1 and L_2 start to store energy. Meanwhile, U_b charges L_f, i_{L1}, i_{L2} and i_{Lf} are all increasing, while C_f is in the state of voltage holding, and U_{Cf} remains constant.
3. Working state 3 $[t_2 - t_3]$: as shown in Fig. 3(c), $S_1S_2S_{f1}S_{f2} = 1000$. The diode D is cut off due to the increase of cathode potential, the capacitors C_1 and C_2 start to discharge, and

the inductors L_1 and L_2 start to store energy. Meanwhile, U_b and L_f charge C_f, i_{L1}, i_{L2} and U_{Cf} are increasing, while i_{Lf} is decreasing.

4. Working state 4 $[t_3 - t_4]$ is the same as working state 2.

According to the above analysis of each working state in the boost mode, the main waveforms of each working state in the switching cycle T_s can be obtained as shown in Fig. 4.

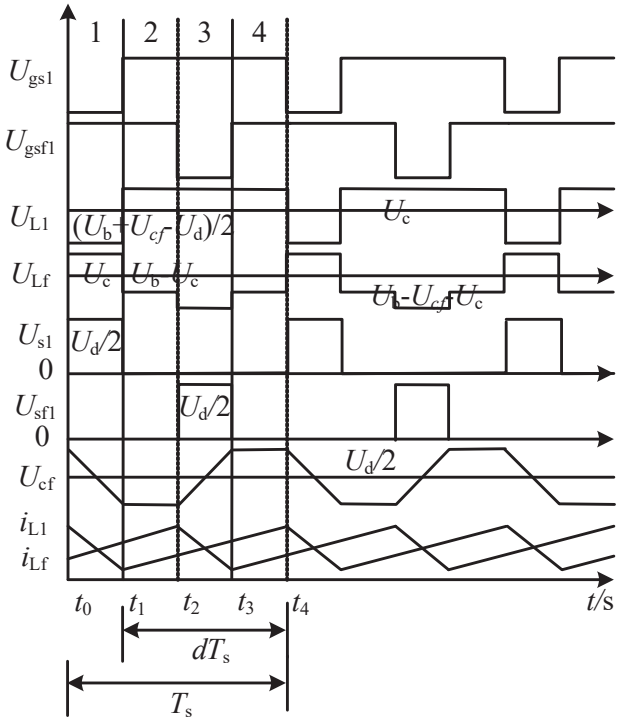

Fig. 4. Main waveforms of the boost mode under different working states

Case 2. The buck mode

When the DC bus voltage of the ESS increases, the bi-directional DC/DC converter starts to work in the buck mode, to stabilize the DC bus voltage. Meanwhile, the reverse parallel diodes D_1 and D_{f1} of S_1, S_{f1}, S_2 and S_{f2} work alternately. Similar to the boost mode, the duty cycle of S_2 and S_{f2} are d_1 and d_2, respectively, and $0 < d_1 = d_2 = d < 0.5$. In the switching cycle T_s, there are three combinations of the buck mode: $S_1S_2S_{f1}S_{f2} = 0100$, $S_1S_2S_{f1}S_{f2} = 0000$ and $S_1S_2S_{f1}S_{f2} = 0001$. The equivalent circuit diagram of each combination mode corresponding to the working state is shown in Fig. 5.

1. Working state 1 $[t_0 - t_1]$: as shown in Fig. 5(a), $S_1S_2S_{f1}S_{f2} = 0100$. U_b charges L_1, L_2, C_1, C_2 and C_f, and the inductance L_f charges the battery through the diode D_{f1}. i_{L1}, i_{L2} and U_{Cf} are increasing while i_{Lf} is decreasing.
2. Working state 2 $[t_1 - t_2]$: as shown in Fig. 5(b), $S_1S_2S_{f1}S_{f2} = 0000$. The inductors L_1 and L_2 charge the capacitors C_1 and C_2, respectively, through D_1, and the inductor L_f charge the battery through D_{f1}. Meanwhile, U_{Cf} keeps the voltage constant.

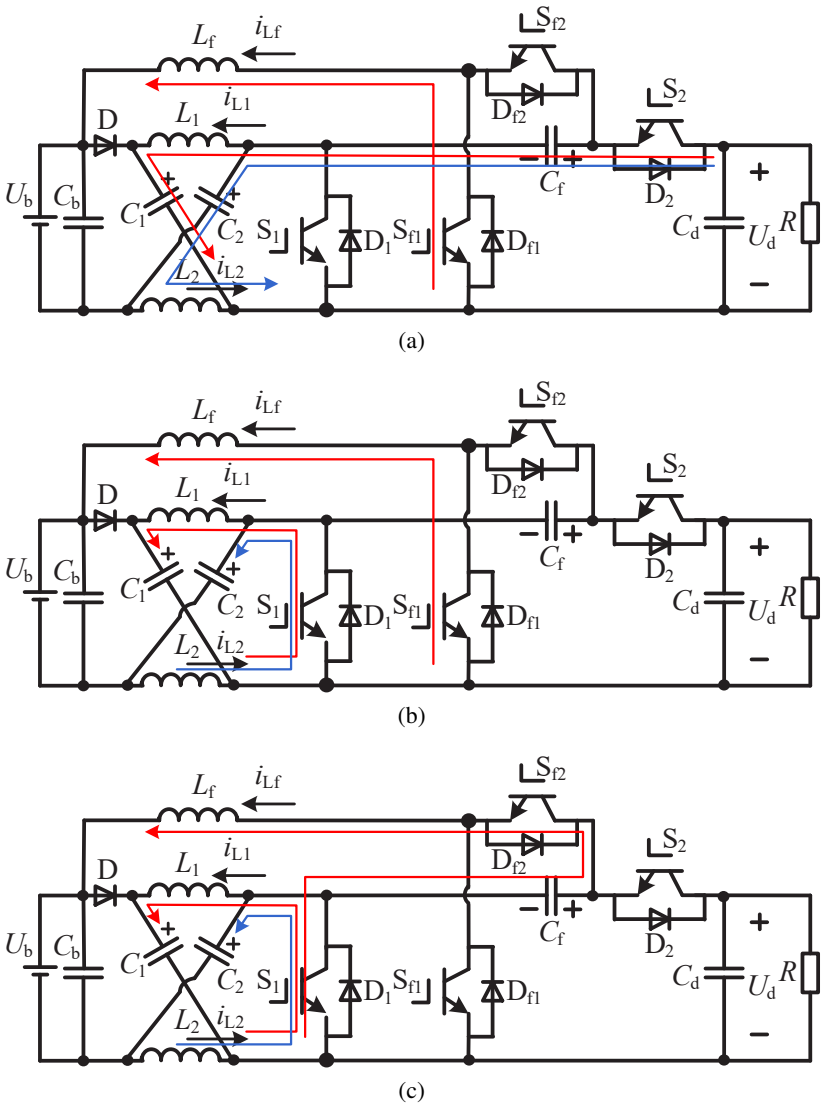

Fig. 5. Equivalent circuit diagram of working states in the buck mode: working state 1 (a); working state 2 (b); working state 3 (c)

3. Working state 3 $[t_2 - t_3]$: as shown in Fig. 5(c), $S_1S_2S_{f1}S_{f2} = 0001$. C_f charges L_f and the battery, and the inductance L_1 and L_2 are, respectively, charged by the capacitors C_1 and C_2 through D_1, and U_{Cf} decreases continuously.
4. Working state 4 $[t_3 - t_4]$ is the same as working state 2.

According to the above analysis of each working state in the buck mode, the main waveforms of each working state in the switching cycle T_s can be obtained as shown in Fig. 6.

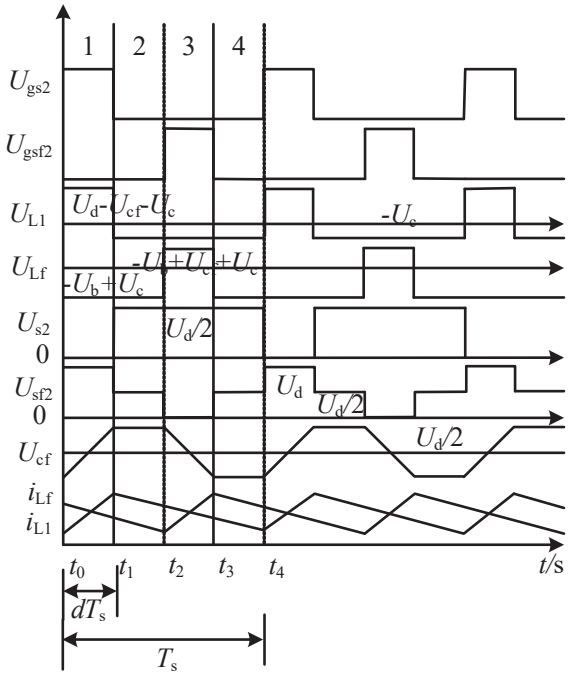

Fig. 6. Main waveforms of the buck mode under different working states

2.3. The performance analysis of a steady state

Case 1. The voltage gain

In order to facilitate the analysis and calculation, it is assumed that all components in the system are ideal, and the disturbances of current, voltage and duty cycles are ignored.

For the Z-source network, because of the symmetry of circuit structure and electrical characteristics [18], when S_1 is on, we can get as follows:

$$\begin{cases} U_L = U_{L1} = U_{L2} \\ U_C = U_{C1} = U_{C2} \end{cases}, \tag{2}$$

where U_{L1} is the voltage of L_1, and U_{L2} is the voltage of L_2. U_{C1} is the voltage of C_1, and U_{C2} is the voltage of C_2.

When the system works in boost mode, the state equations of each working state in the switching period T_s are as follows:

Working state 1:

$$\begin{pmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{Lf}}{dt} \end{pmatrix} = \begin{pmatrix} 0 & 0 \\ 0 & -\frac{1}{L_f} \end{pmatrix} \begin{pmatrix} U_c \\ U_L \end{pmatrix} + \begin{pmatrix} \frac{1}{2L_1} & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} U_{cf} \\ 0 \end{pmatrix} + \begin{pmatrix} \frac{1}{2L_1} & -\frac{1}{2L_1} \\ \frac{1}{L_f} & 0 \end{pmatrix} \begin{pmatrix} U_b \\ U_d \end{pmatrix}, \tag{3}$$

where U_{cf} is the voltage of C_f.

Working state 2 and working state 4:

$$\begin{pmatrix} \dfrac{\mathrm{d}i_{\mathrm{L1}}}{\mathrm{d}t} \\ \dfrac{\mathrm{d}i_{\mathrm{Lf}}}{\mathrm{d}t} \end{pmatrix} = \begin{pmatrix} \dfrac{1}{L_1} & 0 \\ 0 & -\dfrac{1}{L_{\mathrm{f}}} \end{pmatrix} \begin{pmatrix} U_{\mathrm{c}} \\ U_{\mathrm{L}} \end{pmatrix} + \begin{pmatrix} 0 & 0 \\ \dfrac{1}{L_{\mathrm{f}}} & 0 \end{pmatrix} \begin{pmatrix} U_{\mathrm{b}} \\ 0 \end{pmatrix}. \tag{4}$$

Working state 3:

$$\begin{pmatrix} \dfrac{\mathrm{d}i_{\mathrm{L1}}}{\mathrm{d}t} \\ \dfrac{\mathrm{d}i_{\mathrm{Lf}}}{\mathrm{d}t} \end{pmatrix} = \begin{pmatrix} \dfrac{1}{L_1} & 0 \\ 0 & -\dfrac{1}{L_{\mathrm{f}}} \end{pmatrix} \begin{pmatrix} U_{\mathrm{c}} \\ U_{\mathrm{L}} \end{pmatrix} + \begin{pmatrix} 0 & 0 \\ -\dfrac{1}{L_{\mathrm{f}}} & \dfrac{1}{L_{\mathrm{f}}} \end{pmatrix} \begin{pmatrix} U_{\mathrm{cf}} \\ U_{\mathrm{b}} \end{pmatrix}. \tag{5}$$

In a steady state, according to the principle of inductance voltage-second (V-S) balance and the principle of capacitance ampere-second (A-S) balance, when combining Formula (2)–Formula (5), we can get as follows:

$$\begin{cases} U_{\mathrm{cf}} = \dfrac{1}{2} U_{\mathrm{d}} \\ \dfrac{U_{\mathrm{d}}}{U_{\mathrm{b}}} = \dfrac{2(4d^2 - 6d)}{(1-d)\ 3(1-2d)} \end{cases}. \tag{6}$$

Similarly, when the system works in the buck mode, we can get as follows:

$$\begin{cases} U_{\mathrm{cf}} = \dfrac{1}{2} U_{\mathrm{d}} \\ \dfrac{U_{\mathrm{b}}}{U_{\mathrm{d}}} = \dfrac{3}{2} d - \dfrac{1}{2} \end{cases}. \tag{7}$$

It can be seen from Formula (6)–Formula (7) that the voltage gain of the proposed converter working in the boost and buck modes is more than doubled compared with the traditional two-phase interleaved parallel bi-directional DC/DC converter, and it is also improved compared with the existing improved interleaved parallel bi-directional DC/DC converter.

Case 2. The voltage stress of switches

It can be seen from Fig. 4 that when the system operates in the boost mode, the maximum voltage stress borne by the antiparallel diode $\mathrm{D_{f2}}$ of $\mathrm{S_{f2}}$ in the switching cycle T_{s} is U_{d}, while the maximum voltage stress borne by the antiparallel diodes $\mathrm{D_2}$ of $\mathrm{S_2}$, $\mathrm{S_{f1}}$ and $\mathrm{S_1}$ in the switching cycle T_{s} is $U_{\mathrm{d}}/2$. It can be seen from Fig. 6 that when the system operates in the buck mode, the maximum voltage stress of S_{f2} in the switching cycle T_{s} is U_{d}, while that of $\mathrm{D_1}$, $\mathrm{D_{f1}}$ and $\mathrm{S_2}$ in the switching cycle T_{s} is $U_{\mathrm{d}}/2$. Compared with the current interleaved and parallel bi-directional DC/DC converter, the voltage stress of the switches of the novel interleaved and parallel bidirectional DC/DC converter is reduced.

Case 3. Automatic current sharing principle of L_1 and L_{f1} in a steady state

When the system works in the boost mode, the voltage of C_{f} remains unchanged in working states 2 and 4. The discharge current of C_{f} is the discharge current of the inductance L_1 in working state 1, and the charging current of C_{f} is the charging current of the inductance L_{f} in working

state 3. According to the A-S balance principle of C_f, i_{L1} and i_{Lf} can realize automatic current sharing. Similarly, i_{L1} and i_{Lf} can realize automatic current sharing in the buck mode.

Case 4. Performance comparison of different converters

Taking the boost mode as an example, the voltage gain and switching device voltage stress of the traditional interleaved bidirectional DC/DC converter [8] and the proposed two-phase interleaved bidirectional DC/DC converter are compared and analyzed, as shown in Table 1.

Table 1. Comparison of performance of different converters

Parameters	**Traditional two phase interleaved parallel DC/DC converter**	**The proposed two-phase interleaved bidirectional DC/DC converter**
Voltage gain	$1/(1-d)$	$\dfrac{2(4d^2-6d)}{(1-d)3(1-2d)}$
Voltage stress of switch tubes	U_d	$U_d/2$

It can be seen from Table 1 that the voltage gain of the novel two-phase interleaved bidirectional DC/DC converter working in the boost mode is more than double that of the traditional two-phase interleaved bidirectional DC/DC converter. Meanwhile, the voltage stress of switching devices of the novel two-phase interleaved bidirectional DC/DC converter working in the boost mode is reduced by half compared with the traditional two-phase interleaved bidirectional DC/DC converter.

3. Control strategy

In the ESS, the important medium of energy exchange between the energy storage unit and DC bus is an interleaved parallel bi-directional DC/DC converter, which is to control an interleaved parallel bi-directional DC/DC converter to charge and discharge the battery. The novel two-phase interleaved parallel bidirectional DC/DC converter mainly works in the boost and buck modes. In order to ensure its working characteristics, the switches adopt carrier phase-shifting control. When the system works in the boost mode, the trigger signals of S_1 and S_{f1} differ by 180°, and the trigger signals of S_2 and S_{f2} differ by 180° in the same way as those of the buck mode.

The control block diagram of the novel interleaved parallel bi-directional DC/DC converter is shown in Fig. 7. It can be seen from Fig. 7 that the control block diagram of the system is composed of two parts: the logic judgment unit and signal generation unit. When the voltage of DC bus decreases, the system starts to work in the boost mode. In this system, the DC bus voltage is used as the control signal, the steady-state error of the DC bus voltage is utilized, the modulation wave signal of a trigger pulse is generated by the PI controller and limiting link, and then the contact signal of S_1 and S_{f1} is obtained by comparing with the carrier signal of 180° phase difference between the two channels, to realize the purpose of stabilizing the DC bus voltage.

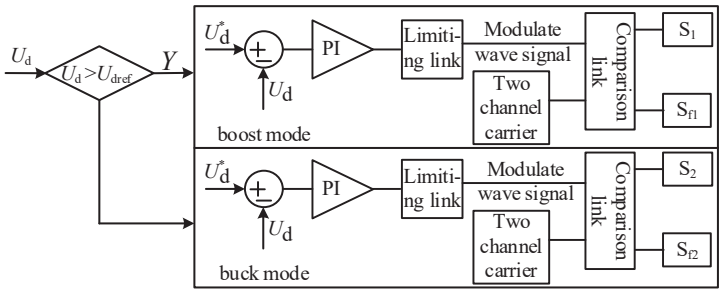

Fig. 7. Control block diagram of the novel interleaved parallel bidirectional DC/DC converter

4. Simulation results and discussion

In order to verify the effectiveness of the proposed converter, Matlab/Simulink is utilized for simulation verification, and the main parameters of the simulation experiment are shown in Table 2.

Table 2. Main simulation parameters of the system

Parameter name	Symbol	Value	Unit
Battery voltage	U_b	7.5	V
DC bus voltage	U_d	60	V
Inductance 1	L_1	2.55×10^{-4}	H
Inductance 2	L_2	2.55×10^{-4}	H
Inductance 3	L_f	2.55×10^{-4}	H
Switched capacitor	C_f	2.24×10^{-5}	F
Z source network capacitance	C_1, C_2	2.25×10^{-5}	F

The main working waveforms of the novel interleaved parallel bi-directional DC/DC converter of the ESS, working in the boost mode and buck mode, are shown in Fig. 8 and Fig. 9, respectively. It can be seen from Fig. 8(a) that in the switching cycle T_s, the maximum voltage stress of S_1 and S_{f1} is also 30 V, only half of the voltage of the DC bus, so the voltage stress of switches in this system is greatly reduced. Fig. 8(b) shows, that the steady-state value of the switching capacitor C_f is about 30 V, and the charge and discharge of the switching capacitor C_f are balanced (the maximum voltage is about 46.3 V, and the minimum voltage is about 11.1 V.) At the same time, according to Fig. 8(c), i_{L1} and i_{Lf} are basically of the same size (current ripple rate is about 9.11%.) Therefore, i_{L1} and i_{Lf} realize automatic current sharing. As shown in Fig. 8(d), the voltage of the DC bus U_d is about 60 V, and the voltage ripple rate is less than 0.11%. The interleaved parallel bi-directional DC/DC converter of the ESS realizes the function of high-voltage gain, which is consistent with the theoretical analysis. It can be seen from Fig. 9(a) that in the switching cycle T_s, the maximum voltage stress of S_2 is also 30 V, only half of the voltage of the DC bus, while the maximum voltage stress of S_{f2} is 60 V, so the voltage stress of switches in this system is greatly

reduced. As shown in Fig. 9(b), the steady-state value of the switching capacitor C_f is about 30 V, and the charge and discharge of the switching capacitor C_f are balanced (the maximum voltage is about 33.6 V, and the minimum voltage is about 26.1 V). Meanwhile, according to Fig. 9(c), i_{L1} and i_{Lf} are basically of the same size. Therefore, i_{L1} and i_{Lf} realize automatic current sharing. As seen in Fig. 9(d), the output voltage U_b at the low-voltage side is about 7.5 V, and the voltage ripple rate is less than 0.14%. The interleaved parallel bi-directional DC/DC converter of the ESS realizes the function of high-voltage gain, which is consistent with the theoretical analysis.

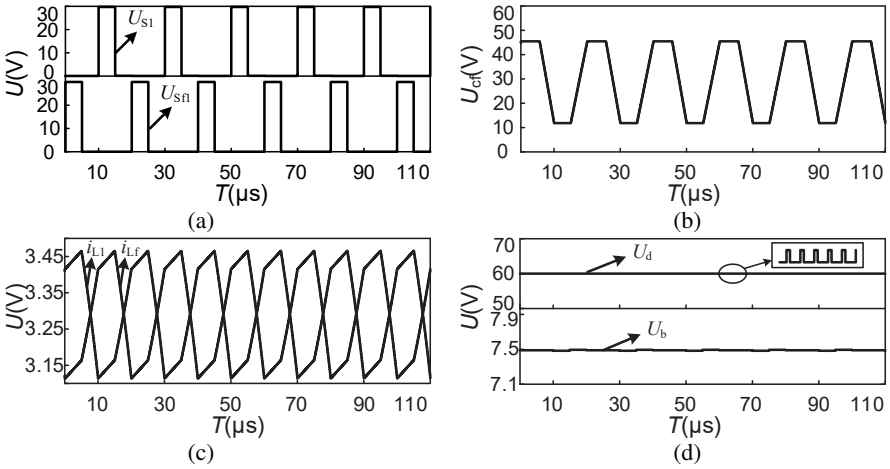

Fig. 8. Main waveforms of the circuit in the boost mode: the voltage stress waveform of switches (a); waveform of switching capacitor voltage (b); current waveform of inductance L_1 and L_f (c); waveform of input and output voltage (d)

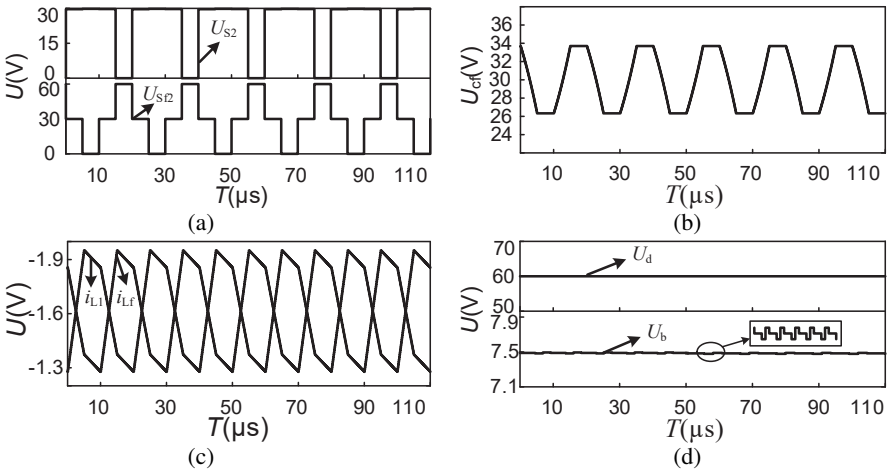

Fig. 9. Main waveforms of the circuit in the buck mode: the voltage stress waveform of switches (a); waveform of switching capacitor voltage (b); current waveform of inductance L_1 and L_f (c); waveform of input and output voltage (d)

5. Conclusion

A two-phase interleaved parallel bi-directional DC/DC converter is proposed in this study. According to the theoretical analysis and simulation, the system has the following advantages. Firstly, high-voltage gain and small voltage ripple. Compared with the traditional two-phase interleaved parallel bi-directional DC/DC converter [8], the voltage gain of this topology is more than double. In addition, compared with the existing mentioned interleaved parallel bi-directional DC/DC converter [19], it is also improved. Furthermore, the system has low-voltage stress, which is helpful to reduce the switching loss. Then, the balance of the inductance current of each phase can be realized by switching the capacitor C_f. Finally, the system can provide a large current, which contributes to reducing the size of the battery, and improves the economy of the ESS.

The next plan is to perform experimental tests, build a prototype, and apply it to the energy storage system, and evaluate some performance indicators.

Acknowledgements

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