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Input signal conditioning circuits for precision SAR analog to digital converters

Abstract

The paper presents a review of the known signal conditioning circuits that may be used as a front-end of precision high-resolution successive-approximation register (SAR) analog to digital converters (ADC). The review was created while searching for the optimal signal conditioning circuit to be used with a high-resolution SAR ADC applied in a precise sampler for voltage, power, energy and impedance metrology applications.

Keywords: SAR analog to digital converter, signal conditioning, amplifier.

1. Introduction

Availability of the high-resolution successive approximation register analog to digital converters opens up the possibility of their use in high-precision measuring instruments like precise samplers, digital multimeters, harmonic analyzers and many others. Despite the high resolution, achieving 24 bits, there is also a dramatic improvement in their dynamic range, which exceeds 100 dB at 1.5 MSa/s output data rate and achieves 145 dB at 30.5 Sa/s [1]. Their DC properties are also impressive.

Unfortunately, the progress in the development of the high-resolution SAR ADCs is not accompanied with the simultaneous development of monolithic integrated circuits, which could serve as SAR ADCs input signal conditioning circuits. Therefore these circuits are designed using discrete components like operational amplifiers, differential amplifiers and set of precise resistors [2]. This paper presents a review of the known signal conditioning circuits that may be used as the front-end of the precision high-resolution SAR ADC. The review was made while searching for the optimal signal conditioning circuit to be used with a high-resolution SAR ADC applied in precise sampler for voltage, power, energy and impedance metrology applications.

2. Classification of the SAR ADC input signal conditioning circuits

The SAR ADC signal conditioning circuit used in a precise sampler or a harmonic analyzer usually has to convert the input measured bipolar AC or DC voltage into one unipolar voltage or two unipolar voltages as shown in Fig. 1.

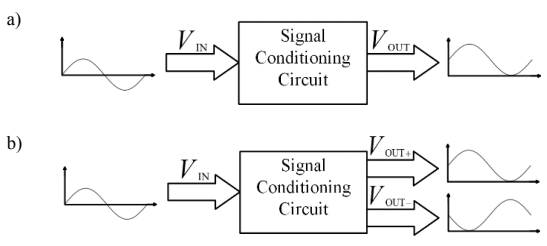

Fig. 1. Pictorial representation of the conversion realized by SAR ADC input signal conditioning circuit: a) for the SAR ADC with pseudo-differential unipolar input, b) for the SAR ADC with differential unipolar input

The circuit shown in Fig. 1a converts the input bipolar voltage V_{IN} (for example sinusoidal) into a unipolar voltage of the same shape, of the peak-to-peak voltage V_{OUT} acceptable by the pseudo-differential unipolar input of the SAR ADC. Voltage V_{OUT} may be called *asymmetrical*.

The circuit presented in Fig. 1b converts the input bipolar voltage V_{IN} (for example sinusoidal) into two unipolar, out-of-phase voltages V_{OUT+} and V_{OUT-} of the same shape and of the peak-to-peak voltages acceptable by the differential unipolar input of the SAR ADC. Voltages V_{OUT+} and V_{OUT-} may be treated as one *differential* input signal of the SAR ADC.

The review presented in the following sections will be divided into two parts: signal conditioning circuits for pseudo-differential unipolar input SAR ADCs, and signal conditioning circuits for differential unipolar input SAR ADCs.

3. Signal conditioning circuits for SAR ADCs with a pseudo-differential unipolar input

In the case of the pseudo-differential unipolar input SAR ADCs, the signal conditioning circuit has to shift and properly scale the input voltage. Examples of such a circuit are shown in Fig. 2. In both of the circuits shown in Fig. 2 the operational amplifiers operate in non-inverting configuration. The output voltage of the circuit shown in Fig. 2a is equal to:

$$V_{OUT}=\left(\frac{R_1\cdot V_{IN}}{R_1+R_2}+\frac{R_2\cdot V_{REF}}{R_1+R_2}\right)\cdot\left(1+\frac{R_4}{R_3}\right), \tag{1}$$

where V_{REF} is a DC reference voltage used to shift the output voltage to the middle of the SAR ADC input range.

The main drawback of the circuit of Fig. 2a is the low impedance of both V_{IN} and V_{REF} inputs, which results in loading the source of the input signal and the source of the reference voltage. The low impedance of these both inputs makes the output voltage sensitive to the internal impedances of the both sources. It is possible to use a precision voltage follower (buffer), but the design of such a buffer is not trivial [3].

Another disadvantage of the circuit of Fig. 2a is the effect of the common mode input voltage of the operational amplifier on the output voltage due to its limited common-mode rejection ratio (CMRR). The first drawback is partially overcome in the circuit shown in Fig. 2b. Here the input voltage is applied directly to the non-inverting input of the operational amplifier, but the detrimental effect of the limited CMRR and the internal impedance of the DC reference source remain. The formula for the output voltage of the circuit of Fig. 2b is simpler in comparison with that of Fig. 2a:

$$V_{OUT}=\left(1+\frac{R_2}{R_1}\right)\cdot V_{IN}-\frac{R_2}{R_1}\cdot V_{REF}, \tag{2}$$

and greatly simplify the design of the circuit, as the both resistance ratios in Eq. (2) can be realized with two resistive dividers. Unfortunately, the gain of the circuit shown in Fig. 2a is higher than 1, i.e. the higher input voltage has to be divided prior to its application to the input of the noninverting input.

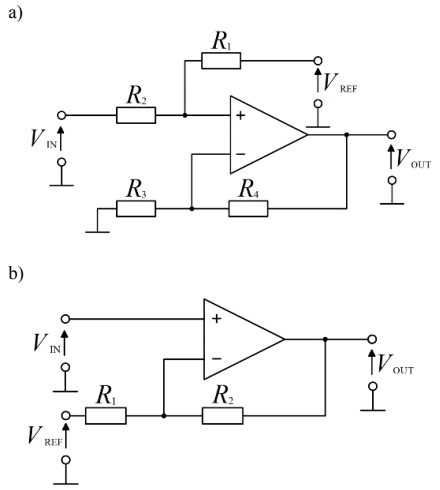

Fig. 2. Signal conditioning circuits for pseudo-differential unipolar input SAR ADCs with operational amplifier in non- inverting configuration

To minimize the effect of the limited CMRR, an operational amplifier can be used in inverting configuration, like in the circuit shown in Fig. 3. The output voltage of the circuit of Fig. 3a is equal to:

$$V_{\mathrm{OUT}} = -\frac{R_2}{R_1} \cdot V_{\mathrm{IN}} - \frac{R_2}{R_3} \cdot V_{\mathrm{REF}} \tag{3}$$

The output voltage of the circuit of Fig. 3b is given by:

$$V_{\mathrm{OUT}} = -\frac{R_2}{R_1} \cdot V_{\mathrm{IN}} + \frac{R_4}{R_3 + R_4} \cdot \left(1 + \frac{R_2}{R_1}\right) \cdot V_{\mathrm{REF}}, \tag{4}$$

i.e. is more complex than that of Fig. 3a. The both circuits shown in Fig. 3 have the same disadvantage, like the circuit of Fig. 2a, namely the low impedance of the both inputs. Moreover, the R_3 resistor increases the noise gain of the circuit and sensitivity to the drift of the input offset voltage of the operational amplifier.

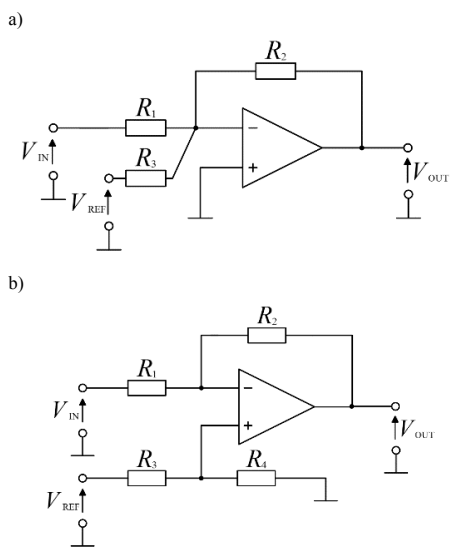

Fig. 3. Signal conditioning circuits for pseudo-differential unipolar input SAR ADCs with operational amplifier in inverting configuration

4. Signal conditioning circuits for SAR ADCs with differential unipolar input

It is well known, that in comparison to the asymmetrical signaling, the differential one provides better rejection of the unwanted common mode signals, coming e.g. from external interference electromagnetic fields, or adjacent wires or printed circuit board traces transmitting digital signal. But the reduction of the common mode noise voltage is at the cost of the complexity of the circuit. Two exemplary signal conditioning circuits for differential unipolar input SAR ADC are presented in Fig. 4.

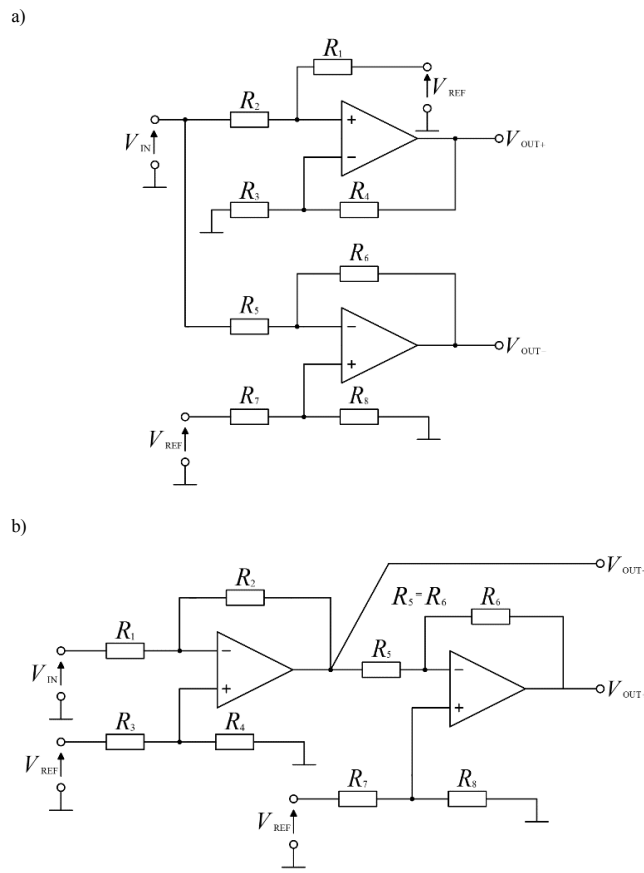

Fig. 4. Signal conditioning circuits for differential unipolar input SAR ADCs

The main drawback of the circuit shown in Fig. 4a is the low impedance of all the inputs and the resulting sensitivity to the internal impedances of the input and DC reference sources. Another drawback is the influence of the common mode input voltage of the upper operational amplifier. Due to the use of operational amplifiers in the inverting configuration, this detrimental effect is reduced in the circuit presented in Fig. 4b. But the input impedance of this circuit is low, like the one presented in Fig. 4a.

Two another signal conditioning circuits are presented in Fig. 5, but they were not considered because of their limitations. One of them is the design using a fully differential amplifier [2], the another one is the transformer-coupled circuit. The application of the last one is limited to conditioning AC voltages only.

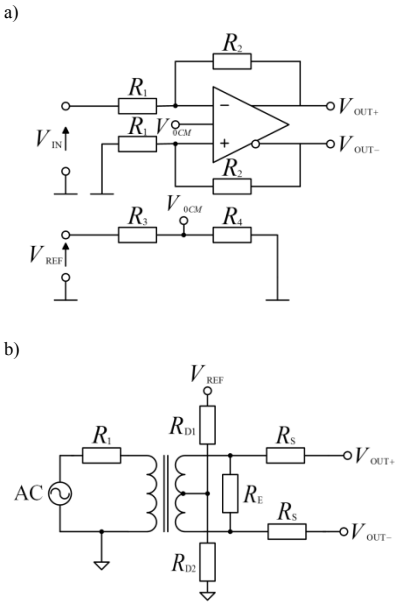

Fig. 5. Another signal conditioning circuits for differential unipolar input SAR ADCs: with a differential amplifier, b) with transformer

5. Summary

Selected signal conditioning circuits that may be used as front-end of a precise high-resolution SAR ADC were presented in this paper and their properties were briefly discussed. The search for the optimal circuit will be continued. The chosen circuit will be used in a precise sampler for voltage, power, energy and impedance metrology applications.

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