Dynamic Comparator Design in 28 nm CMOS

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***Abstract*—The paper presents a dynamic comparator design in 28 nm CMOS process. The proposed comparator is a main block of an asynchronous analog-to-digital converter used in a multichannel integrated circuit dedicated for X-ray imaging systems. We provide comparator's main parameters analysis, i.e. voltage offsets, power consumption, response delay, and input-referred noise in terms of its dimensioning and biasing. The final circuit occupies 5×5 μm^2 of area, consumes 17.1 fJ for single comparison with 250 ps of propagation delay, and allows to work with 4 GHz clock signal.**

***Index Terms*—dynamic comparator, SAR, ADC, X-ray imaging, CMOS, sensor, energy measurement.**

I. Introduction

THE trend in the design of modern ionizing radiation detectors aims at precise measurement of each incoming photon energy [1]–[3], which may be realized in Single Photon Counting (SPC) systems [4]–[6]. The SPC systems (see Fig. 1) are usually comprised of a Charge Sensitive Amplifier (CSA), a comparator, and a digital counter. However, considering the SPC operation mode and necessity of energy measurement of each incoming photon, it can be seen that the integrated circuit needs to be equipped with an analog-to-digital converter (ADC), enabling precise differentiation of the energy levels. Furthermore, as ionizing detectors dedicated to medical imaging often need to be composed of hundreds of thousands of pixels shaped recording channels of area as low as 50×50 μm^2 and ability of operating with high photon flux in the order of 1 Gcps/mm^2, each single recording channel needs to be equipped with an ADC of very low area occupation and processing input signals of about 2.5 MHz frequency. Therefore, to further ease the required single channel parameters, the 28 nm CMOS process is proposed as the feature-size reduction facilitates both the implementation of larger system functionality and its high performance.

Having in mind that ADCs power, area, and speed efficiency are the prime of concern, the most common choice is to use the successive approximation ADC. However, to improve the overall system performance in terms of single pixel area occupation, power consumption, and energy measurement resolution, we propose to use an 8-bit ADC of a hybrid architecture. The concept is to compose the ADC of two main consecutive blocks, i.e. 5-bit SAR-based ADC followed by the 3-bit VCO-based ADC. We assume the single ADC sampling frequency of 10 MHz, and that each SAR-based and VCO-based ADCs has 50 ns to process 5 and 3 bits, respectively.

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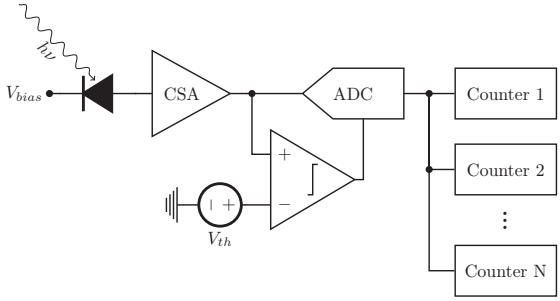

Fig. 1. Simplified readout channel architecture.

Therefore, the average time for a single comparator decision is 10 ns reduced by the reset time.

Considering the SAR-based ADC parameters, it can be seen that these are strongly related to the comparator's parameters, i.e. both static and dynamic power consumption, operation speed, and area occupation. Therefore, in this paper we provide a detailed analysis of the dynamic comparator implemented in 28 nm CMOS process. The comparator is assumed to work with 1 V supply voltage, its input voltage range is 1 V, while the maximum delay should be less than 10 ns.

The article is organized as follows: Section II provides the proposed comparator overview, Section III shows detailed analysis of particular dynamic comparator's parameters, and Section IV contains conclusions.

II. Comparator Overview

There are various comparator designs, differing in their architecture and parameters [7]. In this paper we consider only dynamic comparators because their operation may be controlled by the recording channels internal signal, thus the comparator consumes power only when it is informed the input signal is ready to be compared with the referenced one [8]–[10]. We decided to design dynamic comparator based on [8], as their main parameters are well-balanced in comparison to other works.

The comparator schematic idea is shown in Fig. 2. It is built of two main stages, i.e. the first stage is based on the dynamic differential amplifier, while the second stage consists of the dynamic differential amplifier equipped with positive feedback for rail-to-rail output signal generation. This type of architecture allows to separate the input signal amplification from the latching operation, thus enabling individual block optimization. Additionally, the two stage architecture minimizes kick-back noise effect. The comparator operates in two modes, i.e. whenever CLK signal is low, it is in the RESET mode,

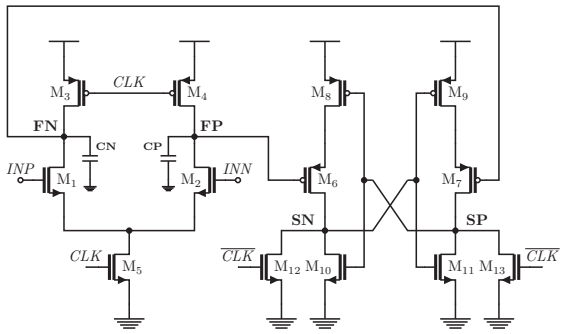

Fig. 2. Two-stage dynamic comparator.

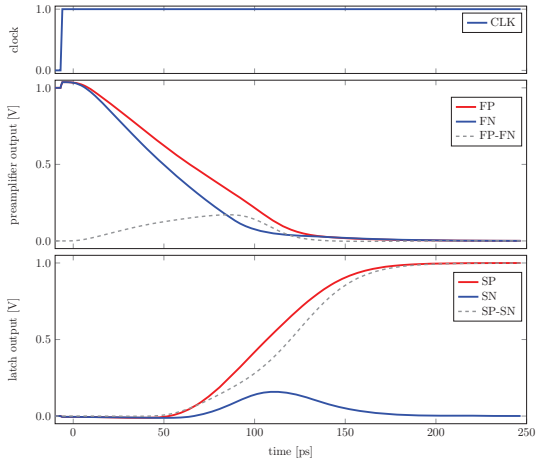

Fig. 3. Node voltages during a comparison phase at input voltage of 15 mV.

otherwise it is in the ACTIVE mode. If the comparator is in the RESET mode, nodes FP, FN are pre-charged to the high supply voltage, while the output nodes SP, SN are set to logic low – in that mode the comparator consumes static power only resulting from transistors leakage currents. Capacitors C_P, C_N, representing FP, FN nodes parasitic capacitances, are therefore charged to the supply voltage. Whenever the CLK signal is set high, the comparator is introduced to the ACTIVE mode, meaning that the comparator starts to compare its input signals. In that mode, transistors $M_{3,4}$ and $M_{12,13}$ are switched off, while M_5 is switched on. The C_P, C_N capacitors are then being discharged by M_5 transistor defined current what results in FP−FN differential voltage build-up – the second-stage common mode input voltage starts to decrease. When the input voltage of the second stage is lower than the $M_{6,7}$ threshold voltage, the second stage starts, finally providing output rail-to-rail voltage, thanks to the positive feedback. Particular node voltages may be observed in Fig. 3.

Power consumed by the comparator depends mainly on the first stage, where C_P, C_N capacitors need to be charged and discharged in RESET and ACTIVE modes, respectively. This may be defined as:

$$E = 2 \cdot C_{P\ (N)} \cdot V_{DD}^2 \tag{1}$$

Assuming both $M_{1,2}$ transistors currents are constant and C_P, C_N capacitors are equal, the comparator differential output voltage VF may be given as:

$$\begin{aligned} V_F &= V_{FP} - V_{FN} \\ &= (I_{S2} - I_{S1}) \cdot C_P \end{aligned} \tag{2}$$

The comparator core, shown in Fig. 2, was further improved by [9] and [11]. One of its modifications was power consumption reduction by leakage currents minimization. This was achieved by transistors M_5 and $M_{6\text{-}9}$ replacement with high threshold voltage devices. To maintain the speed of comparison, remaining transistors were replaced with low threshold voltage devices. Another [9] aspect was to apply a logic gate connected to the latch outputs to provide ready-indication signal for an asynchronous logic. This approach allowed to give the comparator more time for taking a decision whenever the input voltage difference is low, further minimizing both power consumption and metastability effect. Also [11] proposed to minimize power consumption by modifying M_5 transistor operation. Namely, an additional switch with parallel capacitance was added to the M_5 transistor source, which resulted in both increasing voltage gain and lowering the noise of the comparator input stage.

III. Comparator Design

The comparator is assumed to be a part of a project for precise ionization energy measurement and will be realized in 28 nm CMOS process. Since the comparator is based on two consecutive stages, we hereafter analyze them individually to optimize the design for low power consumption, small area occupation, and short decision time. All the following analyses are based on schematic-level simulations.

A. First Stage

It is well known that the first block of signal conditioning chain often determines main system parameters. Therefore, we analyzed in detail how the voltage gain, input-referred noise, voltage offset, delay, and power consumption depend on the first stage transistors parameters (see Fig. 4). These were verified when the differential output voltage of the latch reached 2 mV, which was assumed as the moment of taking over by the second stage, applying differential input voltage of 1 mV. The first stage is responsible for input signal difference amplification, hence its voltage gain is the first considered parameter. Importantly, higher input stage voltage gain suppresses undesired effects of the second stage, like e.g. noise, offset or kick-back. It can be seen that, for constant W/L ratio, the maximum gain is reached at five times the minimum channel length and equals about 12 (see Fig. 4 and Fig. 6). A natural consequence of increasing input transistors dimensions is higher C_P (C_N) capacitance, resulting in higher energy consumption. However, the input-referred noise and voltage offsets are lower.

We also checked how the common mode input voltage influences main comparator's parameters (see Fig. 5). Here, the input pair transistors' threshold voltage is around 500 mV. As shown in Fig. 5, working below the threshold guarantees high gain and low noise, but at the expense of extended propagation delay, which leads to increased probability of metastability-induced error as well.

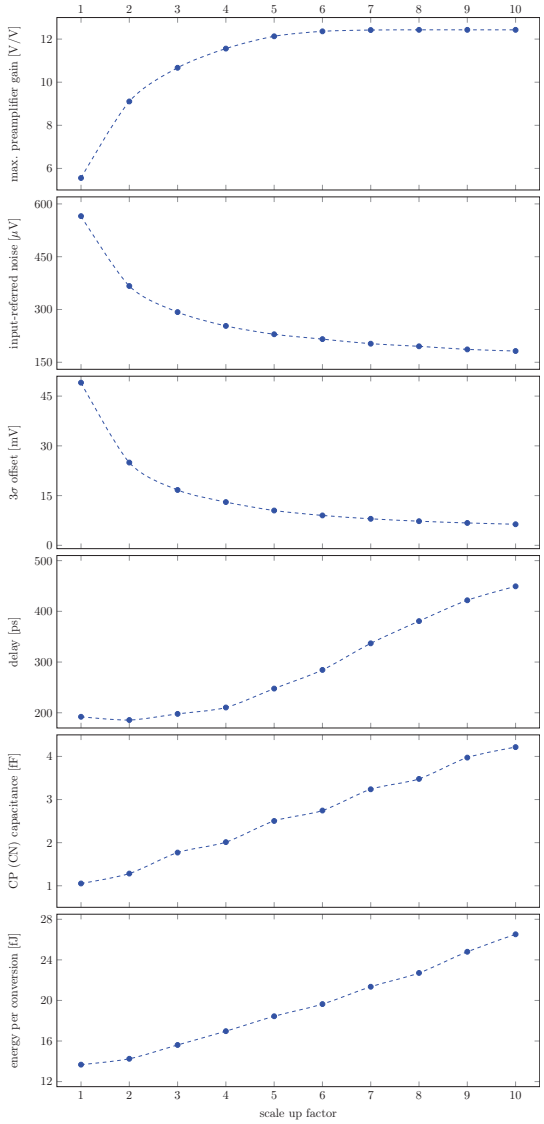

Fig. 4. Circuit parameters as a function of input pair scaled size. Initial dimension is 1μm/30nm.

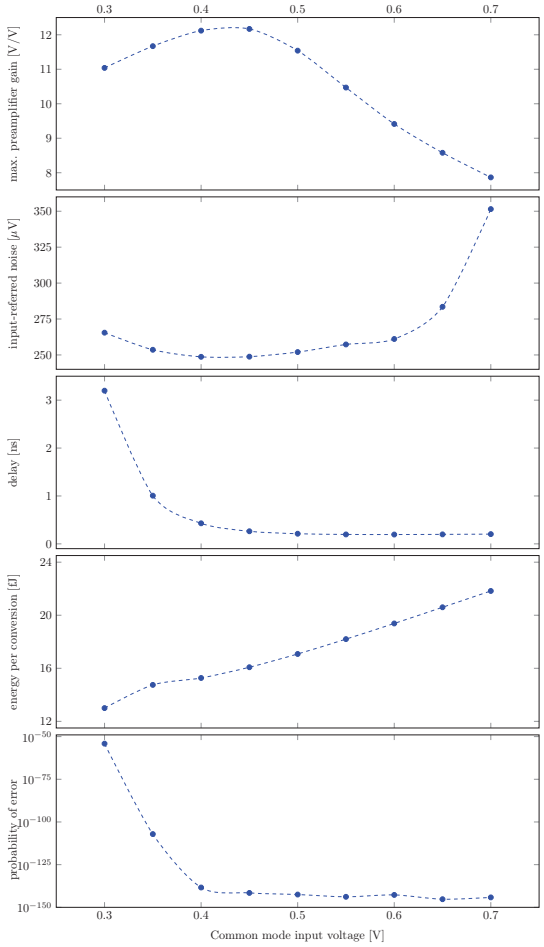

Fig. 5. Input common mode voltage impact on circuit parameters.

Ideally, the comparator takes a decision providing an output digital signal of either zero or one. In reality, sometimes the comparator does not make a decision in the required time, which happens at high conversion rates (see Fig. 5). As a result, the probability of error generation in a single conversion increases. This phenomenon is described by [12]:

$$P_{err} = \frac{2V_L}{A_{UL}LSB} \cdot e^{\frac{-T}{\tau}} \tag{3}$$

where V_L is the minimum valid logic level, A_{UL} is the comparator's gain, LSB is the voltage corresponding to the Least Significant Bit, T is the maximum time period to make a decision, and τ is the time difference between reaching at the latch differential output 1 mV and 2.718 mV (e, Euler's number). Here, the error probability was checked at 10 μV differential input voltage. As it can be seen for the considered resolution and conversion rate the metastability is not an issue.

We also checked how the first stage NMOS tail transistor and PMOS transistors influence the comparator's main parameters (see Fig. 6b and Fig. 6c). A larger channel width and shorter length of the first stage PMOS transistors result in a faster reset, while an increase in any of these dimensions causes higher overshoot (clock feed-through) due to larger parasitic capacitance (see Fig. 7). As the FP, FN nodes start dropping from a higher voltage, the time required to cross the second-stage threshold voltage is longer. Therefore, both the delay and the energy consumption increase.

B. Second Stage

The main impact on the comparator's parameters is revealed by the first stage (see Fig. 4). The second stage is responsible for the fast rail-to-rail (digital) output signal generation and this operation can be provided with low energy consumption and low area occupation by using minimum-size devices. However, the latch input transistors $M_{6,7}$, being fed with still quite a low voltage difference from the preamplifier, may significantly affect the offset and noise performance (see Fig. 8). It can be seen that to ensure fast latch settling at low energy consumption, small transistors seem to be a good option. However, at input transistors width lower than 500 nm, the voltage offsets and response delay increase rapidly. Additionally, the use of the doubled minimum length is also beneficial in terms of noise, not affecting dramatically the

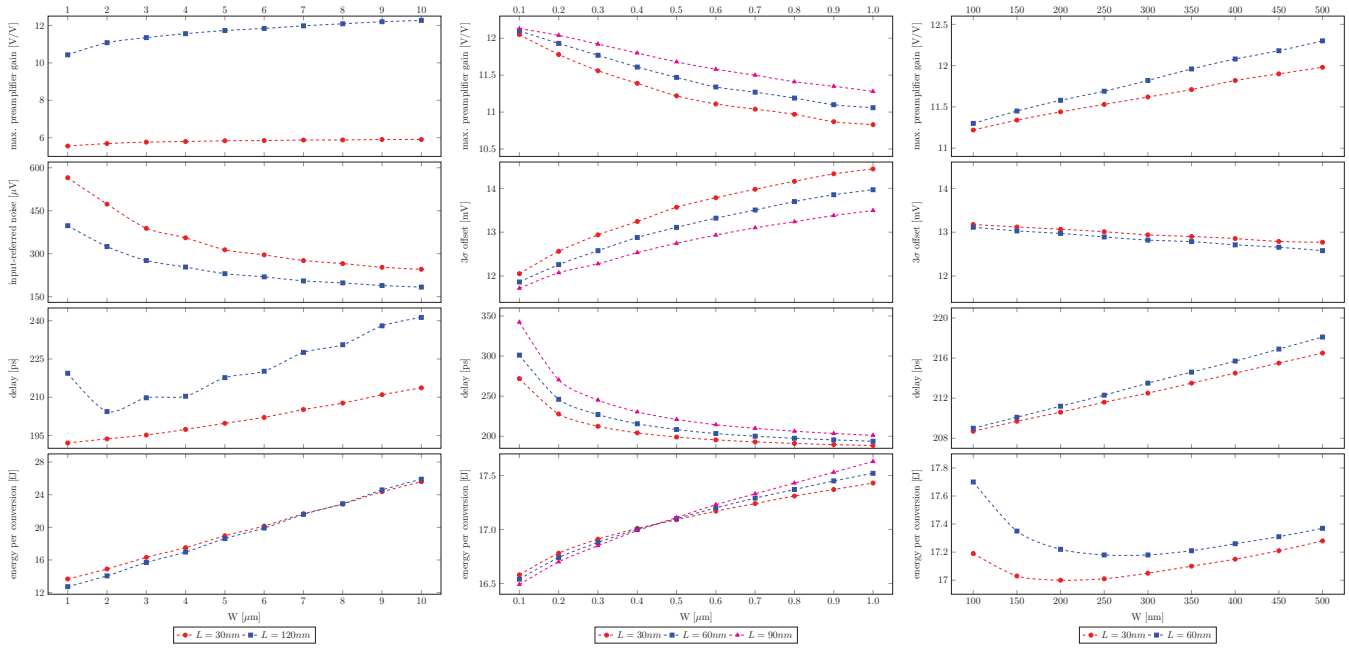

Fig. 6. Simulated impact of first stage (a) input pair, (b) NMOS tail, and (c) PMOS transistors dimensions on circuit parameters.

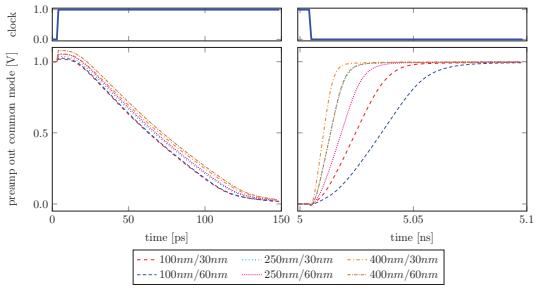

Fig. 7. First stage PMOS transistors impact on charging and discharging.

preamp gain and consumed energy. The PMOS transistors $M_{8,9}$, similarly as in a classic inverter, were assumed to be twice as wide as the NMOS $M_{10,11}$ to balance charging and discharging of SP, SN nodes.

C. Summary

Having in mind the thorough analysis, the low-area dynamic comparator of dimensions presented in Tab. I was designed. Its main parameters are listed in Tab. II. Fig. 9 presents voltages and currents of comparator during conversion and reset phases. The energy consumption was calculated by integrating the total current during a single cycle. As the comparator will be used in the asynchronous SAR ADC, we performed additional analysis of comparator's propagation delay for wide scale of differential input voltages (see Fig. 10). It can be seen that comparator's noise level and assumed ADC LSB are distant, preventing loss of the equivalent number of bits of the final ADC.

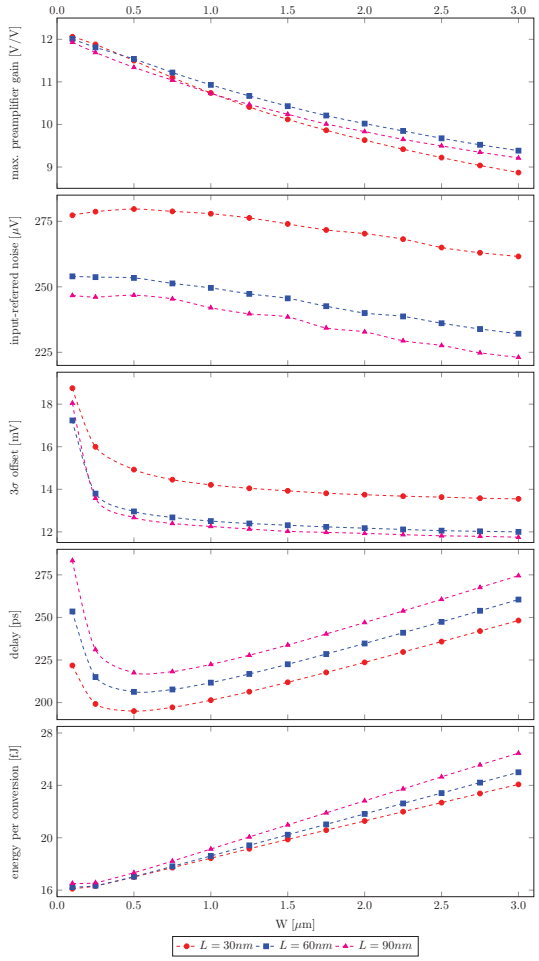

Fig. 8. Latch input transistors dimension impact on circuit parameters.

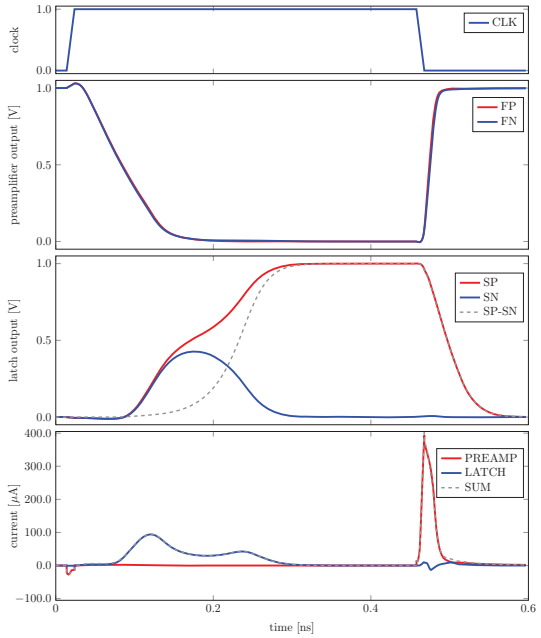

Fig. 9. Node voltages and currents of the first and the second stage of the comparator at 1 mV differential input voltage.

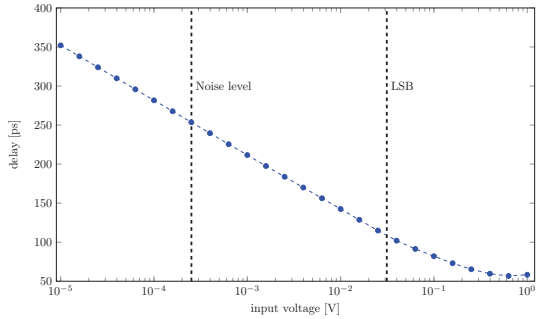

Fig. 10. Simulated comparator delay.

IV. Conclusion

In this work, the low-area dynamic comparator design in 28 nm CMOS process was presented. The influence of particular transistors dimensioning and input common mode voltage level were discussed. By using advanced technological node and proper transistors dimensioning, the energy efficiency of 17.1 fJ/comparison could be achieved at 10 MS/s. Thanks to the fully dynamic design, the power consumption only occurs while the comparator is triggered to take decision on differential input voltage.

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TABLE I
Proposed dimensions

Transistor	W	L
M_1,M_2	4 μm	120 nm
M_3,M_4	250 nm	30 nm
M_5	500 nm	60 nm
M_6,M_7	500 nm	60 nm
M_8,M_9	200 nm	30 nm
M_{10}-M_{13}	100 nm	30 nm

TABLE II
Main parameters

Parameter	Value	Unit
Max. Preamp Gain	11.5	V/V
Input-Referred Noise	252	μV_{rms}
Mismatch-Induced Offset (3σ)	13.0	mV
Propagation Delay (at noise level)	250	ps
Preamp Energy	7.5	fJ
Latch Energy	9.6	fJ
Total Energy	17.1	fJ
Estimated Area	5×5	μm^2

References

[1] K. Taguchi and J. S. Iwanczyk, "Vision 20/20: Single photon counting x-ray detectors in medical imaging." *Med. Phys.*, vol. 40, p. 100901, Oct. 2013.

[2] C. H. McCollough, S. Leng, L. Yu, and J. G. Fletcher, "Dual-and multi-energy CT: principles, technical approaches, and clinical applications," *Radiology*, vol. 276, no. 3, pp. 637–653, 2015.

[3] H. Kim, S. Han, J. Yang, S. Kim, Y. Kim, S. Kim, D. Yoon, J. Lee, J. Park, Y. Sung, S. Lee, S. Ryu, and G. Cho, "An asynchronous sampling-based 128×128 direct photon-counting x-ray image detector with multi-energy discrimination and high spatial resolution," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 541–558, Feb. 2013.

[4] R. Kłeczek, P. Gryboś, R. Szczygieł, and P. Maj, "Single photon-counting pixel readout chip operating up to 1.2 Gcps/mm^2 for digital X-ray imaging systems," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2651–2662, Sep. 2018.

[5] R. Ballabriga, J. Alozy, G. Blaj, M. Campbell, M. Fiederle, E. Frojdh, E. H. M. Heijne, X. Llopart, M. Pichotka, S. Procz, L. Tlustos, and W. Wong, "The Medipix3RX: a high resolution, zero dead-time pixel detector readout chip allowing spectroscopic imaging," *J. Instrum.*, vol. 8, no. 02, pp. 02 016–1–02 016–15, feb 2013.

[6] R. Dinapoli, A. Bergamaschi, D. Greiffenberg, B. Henrich, R. Horisberger, I. Johnson, A. Mozzanica, V. Radicci, B. Schmitt, X. Shi, and G. Tinti, "EIGER characterization results," *Nucl. Instrum. Meth.*, vol. A 731, pp. 68–73, 2013.

[7] A. Rivetti, *CMOS: Front-End Electronics for Radiation Sensors*. CRC Press, 2015.

[8] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta, "A 10-bit charge-redistribution ADC consuming 1.9μW at 1 MS/s," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1007–1015, May 2010.

[9] P. J. A. Harpe, C. Zhou, Y. Bi, N. P. van der Meijs, X. Wang, K. Philips, G. Dolmans, and H. de Groot, "A 26μW 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, Jul. 2011.

[10] B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]," *IEEE Solid-State Circuits Mag.*, vol. 7, no. 2, pp. 12–17, 2015.

[11] H. S. Bindra, C. E. Lokin, A. Annema, and B. Nauta, "A 30fJ/comparison dynamic bias comparator," in *Proc. ESSCIRC*, Sep. 2017, pp. 71–74.

[12] W. Evans, E. Naviasky, H. Tang, B. Allison, and J. Matsuzaki. (2006) Comparator metastability analysis. [Online]. Available: http://www.designers-guide.org/analysis/metastability.pdf

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