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Low power 9-bit pipelined A/D and 8-bit self-calibrated D/A converters for a DSP system

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Abstract. A low power, low voltage current mode 9 bit pipelined a/d converter and 8 bit self-calibrated d/a converter to interface a DSP system are presented in the paper. The a/d converter is built of 1.5 bit stages with digital error correction logic. The d/a converter is composed of 3 LSBs fine and 5 MSBs coarse current mode converters. The a/d and d/a converters were designed in 0.35 μm technology, then fabricated to verify the proposed concept. The performances of both converters are compared to the performances of known converter structures. The main advantages of the proposed converters are low power consumption and small chip area.

Key words: current mode circuits, pipelined a/d converter, self-calibrating d/a converter.

1. Introduction

A number of monolithic a/d and d/a converters have been proposed and implemented in the past few years [1-21]. In modern portable video applications low power and low chip area of the IC are required. Therefore, low power and low voltage approaches to the interfaces of the 2D DSP system are described in the present paper. Prototype pipelined a/d and self-calibrated d/a converter circuits were designed, fabricated and then tested. The converters were introduced at MWSCAS'2011 [2], and the present publication is an extension of the paper included in the proceedings of the MWSCAS'2011. As shown in Fig. 1, a pipelined a/d converter was proposed for the input interface and a self-calibrated d/a converter for the output interface of the DSP system, respectively.

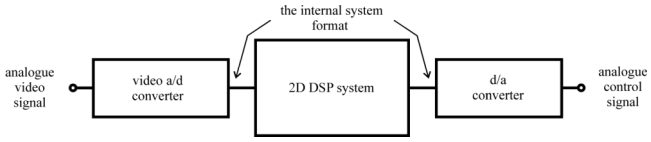

Fig. 1. DSP system with proposed I/O interfaces

The pipelined a/d converter structure is very attractive, because it effectively overcomes the power consumption and IC area limitations of the flash structure. The proposed pipelined a/d converter (ADC) converts the analogue current input signal into a digital voltage representation. The self-calibrated d/a structure is very attractive, because it offers both high resolution and accuracy of conversion. To improve the resolution and accuracy, the d/a converter (DAC) is built of two different structures to convert N most significant bits (MSBs) and M least significant bits (LSBs), respectively. The current mode conversion is used to optimize the power consumption and chip area of the presented converters. The low power consumption is a result of low voltage, current mode and AB class operation of converters functional blocks. The small chip area is a result of the small MOS capacitances used in the SI technique in comparison to commonly used SC technique.

2. Pipelined ADC functional building blocks

The N stages ($N + 1$ bit) pipelined ADC shown in Fig. 2 consists of a series of identical 1.5 bit stages that are isolated by track and hold (T/H) buffers, except for the last 2 bit stage. Each 1.5 stage is composed of the T/H buffer, a 1.5 bit sub-ADC (SADC), a 1.5 bit sub-DAC (SDAC), a subtractor and an amplifier with a gain equal to 2. The first stage operates on the most recent current sample, while the following stages operate on analogue remainder currents, called residues, from previous samples. In first stage the T/H buffer samples and holds the input current. In each next stage the T/H buffer samples and holds the output current from the previous stage. The held input current is converted into 1.5 bit digital code by the 1.5 bit SADC and then back to analogue by the 1.5 bit SDAC. The output current of the SDAC is subtracted from the held input current, and the difference is amplified by 2 to produce an output residue current that is passed on to the next stage. The held signal is passed along from stage to stage until it reaches the final stage in the pipelined ADC. The use of T/H buffers allows each of the stages to operate on N samples simultaneously, thus giving very high speed conversion of the pipelined ADC. The overall voltage output digital data are stored in the appropriate number of shift registers so that the digital data arriving at the correction logic correspond to the same sample. A digital correction logic is used to eliminate comparator offset. The correction structure uses additional comparators in each stage, to add an extra bit to configure 1.5 stages. The 1.5 bit stage is a 1 bit stage into which some redundancy is built to provide a large tolerance for component imperfections. This makes the pipelined ADC almost insensitive to comparator offsets.

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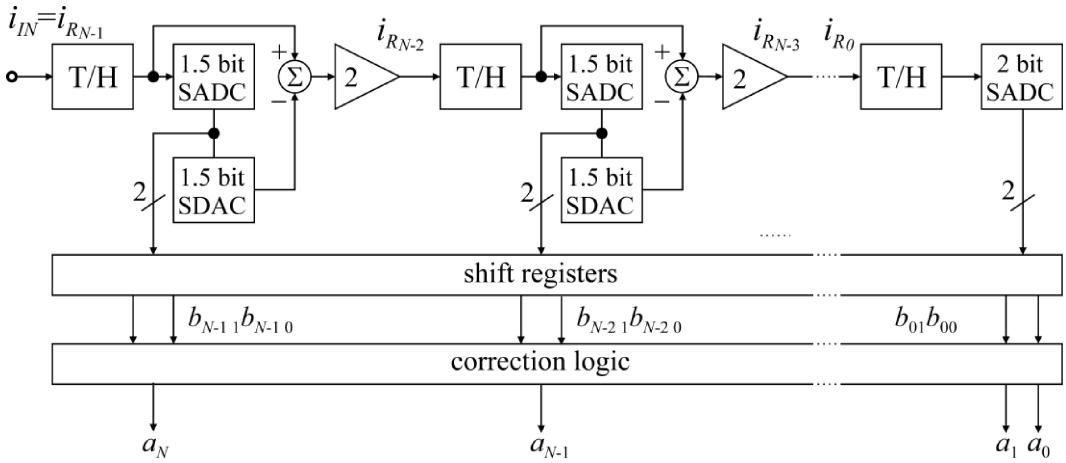


Fig. 2. Basic pipelined ADC with 1.5 bit stages

In each of the $N-1$ 1.5 bit stages of the ADC, the residue current is converted by the 1.5 bit SADC into 2 bit 3 states digital code (00, 01 and 10) and then back to analogue by the 1.5 bit SDAC. The output current of the SDAC is subtracted from the held input current, and the difference is amplified by 2 to produce an output residue current that is passed on to the next stage. In the last 2 bit stage, the residue current is converted by the 2 bit SADC into 2 bit 4 states digital code (00, 01, 10, 11). The proposed functional building block structures of the ADC composed of 1.5 bit stages will be described and presented in this paragraph in the same manner of description as presented in our publication [3] to the functional building block structures of the ADC composed of 2.5 bit stages. Detailed design and simulations results of the basic functional blocks are described in our publication [4].

2.1. Track and hold circuit. In each stage the analog residue current is passed to the next stage through the T/H circuit. The T/H circuit structure is shown in Fig. 3. It consists of a second generation AB class memory cell [22] and an output stage for a full-clock period output signal. The non-ideal effects of the circuit are described in detail in the literature [23]. The T/H circuit operates as follows. In each i^{th} stage of the pipelined ADC, during the track phase (ϕ_T), the next residue current sample i_{Ri} comes from the previous stage to the input of the T/H circuit. During the hold phase (ϕ_H), the T/H circuit holds the residue current sample i_{Ri} and output current $i_{T/HOUTi}$ equals i_{Ri}. The held analog current is passed along from stage to stage until it reaches the final stage in the pipeline. After every half-clock period, the next analog current sample follows the previous current sample, so at the same time, N analog current samples are being converted concurrently in the N stages of the pipeline. The sampling frequency of the T/H circuit is 50MHz. This value was selected in view of the application field of the proposed a/d converter. Another factor for choosing this frequency at the design stage was ability to refer the results of research to similar designs, as described in the world literature. The proposed T/H circuit in the pipelined ADC structure composed of 1.5 bit stages has already been successfully used in the pipelined ADC structure composed of 2.5 bit stages presented and described in detail in our publication [3].

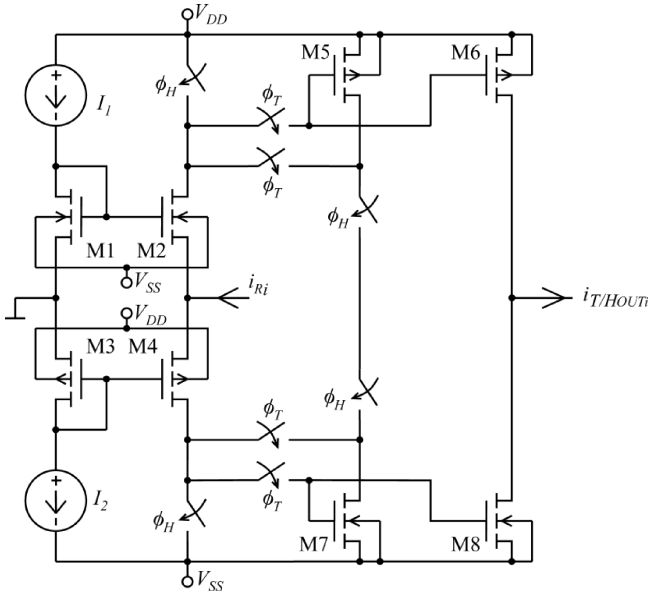


Fig. 3. Current-mode T/H circuit

2.2. 1.5 bit and 2 bit SADCs. The 1.5 bit current SADC is based on window comparator structure. Each 1.5 bit stage uses two symmetrical comparison current levels – I_{FS}/4 and I_{FS}/4, where I_{FS} and –I_{FS} to denote positive and negative full-scale currents, respectively. A choice of the full-scale levels is not critical, and for our design the input currents range from -100 μA to 100 μA. This range is chosen in order to reduce the noise influence and interference on the converter input and on the inputs of following stages of the pipelined structure. On the other hand, a limitation of the input current results in a smaller reference current I_{FS} It decreases the power consumption of the system. The operating current range is divided into three subranges and the 1.5 bit SADC output consists of two bits. This is the initial digital output,

after code conversion but before error correction. The SADC output codes $B_i = b_{i1}b_i$ are:

$$B_i = \begin{cases} 00 & \text{when } i_{R_i} \leq \frac{-I_{FS}}{4} \\ 01 & \text{when } \frac{-I_{FS}}{4} \leq i_{R_i} \leq \frac{I_{FS}}{4} \\ 10 & \text{when } \frac{I_{FS}}{4} \leq i_{R_i} \end{cases} \quad (1)$$
$$i = N-1, \ldots, 1$$

where N denotes the number of stages.

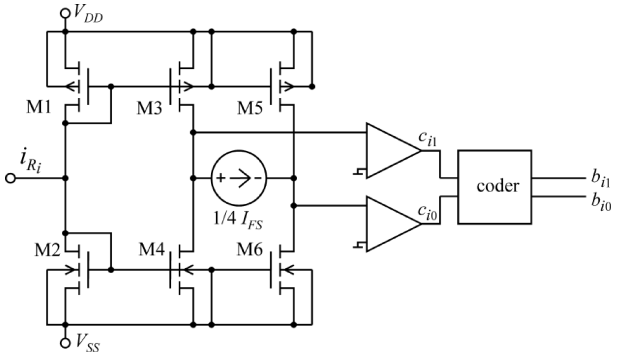


Fig. 4. Current-mode 1.5 bit SADC

The structure of the 1.5 bit current SADC based on current comparators is shown in Fig. 4. The structure consists of two current copiers, current sources I_{FS}/4 and$-I_{FS}$/4, two current comparators with voltage output, and a code converter. The current copiers are composed of the same sizes of NMOS and PMOS transistors, respectively. The current source I_{FS}/4 is used to add current to and$-I_{FS}$/4 to subtract current from current copiers resulting in two relevant current levels converted to temperature digital code $C_i = c_{i1}c_i$. The output coder converts the code C_i into 2 bit 3-state digital output codes $Bi = b_{i1}b_i$ of the 1.5 bit SADC described in Eq. (1). In the last stage, the 2 bit stage uses three symmetrical comparison current levels $-I_{FS}$/2, 0 and I_{FS}/2. The SADC output codes $B = b_{01}b_{00}$ are:

$$B_0 = \begin{cases} 00 & \text{when } i_{R_0} \leq \frac{-I_{FS}}{2} \\ 01 & \text{when } \frac{-I_{FS}}{2} \leq i_{R_0} \leq 0 \\ 10 & \text{when } 0 \leq i_{R_0} \leq \frac{I_{FS}}{2} \\ 11 & \text{when } \frac{I_{FS}}{2} \leq i_{R_0} \end{cases} \quad (2)$$

The structure of the 2 bit current SADC based on current comparators is shown in Fig. 5. The structure is similar to the structure of the 1.5 current comparator. Current sources I_{FS}/2 and $-I_{FS}$/2 are used to add current to or subtract current from current copiers resulting in two relevant current levels converted to temperature digital code $C = c_2c_1c_{00}$. The output coder converts the code C into 2 bit 4-state digital output codes $B_0 = b_{01}b_{00}$ of the 2 bit SADC described in Eq. (2).

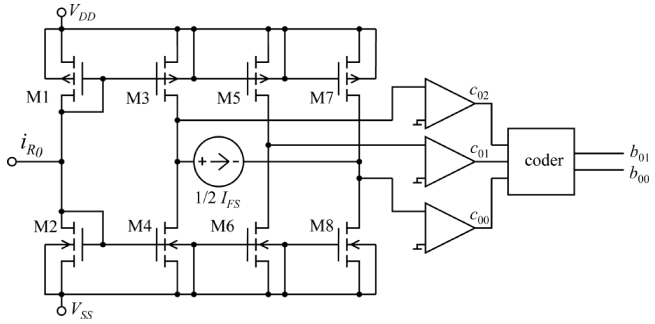


Fig. 5. Current-mode 2 bit SADC

The output codes B_i described by (1) and (2) are the initial digital outputs, after code conversion but before error correction.

2.3. 1.5 bit SDAC. The 1.5 bit SDAC structure is shown in Fig. 6. The structure consists of reference current sources $I_{FS}/2$ and $-I_{FS}/2$, and cascaded current copiers. The temperature digital code $C_i = c_{i1}c_i$ (corresponding to the output code $Bi = b_{i1}b_i$) of the 1.5 bit SADC is used to add or subtract reference current to or from the output current. Thus, the 1.5 bit SDAC current i_{SDACi} outputs are $-I_{FS}$/2, 0, I_{FS}/2 for the SADC$_i$ output codes 00, 01 and 10, respectively:

$$i_{SDAC_i} = \begin{cases} -\frac{I_{FS}}{2} & \text{for} \quad B_i = 00 \\ 0 & \text{for} \quad B_i = 01 \\ \frac{I_{FS}}{2} & \text{for} \quad B_i = 10 \end{cases}, \; i = N-1, \ldots, 1, \quad (3)$$

where N denotes the number of stages.

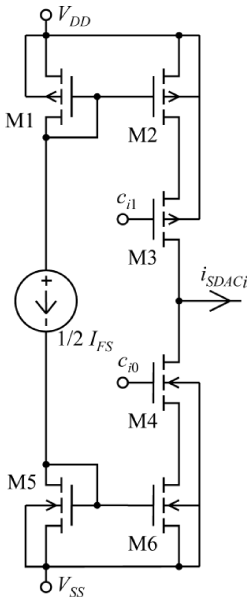


Fig. 6. Current-mode 1.5 bit SDAC

2.4. Reference current sources. The structures of 1.5 bit SDAC (Fig. 4), 2 bit SADC (Fig. 5) and 1.5 bit SDAC (Fig. 6) contain reference current sources $I_{FS}/2$, $-I_{FS}/2$, $I_{FS}/4$ and $-I_{FS}/4$.

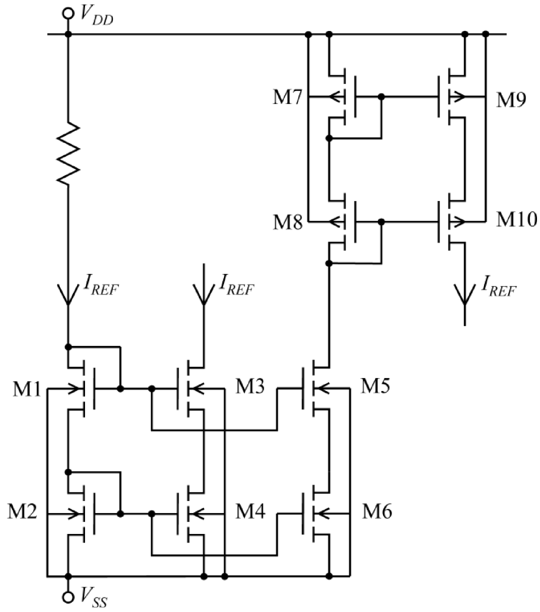


Fig. 7. Reference current sources

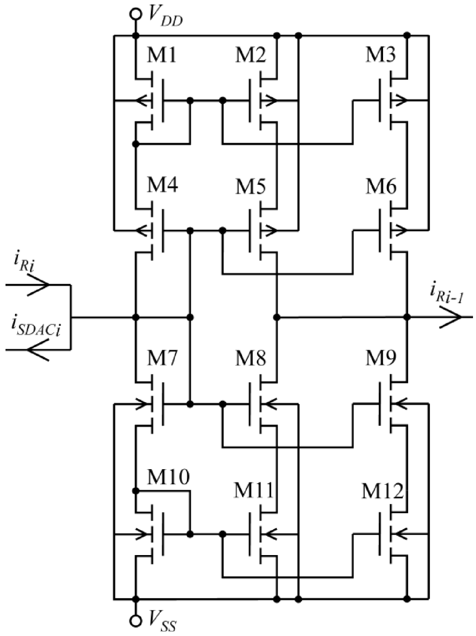


Fig. 8. Current multiply by two circuit

As shown in Fig. 7, cascaded current sources provide with all the desired sources to the ADC converter functional blocks. Two mirrors are used to produce reference currents I_{REF} and $-I_{REF}$.

2.5. Current multiply by two circuit. In each stage, the 1.5 bit SDAC output current is subtracted from the residue current of the previous stage, and the difference is multiplied by 2 to produce a residue current that is passed to the next stage. This residue current is expressed as follows

$$i_{R_{i-1}} = 2\left(i_{R_i} - i_{SDAC_i}\right) = \begin{cases} 2i_{R_i} + I_{FS} & \text{for} \quad B_i = 00 \\ 2i_{R_i} & \text{for} \quad B_i = 01 \\ 2i_{R_i} - I_{FS} & \text{for} \quad B_i = 10 \end{cases} \qquad i = N-1, \ldots, 1, \tag{4}$$

where N denotes the number of stages.

Cascaded AB class current sources are used to multiply the analogue current residue signal by 2 as shown in Fig. 8. To multiply negative currents by two, three PMOS transistors – an input transistor M4 and output transistors M5 and M6 – have the same dimensions and three PMOS transistors – active loads M1, M2 and M3 transistors – have the same dimensions, respectively. Similarly, to multiply positive currents by two, three NMOS transistors – an input transistor M7 and output transistors M8 and M9 – have the same dimensions and three NMOS transistors – active loads M10, M11 and M12 transistors – have the same dimensions, respectively. The output residue current (4) is passed to the next stage.

2.6. Correction logic. A pipelined architecture is sensitive for comparator offset errors. An error correction is achieved by the correction logic structure shown in Fig. 9. The overall voltage output digital data are stored in the appropriate number of shift registers so that the digital data arriving at the correction logic correspond to the same sample. The error correction is solved by adding a single extra comparator in each 1 bit stage resulting in a 1.5 bit stage except for the final one in which two extra comparators are added resulting in a 2 bit stage. Each 1.5 bit stage produces a 2 bit code. Once the error correction algorithm is applied, the 2 bit per stage code $B_i = b_{i1}b_{i0}$ is reduced to the final one bit per stage code. To generate the final error corrected N+1 bit output code from the 2 bit codes, the two digital outputs from each adjacent stage are added together with 1 bit overlapped between adjacent stages as follows:

$$\begin{array}{lcccccccc} B_{N-1} = & b_{N-11} & b_{N-10} & & & & & & \\ \multicolumn{9}{l}{\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots} \\ B_2 = & & & & b_{21} & b_{20} & & & \\ B_1 = & & & & & b_{11} & b_{10} & & \\ B_0 = & & & & & & b_{01} & b_{00} & \\ \hline A = & a_N & a_{N-1} & \ldots & a_3 & a_2 & a_1 & a_0 & \end{array} \tag{5}$$

The correction procedure is illustrated on the last 2 stages: the 1.5 bit and 2 bit stages, respectively. The procedure to determine codes in two different ranges with no offset error is illustrated in Fig. 10a. The codes for those ranges are 010 and 101. The procedure to determine codes in two different ranges for error offset is illustrated in Fig. 10b. The codes for those ranges remain 010 and 101, respectively.

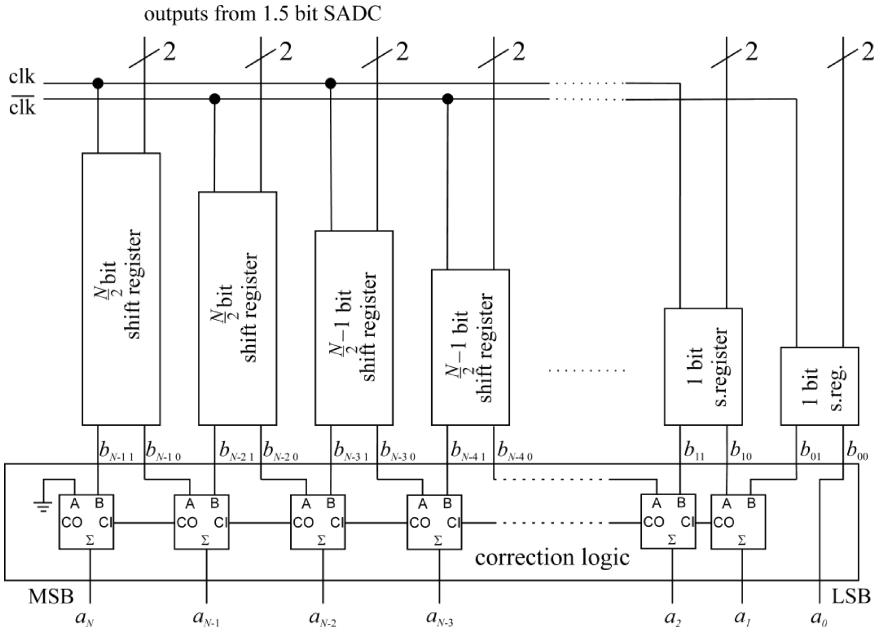


Fig. 9. Correction logic structure

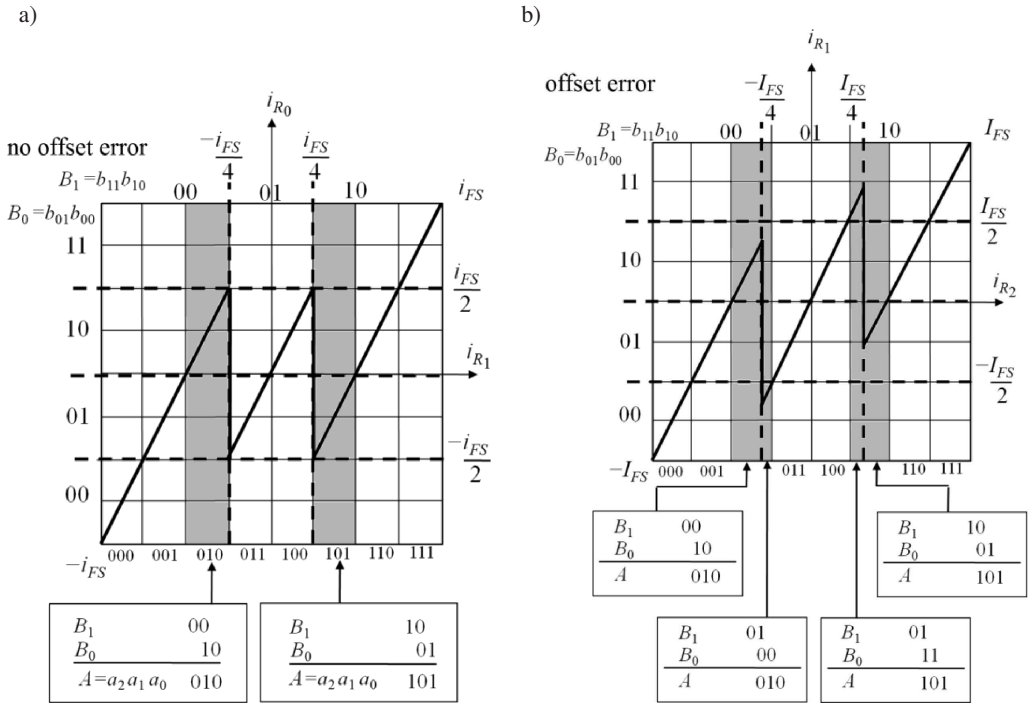


Fig. 10. Procedure to determine digital codes

3. Self-calibrated DAC

The self-calibrated current mode $M+N$ resolution d/a converter (DAC) is shown in Fig. 11. It consists of M LSBs fine and N MSBs coarse converters. The fine converter is composed of bidirectional current switches and an M bit binary current divider, while the coarse converter is composed of bidirectional current switches, a calibrated multiple dynamic current mirror and a coarse decoder, respectively.

The fine converter structure is shown in Fig. 12. The M bit binary current divider and the bidirectional current switches controlled by the M least significant data bits are used to divide reference current I_{REF} with respect to M LSBs. Thus, the fine output current is

$$\begin{aligned} i_{OUTM} &= I_{REF} \sum_{i=N+1}^{N+M} a_i 2^{N-i} \\ &= 2^N I_{REF} \sum_{i=N+1}^{N+M} a_i 2^{-i}. \end{aligned} \tag{6}$$

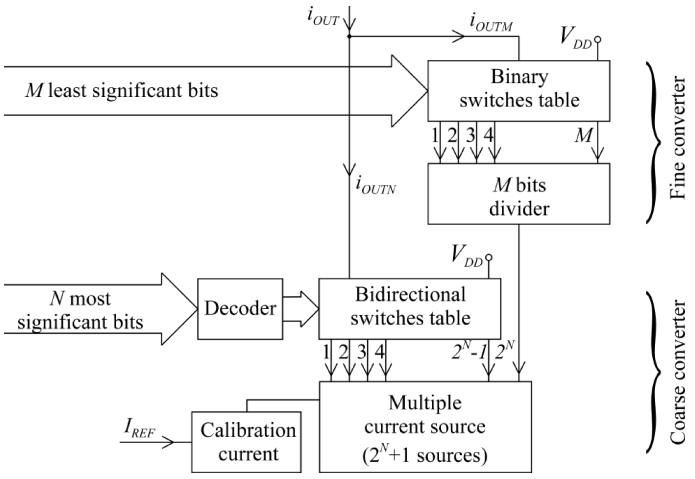


Fig. 11. The proposed self-calibrated DAC structure

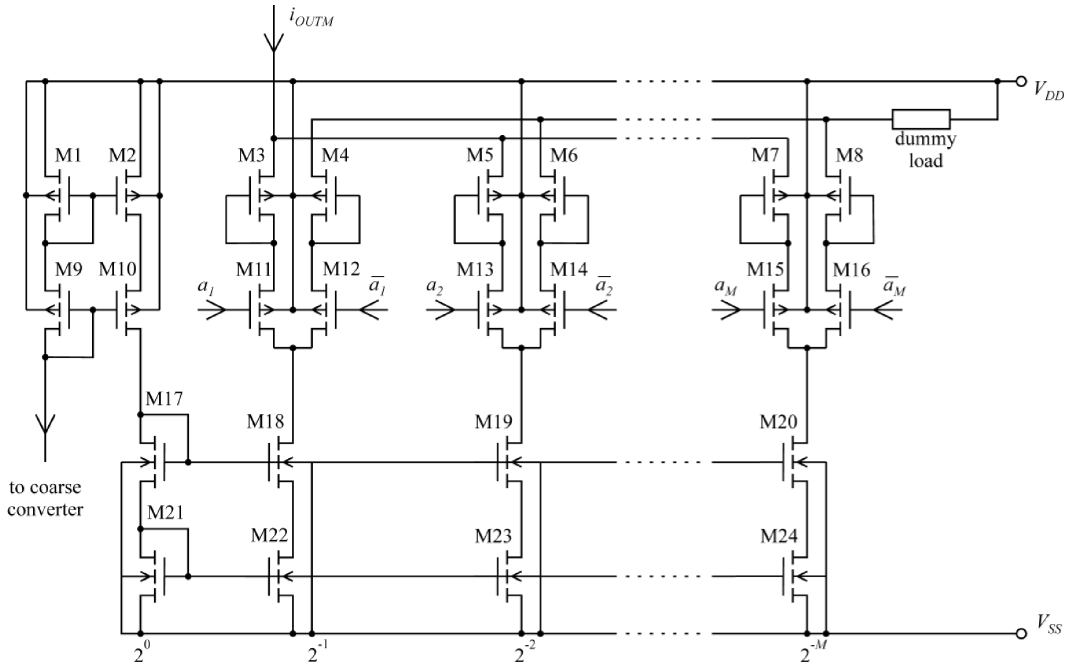


Fig. 12. The fine M LSBs converter

The rest of the reference current ($I_{REF} - i_{OUTM}$) is dumped to a fine dummy load by the two-way current switches. Finally, Eq. (6) can be rearranged into the following form:

$$i_{OUTM} = I_{FS} \sum_{i=N+1}^{N+M} a_i 2^{-i}, \tag{7}$$

where

$$I_{FS} = 2^N I_{REF}. \tag{8}$$

The coarse converter structure without coarse decoder is shown in Fig. 13. The N bit calibrated multiple dynamic current mirror and the bidirectional current switches controlled by the outputs of the decoder (y_1 to y_N) are used to sum the appropriate number of reference currents I_{REF} with respect to N MSBs. The calibrated multiply dynamic current mirror generates 2^N copies of the reference currents I_{REF}. $2^N + 1$ phases and different switches are demanded to calibrate 2^Ncopies of reference current I_{REF}. Each copy of the reference current is calibrated by the reference current during one phase per cycle. In fact, the current source composed of transistor the M12 is used to replace the calibrated one. One of the 2^N outputs is used to determine the current of M least significant bits. The rest of the $2^N - 1$ outputs are connected to the output or to a coarse dummy load. Therefore, the coarse output current is

$$i_{OUTN} = I_{FS} \sum_{i=1}^{N} a_i 2^{-i} \tag{9}$$

and the total current can be expressed as follows:

$$i_{OUT} = i_{OUTN} + i_{OUTM} = I_{FS} \sum_{i=1}^{N+M} a_i 2^{-i}. \tag{10}$$

The resolution of the converter is $N + M$ bits.

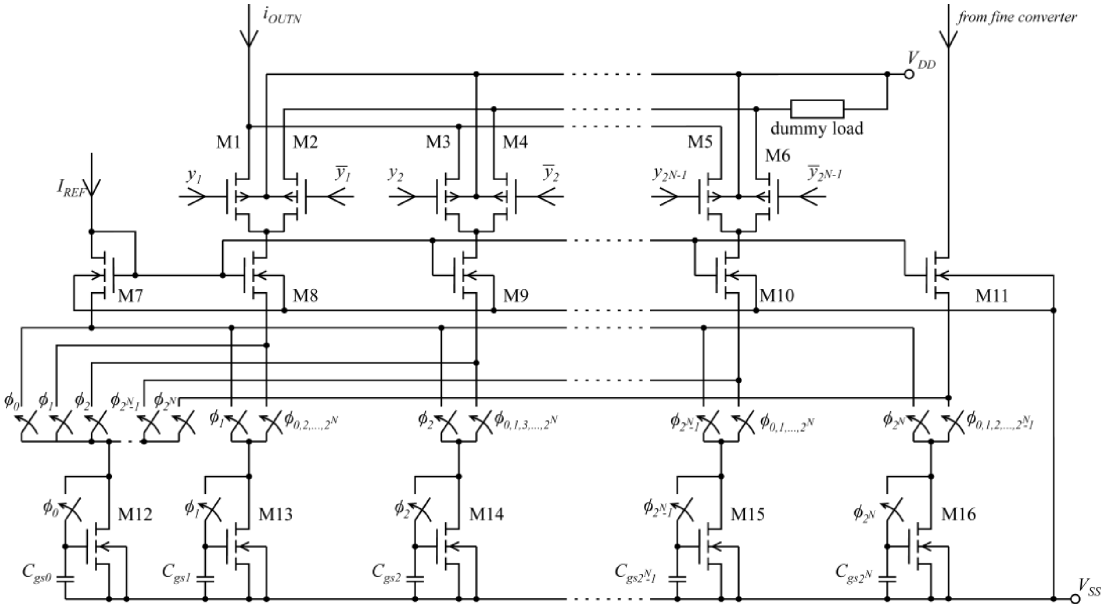


Fig. 13. The fine N MSBs converter without coarse decoder

4. Experimental results and concluding remarks

To verify the proposed current-mode pipelined ADC and self-calibrated DAC structures, the ASIC experimental circuit shown in Fig. 14 was designed. The circuit contains plenty of current mode building blocks to configure 1.5 bit and 2 bit stages N bit ADC and self-calibrated N bit DAC. All the building blocks were designed in CMOS AMS 0.35 μm technology simulated, fabricated and measured. The ASIC building blocks were used to configure a 9 bit resolution prototype pipelined ADC composed of seven 1.5 bit stages and one 2 bit stage. The performances of the ADC were measured and compared to the performances of pipelined ADC structures fabricated in 0.35 μm or similar technologies [59]. The static linearity of the ADC was measured using a low-frequency (10 kHz) tone and analyzing over 10^5 output codes. The code density was used to determine maximum differential nonlinearity (DNL) and maximum integral nonlinearity (INL) errors. A code density test showed DNL is 0.7 LSB and INL is 0.9 LSB. Figure 15 shows the plots of the DNL and INL versus the output code, respectively.

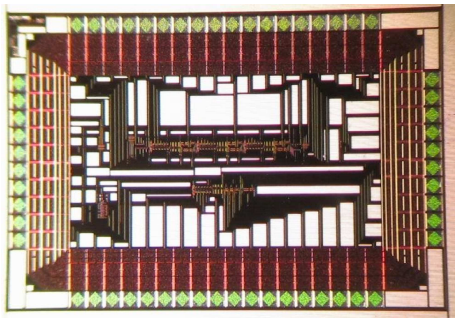
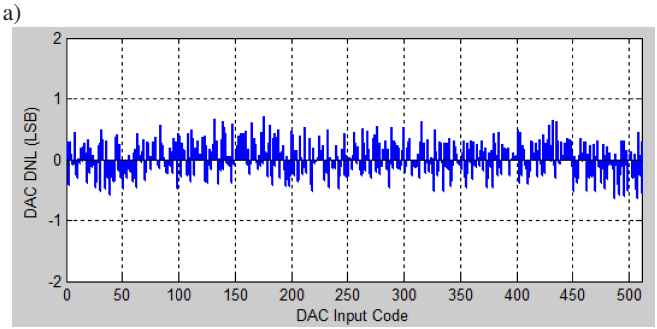


Fig. 14. ADC and DAC chip micrograph of experimental circuit in 0.35μm technology

a)



b)

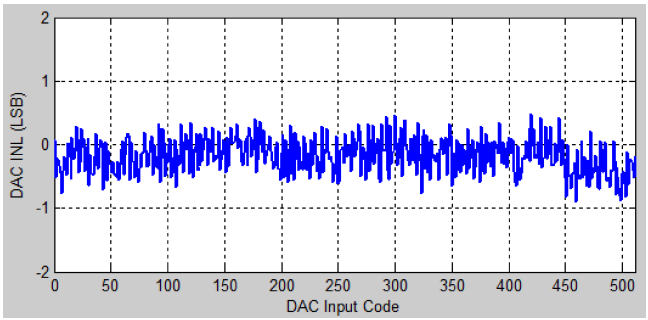


Fig. 15. (a) ADC DNL, (b) ADC INL

The dynamic linearity of the ADC was measured by analyzing the Fast Fourier Transform of the output codes for a single input tone at the Nyquist rate. The FFT of the ADC output was used to determine a Spurious Free Dynamic Range (SFDR) and Signal to Noise and Distortion Ratio (SNDR) at the Nyquist rate. Figure 16 shows the FFT of the ADC output at 50Msamples/s with 24.95 MHz full-scale sine wave input above the Nyquist rate to avoid aliasing. The SFDR is 74.32 and SNDR is 51.83 dB

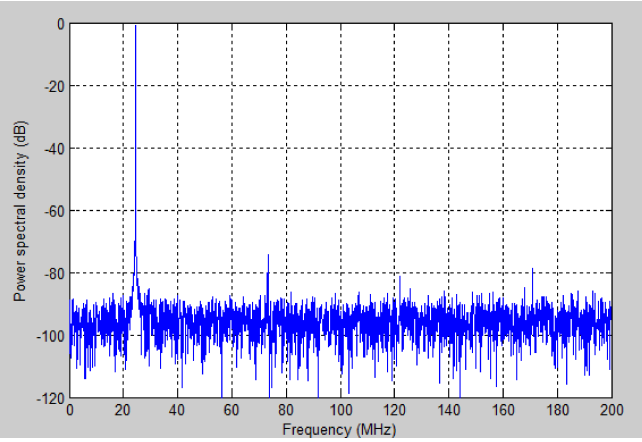


Fig. 16. ADC power spectrum with 24.95 MHz tone

All the measured performances of the ADC fabricated in CMOS 0.35 μm technology are summarized in Table 1 and compared to the performances of known: switched capacitor (SC) voltage mode [5–7] and switched current (SI) [8, 9] ADCs fabricated in the CMOS 0.35 μm and 0.25 μm technologies. Additionally, the performances of the pipelined ADCs fabricated in the CMOS 0.09 μm and 0.065 μm technologies [10–13] are shown in Table 1. Figures of merit (*FOM*) and *ENOB* parameters of all ADC structures are also described. Table 1 shows that the *FOM* of the presented ADC is lower than that of the other ADC structures, except for the ADC [6]. The *ENOB* parameter of the presented ADC is comparable to that of the other ADC structures. The following performances of the presented ADC: sampling rate, resolution, SFDR, SNDR, DNL and INL are comparable to the performances of the other ADC structures. The following performances of our ADC: active chip area and supply voltage are lower than the performances of the ADCs fabricated in CMOS 0.35 μm or 0.25 μm technologies and comparable to the performances of the ADCs fabricated in CMOS 0.09 μm or 0.065 μm technologies. Power consumption of the presented ADC is lower than that of the other ADCs fabricated in CMOS 0.35 μm or 0.25 μm technologies except for the ADC [7] and ADCs fabricated in CMOS 9 nm and 65 nm technologies. Low power consumption is a result of AB class operation of converters functional blocks and low supply voltage, which has no influence on input current range and final resolution. The small active chip area is a result of small MOS capacitances used in switched current technique.

Having examined the results presented in Table 1, we can conclude that the presented ADC functions correctly and satisfies the input requirements. The advantages of the presented current mode converter are low power consumption and small active area. The other performances are similar to the performances of known SC and SI pipelined ADCs fabricated in the CMOS 0.35 μm and 0.25 μm technologies To reduce power consumption of the presented ADC, the building blocks of the ADC are designed in AB class where no large bias currents are used. To reduce chip area of the presented ADC, the current-mode technique is used. Further decrease of supply voltage, power consumption and active chip area of the proposed SI ADC can be achieved by the use of technologies with dimensions smaller than 0.25 μm.

The ASIC building blocks were used to configure an 8 bit resolution prototype self-calibrated DAC composed of 5+3 most significant and least significant bit sections, respectively. The performances of the DAC were measured and are presented in Table 2.

Similarly to the ADC measurements, the static linearity of the DAC was measured using a low-frequency (10 kHz) tone and analyzing over 10^5 output codes. A code density test showed that DNL and INL are both equal to 0.2 LSB. Figure 17 shows the plots of the DNL and INL versus output code, respectively.

Table 1
Comparison of performances of the proposed and other SC and SI ADCs

	This work	[5]	[6]	[7]	[8]	[9]	[10]	[11]	[12]	[13]
Architecture (b/st.)	1.5	1.5	2.5	1.5	1.5	3.5	2.5	1.5	1.5	1.5
Technology (μm)	0.35	0.25	0.35	0.35	0.35	0.35	0.09	0.09	0.09	0.065
Resolution (bit)	9	10	10	8	8	10	9	9.4	10	10
Sampling rate (Hz)	50M	30M	20.5M	19M	12.5M	100M	250M	50M	80M	100M
Supply voltage (V)	3.0	3.0	1.5	2.5	3.3	3.3	1.1	1.2	0.8	1.2
Power (mW)	10	60	19.5	4	29	498	22.8	1.44	6.5	4.5
SNDR (dB)	51.83	56.51	56	–	44.6	–	38.7	49.4	–	59
SFDR (dB)	74.32	71.94	60	51.57	–	70.6	46	–	–	–
DNL (LSB)	0.7	0.4	0.3	0.63	0.4	–	1.2	–	–	–
INL (LSB)	0.9	0.85	3.4	0.58	0.8	–	1.4	–	–	–
ENOB	8.31	9.09	–	7.3	7.3	–	6.13	7.91	8.84	9.5
FOM (pJ/conv.)	0.63 p	3.91	0.19	1.88	14.7	–	2.21	119	178	62
Active area (mm^2)	0.19	1.36	1.3	4.78	0.72	12.7	0.8	0.123	0.64	0.07

Table 2
Comparison of performances of the proposed self-calibrated and other DACs

	This work	[14]	[15]	[16]	[17]	[18]	[19]	[20]	[21]
Technology (μm)	0.35	0.35	0.25	0.25	0.35	0.35	0.18	0.35	0.18
Resolution (bit)	8	8	10	8	10	8	8	8	10
Sampling rate (Hz)	50M	50M	200M	50M	210M	100M	500M	100M	–
Supply voltage (V)	3.0	3.3	3.3	2.0	3.3	3.3	1.8	3.3	1.8
Power (mW)	24	2.5	82	2	83	54.5	–	45	–
SNDR	56.1	–	–	–	50	–	44	–	–
SFDR (dB)	58.3	58	55.5	50	53	62.13	35.42	54	–
DNL (LSB)	0.2	0.37	0.3	0.3	0.7	0.12	0.14	0.15	0.35
INL (LSB)	0.2	0.3	0.2	0.23	1.1	0.32	0.33	0.15	0.30
Active area (mm^2)	0.32	0.4	0.91	0.25	5	0.449	–	0.449	0.45

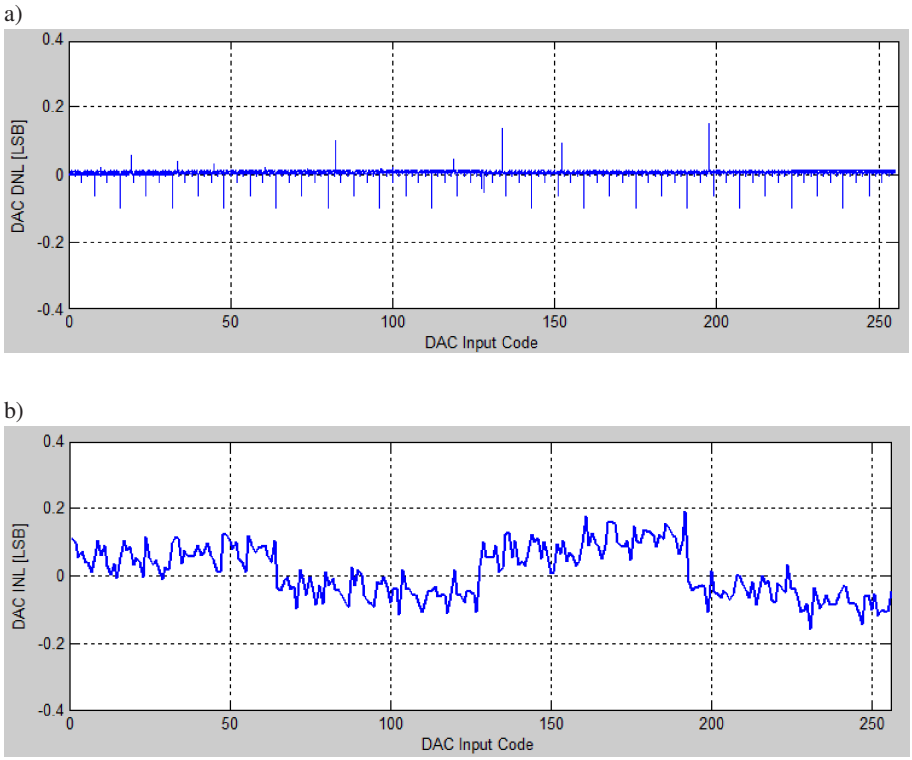


Fig. 17. (a) DAC DNL, (b) DAC INL

All the measured performances of the DAC fabricated in CMOS 0.35 μm technology are summarized in Table 2 and compared to the performances of the prototype current-mode DACs known in the literature. Their applications cover HD TV, Bluetooth transmission, the widespread WLAN networks, and others. They are fabricated in CMOS 0.35 μm, 0.25 μm and 0.18 μm technologies. The performances of the proposed DAC are mostly similar or better to the performances of the DAC structures presented in the literature [14–21].

Presented DAC has rather small active chip size and good DNL and INL parameters. Power consumption of our DAC is small, but not so small as that of DACs [14, 16]. It is a consequence of a complexity of multiple dynamic current source structure, but the presented DAC structure results in better conversion accuracy.

Having examined the results presented in Table 2, we can conclude that the presented DAC functions correctly and satisfies the input requirements. The advantages of the presented current mode DAC are low power consumption and small active area. The other performances are similar to the performances of known DACs.

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