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Active power decoupling topology for AC-DC and DC-AC single-phase systems with decoupling capacitor minimization

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Abstract: Passive power decoupling in single-phase DC-AC and AC-DC systems usually requires usage of electrolytic capacitors. To minimize converter volume, increase reliability, robustness and to eliminate ripple power effect on the DC side, new solutions for Active Power Decoupling are proposed. In this paper a novel Active Power Decoupling topology for low power single-phase AC-DC and DC-AC converters is presented. The proposed topology is based on well-known boost and buck-boost topologies but with a completely different control scheme. The topology description with a complete control algorithm is presented. The proposed APD solution is verified by experimental results of a 450 W converter in AC-DC mode and a 320 W converter in DC-AC mode.

Key words: active power decoupling, capacitance reduction, microgrid converter, double-line frequency ripple power, single-phase systems, power factor correction

1. Introduction

In recent years, especially in highly developed countries, increased demand for all kinds of consumer goods in particular consumer electronics and household appliances is noted. Most of these devices are a low power DC load type connected to a single-phase AC line [1–3]. In the Smart Grid concept, which is gaining attention in recent years [4–6], small photovoltaic systems frequently use microinverters which a connect photovoltaic DC source to the AC power grid [7]. In order to exchange power in AC-DC or DC-AC single-phase systems, power converters are needed.

In single-phase AC-DC and DC-AC systems with sinusoidal current in the utility line the phenomenon of instantaneous power imbalance occurs. If ripple second harmonic power is not compensated, it can propagate to the DC part of the subsystem [1, 3, 8–9]. This can lead to significant problems in DC systems reducing performance, efficiency and lifespan [1, 3, 8–9].

Potential problems in DC-AC systems are low-frequency flicker of LED lamps, shortening of fuel-cell/batteries lifespan [2, 3], reducing PV power conversion by limiting MPPT algorithm efficiency [2–3, 7, 9]. In a single-phase AC-DC converter powering inverters driving 3-phase AC motors (e.g. household appliances) double-line frequency power ripple presence leads to an undesired second harmonic in motor currents, hence to the motor's torque causing vibrations and faster wear.

In most single-phase converter topologies, instantaneous power decoupling is realized by passive decoupling providing the decoupling capacitor with capacity high enough to passively filter ripple second harmonic power [3, 9]. In most cases decoupling capacitance is several times greater than needed from the system power decoupling perspective. To obtain high capacities, electrolyte capacitors (E-caps) are used [3, 9–10]. This leads to severe consequences as E-caps are known as the most unreliable components in power electronic converters with high failure rates, rapidly increasing with high operating temperatures [1, 3, 7, 9–11].

To address these issues the Active Power Decoupling (APD) technique has been recently widely studied [1–3, 7–10, 12–18, 20]. APD can be categorized in many ways: dependent vs independent techniques [2], closed-loop vs open-loop control method [3], capacitive vs inductive energy storage [3], AC vs DC decoupling [8, 10]. Despite many possible approaches, the fundamental idea behind any APD method is to (according to Sun *et al*. [3]) "*divert the ripple power to another specific energy storage component with relatively small size and long lifetime by an extra active switching circuit*".

In this paper a novel topology for APD technique for AC-DC and DC-AC mode of operation is presented. The topology implements DC side APD technique with capacitive energy storage. The main advantages of the proposed topology are a simple closed-loop control method hence good performance under disturbances and parameter variation, utilization of film capacitors, unity power factor and elimination of double-line frequency ripple power component on the DC side. The paper describes the double-line frequency ripple power phenomenon and the DC side power decoupling principle. An extensive explanation of the topology's working principle with derivation of a formula for decoupling capacitor parameters is presented. A closed-loop control algorithm for AC-DC and DC-AC mode of operation is described. The proposed topology and control algorithm features and performance are verified by experimental results.

2. Power decoupling principle

Assuming that a single-phase AC system has sinusoidal voltage and unity power factor, voltage and current waveforms can be expressed as:

$$\begin{cases} u_{ac}(t) = U_m \sin(\omega t) \\ i_{ac}(t) = I_m \sin(\omega t) \end{cases}, \tag{1}$$

where: U_m is voltage amplitude, I_m is current amplitude and ω is angular frequency.

Hence, instantaneous power in a single-phase system is equal to:

$$p_{ac}(t) = u_{ac}(t) \cdot i_{ac}(t) = U_m \cdot I_m \sin^2(\omega t) = P_{ac} - P_{ac} \cdot \cos(2\omega t), \tag{2}$$

where: P_{ac} is the average power.

Instantaneous power consists of average power equal to DC load power (not considering converter losses) and a variable component with double line frequency. In order to compensate for the variable power component, an energy storage element (capacitor or inductor) is needed.

According to [1] recently more studies on capacitive energy storage are conducted. When a capacitor is responsible to store the energy imbalance in its electrical field, its instantaneous voltage can be expressed as (according to [8, 12–13, 20]):

$$\begin{cases} u_C(t) = \sqrt{U_0^2 + \dfrac{P_{ac}}{C \cdot \omega} \cdot \sin(2\omega t)} & \text{for } DC-AC \\ u_C(t) = \sqrt{U_0^2 - \dfrac{P_{ac}}{C \cdot \omega} \cdot \sin(2\omega t)} & \text{for } AC-DC \end{cases}, \tag{3}$$

where: u_c is the decoupling capacitor voltage, U_0 is the decoupling capacitor stabilized voltage value and C is the decoupling capacity.

During each AC system cycle (20 ms for 50 Hz systems) the energy imbalance is stored (during periods where there is excessive energy in AC system) and delivered (during periods of lack of energy in AC system) twice (Fig. 1). The energy needed to compensate power imbalance in each decoupling cycle (10 ms – Fig. 1) can be express as a difference of maximum and minimum energy of the decoupling capacitor (based on (3)):

$$\Delta W = \frac{1}{2} C \cdot \left(U_{C\max}^2 - U_{C\min}^2\right) = \frac{P_{ac}}{\omega}, \tag{4}$$

where: ΔW is the balancing energy needed for each decoupling cycle, $U_{C\max}$ is the maximum voltage of decoupling capacitor, $U_{C\min}$ is the minimum voltage of decoupling capacitor.

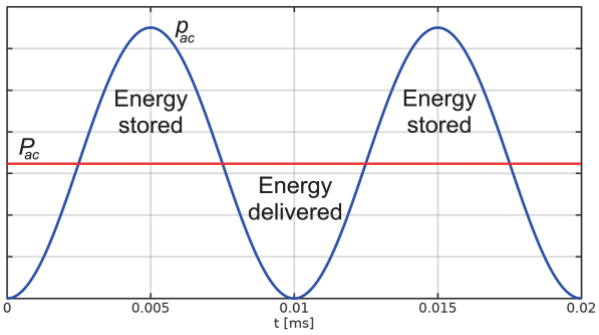


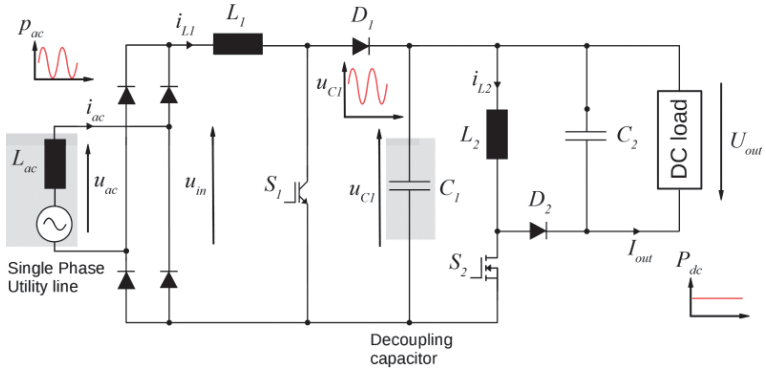
Fig. 1. Instantaneous power flow in AC-DC, DC-AC system

ΔW is the energy needed to decouple AC and DC systems in each decoupling cycle, therefore it is a theoretical limit for decoupling capacitor energy volume, that all APD solutions aim to achieve.

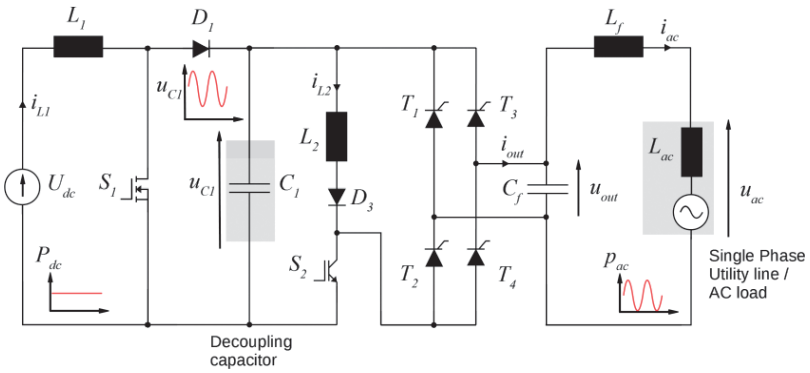
3. Operating principle of proposed topology

3.1. Circuit topology

In Fig. 2, a proposed topology for AC-DC (a) and DC-AC (b) mode of operation is presented. The proposed topology consists of input boost converter (inductor L_1, transistor S_1, diode D_1 and power decoupling capacitor C_1) and output buck-boost converter (capacitor C_1, transistor S_2, inductor L_2 and in the case of DC-AC mode diode D_3 and thyristors T_1, T_2, T_3, T_4 or diode D_2 and capacitor C_2 in the case of AC-DC mode). Although the topology is based on well-known DC-DC topologies, it needs to be emphasized that the control algorithms are completely different than in classical solutions. The converters' work is combined, with one control algorithm and driver circuit. The input part (boost converter) can work in continuous current mode allowing elimination of an external input filter.



(a)



(b)

Fig. 2. Proposed topology for AC-DC (a) and DC-AC (b) operation

In AC-DC mode of operation, the input part is responsible for grid current shaping, forcing sinusoidal current waveform (fundamental harmonic) in phase with grid voltage allowing Power Factor Correction. Inductor L_1 RMS current depends on the converter's DC output load. In DC-

AC mode of operation, the input part is responsible for elimination of second harmonic ripple in the input current. The main field of application of DC-AC mode converter is a single-phase microinverter connected to a PV module. For proper operation, converter output power depends on the accessible instantaneous power of PV module (depending on the irradiance), hence inductor L_1 input average current depends on the converter's DC instantaneous input power.

The output part (buck-boost converter) works in discontinuous current mode. This allows simplification of the signal conditioning circuit as only the peak value of L_2 inductor current is controlled. In AC-DC mode of operation, the output part is responsible for control of output voltage U_{out} level without second harmonic ripple. In DC-AC mode of operation, the output part shapes inductor L_2 current as a rectified sinusoidal waveform in phase with grid voltage. Thyristor pairs (T_1, T_4 and T_2, T_3) operate with half cycle modulation, shaping grid current i_{ac}. D_3 diode is responsible for blocking reverse current during thyristors' reverse recovery in each transistor's S_2 switching cycle. This provides better controller stability and slightly improves converter efficiency. A detailed description of this phenomenon can be found in [13, 20].

Input and output parts are connected by DC-link power decoupling capacitor C_1 which provides storage for instantaneous imbalance energy. By allowing high voltage levels, capacitance can by minimized, hence elimination of electrolytic capacitors is possible. With boost converter as input stage for proper operation decoupling capacitor voltage (u_{C1}) must be always greater than input voltage. This condition can be written as:

$$\begin{cases} u_{C1}(t) > U_{dc} & \text{for } DC-AC \\ u_{C1}(t) > |u_{ac}(t)| & \text{for } AC-DC \end{cases}, \tag{5}$$

where: u_{C1} is decoupling capacitor voltage, U_{dc} is input voltage for DC-AC mode and u_{ac} is input voltage for AC-DC mode.

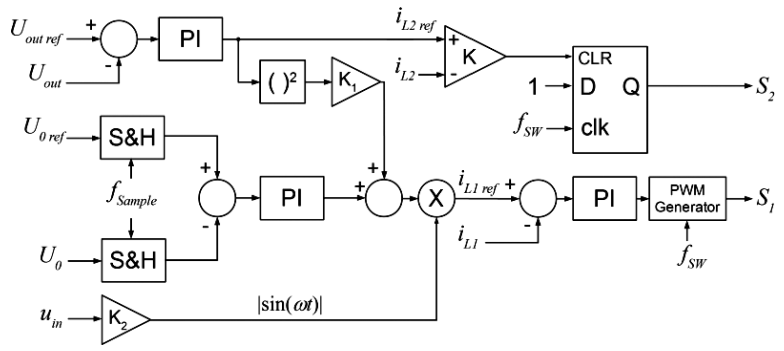
Solving (3) and (5) the formula for value of a decoupling capacitor can be obtained from:

$$\begin{cases} C_1 > \dfrac{P_{ac}}{\omega} \cdot \dfrac{1}{U_0^2 - U_{dc}^2} & \text{for } DC-AC \\ C_1 > \dfrac{P_{ac}}{\omega} \cdot \max\left[\dfrac{\sin(2\omega t)}{U_0^2 - U_m^2 \sin^2(\omega t)}\right] & \text{for } AC-DC \end{cases}. \tag{6}$$

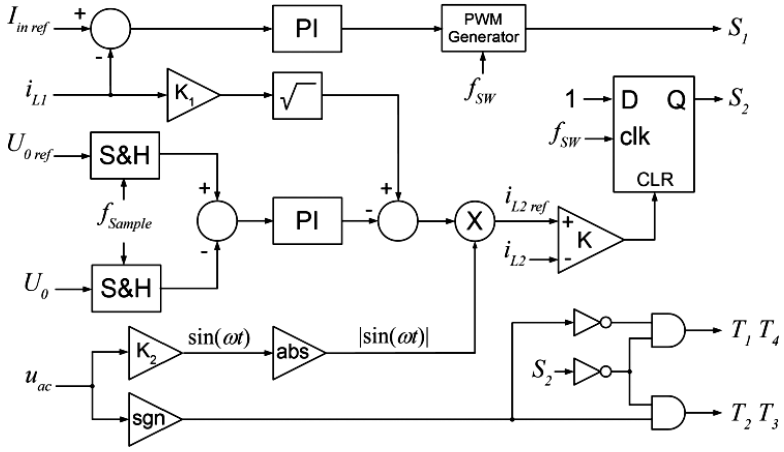
Inequation (6) sets lower boundary condition for decoupling capacitor value satisfying system power decoupling requirements. According to (6) maximizing U_0 voltage level decreases needs for decoupling capacitance. Small values of decoupling capacitance allows usage of film capacitors (e.g. PET or PP), improving converter's reliability and decreasing capacitor volume and cost. On the other hand small capacitance leads to larger voltage stress on switching elements and affect efficiency. Therefore, selection of decoupling capacitance, hence U_0 voltage level, is a multidimensional issue.

3.2. Closed-loop control strategy

In Fig. 3, a block diagram of control algorithm for AC-DC (a) and DC-AC (b) mode of operation is presented.



(a)



(b)

Fig. 3. Control algorithm block diagram: AC-DC (a) and DC-AC (b) systems

In AC-DC mode output voltage U_{out} is compared with its reference level and difference signal is an input for U_{out} PI controller. Controller output signal $i_{L2\ \text{ref}}$ is compared with i_{L2} current. From that comparison transistor's S_2 gate signal is generated. Additionally U_{out} PI controller output signal contains information on DC load level and together with U_0 PI controller output signal is used to generate reference signal ($i_{L1\ \text{ref}}$) for inductor L_1 current and hence transistor's S_1 gate signal.

In DC-AC mode inductor L_1 average current level is regulated. Input current reference level $I_{\text{in ref}}$ is compared with i_{L1} current and difference signal is an input for I_{in} PI controller. Controller output signal is used to generate transistor's S_1 gate signal. Measured instantaneous i_{L1} current level, together with U_0 PI controller output signal contains information of available power in DC source and is used to generate $i_{L2\ \text{ref}}$ signal. From the comparison of $i_{L2\ \text{ref}}$ signal and i_{L2} current, transistor's S_2 gate signal is generated. Thyristor's enable signal (T_1, T_4 and T_2, T_3 pairs) is based on the u_{ac} voltage polarization. Insignificant U_{out} voltage lag and temporary driver signal

blocking (during u_{ac} voltage zero-crossing) allow use of a simple half cycle modulation technique in practical implementation, providing robust solution.

In the proposed solution $\sin(\omega t)$ signal is generated as proportional to u_{ac} voltage. In most cases it will result in i_{ac} current distortion as u_{ac} voltage contains higher order harmonics. A Phase Control Loop (PLL) can be utilized to address this issue, but this involves a more complex practical implementation.

Although the theoretical instantaneous voltage of the decoupling capacitor is known (3) it cannot be used as a reference in practical implementation, hence instantaneous voltage u_{C1} of decoupling capacitor C_1 is not regulated as in classical solutions. Control circuit maintains only the proper level of stabilized voltage value U_0 in u_{C1} voltage. Decoupling capacitor instantaneous voltage u_{C1} is equal to U_0 value twice per $u_{C1}(t)$ period i.e. every 5 ms in 50 Hz system. Hence by measuring u_{C1} instantaneous voltage level in predefined moment of time U_0 level can be obtained. Moments of time when U_0 value can be measured are directly connected with AC system voltage: first measuring event occurs when u_{ac} voltage is zero-crossing and second is when u_{ac} voltage reaches its maximum/minimum value.

By such infrequent U_0 level comparison with $U_{0\text{ref}}$ level controller dynamic is considered low. To maintain robust operation during transient states (i.e. load changes, startup procedure) when controller receives delayed (up to 5 ms) information about changes in U_0 level, the decoupling capacitor must be slightly oversized in comparison with a minimal value obtained from formula (6).

Many topology variants were simulated (all results can be found in [20]) and for experimental verification topologies working in continuous current mode of boost converter and discontinuous current mode of buck-boost converter were chosen (for both AC-DC and DC-AC modes of operation).

4. AC-DC topology experimental results

To validate a proposed topology and control algorithm a laboratory model of 450 W PFC APD rectifier has been built (Fig. 4). Converter specification is given in Table 1.

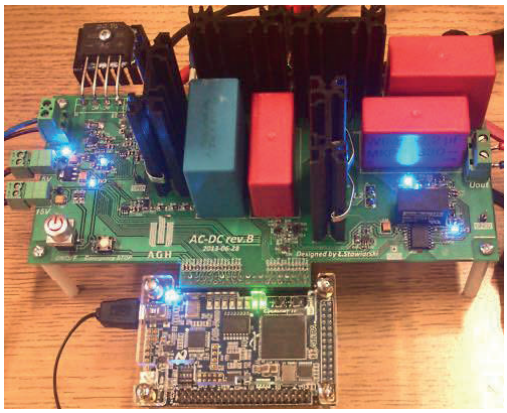


Fig. 4. AC-DC laboratory model

Table 1. AC-DC laboratory model specification

Parameter name	Symbol	Value	Unit
Output power	P_{out}	450	W
Output voltage reference level	$U_{\text{out ref}}$	400	V
Decoupling capacitor stabilized voltage value reference level	$U_{0\text{ref}}$	425	V
Switching frequency	f_{sw}	30	kHz
Output voltage switching component reference level	$\Delta U_{\text{out ref}}$	4	V
Boost converter inductance	L_1	4	mH
Buck-boost converter inductance	L_2	1	mH
Decoupling capacitance	C_1	19.7	μF
Output capacitance	C_2	6.9	μF

The laboratory model was designed to work in inductor L_2 discontinuous current mode. In that mode transistor S_2 is turned-on in Zero Current Switching mode, hence S_2 switching losses are only turn-off losses. Generally MOSFET transistors are characterized by lower turn-off losses than IGBT transistors, therefore SiC MOSFET ROHM SCT2280KE (1.2 kV, 14 A) working as S_2 transistor was chosen. For S_1 switch IGBT transistor International Rectifier IRG4PF50W (900 V; 28 A) was used. In order to minimize diode recovery loss SiC diodes were used: D_1 – GeneSiC Semiconductor C4D08120A (1.2 kV; 7 A), D_2 – Cree C4D08120A (1.2 kV; 11.3 A).

The decoupling capacitance value was based on formula (6). The theoretical value was increased to compensate for component tolerances and provide additional energy backup in transient states. Two polypropylene (PP) capacitors in parallel were used: EPCOS B32776G8156K (15 μF; 800 V) and WIMA MKP4J044707G00KYSD (4.7 μF; 630 V). To maintain switching component in the output voltage – $\Delta U_{\text{out ref}}$ on the desired 1% of average output voltage level, converter's output capacitance is calculated to be 6.9 μF. Two PP capacitors in parallel were used: WIMA MKP4J044707G00KYSD (4.7 μF; 630 V) and MKP4J042207E00KYSD (2.2 μF; 630 V).

The control algorithm is realized in a field-programmable gate array (FPGA) Cyclone IV EP4CE22F17C6N.

During all experiments resistive load (347 Ω) was used.

Fig. 5 shows converter steady state boost inductor current, buck-boost inductor current, decoupling capacitor voltage and rectified input voltage. Decoupling capacitor voltage has ripple of around 202 V and peak value of 510 V and minimum of 308 V. It can be seen a double-line frequency component in u_{C1} voltage.

Fig. 6 shows input/output voltage and current waveforms. Input current is in phase with input voltage resulting in 0.993 PF. Output voltage does not contain double-line frequency ripple which proves proper converter APD operation.

Fig. 7 shows boost inductor current, buck-boost inductor current, decoupling capacitor voltage and rectified input voltage with scope time-base comparable with switching frequency. Buck-

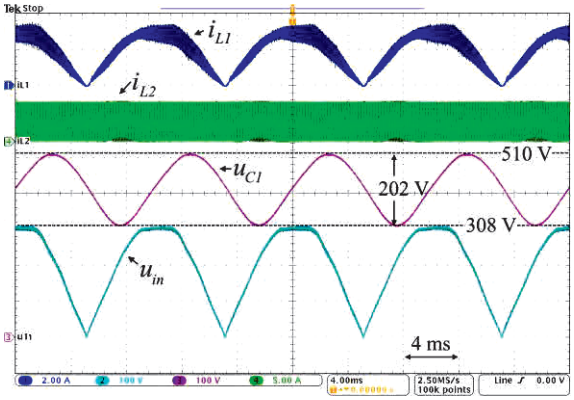


Fig. 5. AC-DC experimental results: boost inductor current $i_{L1}(t)$, buck-boost inductor current $i_{L2}(t)$, decoupling capacitor voltage $u_{C1}(t)$ and rectified input voltage $u_{\text{in}}(t)$

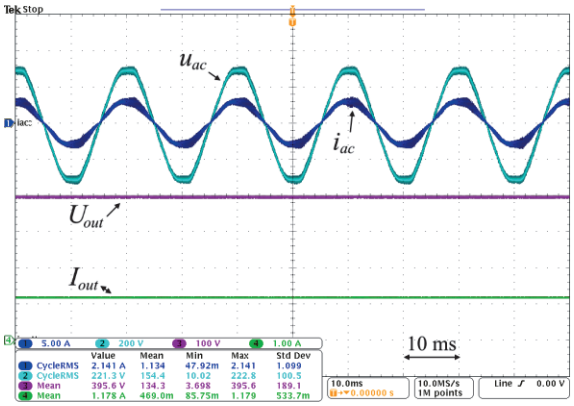


Fig. 6. AC-DC experimental results: input voltage $u_{ac}(t)$, input current $i_{ac}(t)$, output voltage $U_{\text{out}}(t)$ and output current $I_{\text{out}}(t)$

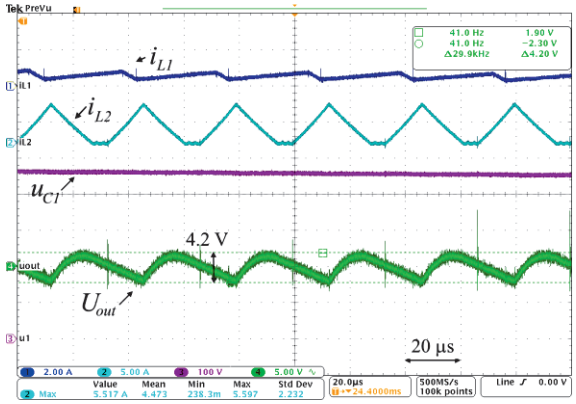


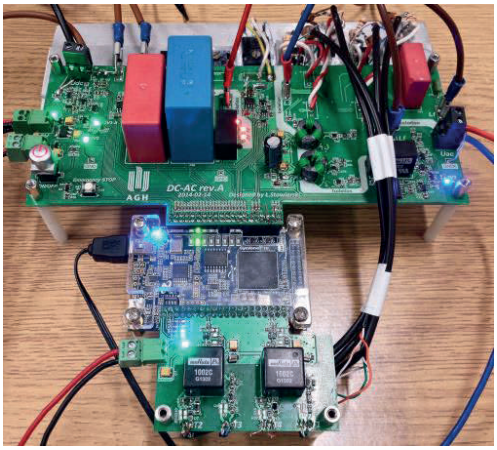
Fig. 7. AC-DC experimental results: boost inductor current $i_{L1}(t)$, buck-boost inductor current $i_{L2}(t)$, decoupling capacitor voltage $u_{C1}(t)$ and output voltage $U_{\text{out}}(t)$ switching component

boost inductor L_2 discontinuous current mode and Boost inductor L_1 continuous current mode operation can be seen. Switching frequency ripple in output voltage is around 4 V which is within specification limit.

The converter working in AC-DC rectifier mode has very high efficiency, reaching 97% (input power 457.4 W and output power 443.8 W) without considering the controller power dissipation. Measurements were conducted with Tektronix DPO 4054 oscilloscope with high-end current (Tektronix TCP0030, TCP01500) and voltage (Testec TT-SI9110, Tektronix P5100) probes. Efficiency/PF was calculated in MATLAB on the measured voltage/current data.

5. DC-AC topology experimental results

To validate the proposed topology and control algorithm a laboratory model of 320 W APD inverter has been built (Fig. 8). Converter specification is given in Table 2.



Fi. 8. DC-AC laboratory model

Table 2. DC-AC laboratory model specification

Parameter name	Symbol	Value	Unit
Input power	P_{in}	320	W
Input voltage	U_{dc}	40	V
Decoupling capacitor stabilized voltage value reference level	$U_{0\text{ref}}$	285	V
Switching frequency	f_{sw}	30	kHz
Input current switching component reference level	$\Delta i_{L1\text{ref}}$	400	mA
Boost converter inductance	L_1	3	mH
Buck-boost converter inductance	L_2	243	μH
AC line filter inductance	L_f	880	μH
Decoupling capacitance	C_1	17.2	μF
AC line filter capacitance	C_f	470	nF

As mentioned in section 3.1 the main field of application for DC-AC mode are single-phase microinverters directly connected to a PV module, hence to address these applications input voltage level was set to 40 V. Therefore, $U_{0\text{ref}}$ value is a compromise between input stage efficiency (lower for high step-up ratios [19]) and decoupling capacity minimization. During experiments the converter was supplied from bench DC power supply and as a load 230 VAC line was used.

Decoupling capacitance value was based on formula (6). The same as in AC-DC rectifier mode, the theoretical value was increased to compensate for component tolerances and provide additional energy backup in transient states. Therefore, two polypropylene (PP) capacitors in parallel were used: EPCOS B32776G8156K (15 μF; 800 V) and WIMA MKP4J042207E00KYSD (2.2 μF; 630 V). For AC line filter PP capacitor WIMA MKP4J034705G00KYSD (470 nF; 630 V) was selected.

The converter in DC-AC mode with specification from Table 2 works with high input current. Pre-analysis showed that the vast majority of S_1 switch power losses are conduction losses. To minimize that part, MOSFET transistor with low R_{DS} was selected: Infineon IPW65R045C7 (650 V, 46 A, 45 mΩ). Other components were selected as: S_2 – IGBT transistor – International Rectifier IRG4PF50W (900 V, 28 A), thyristors – NXP BT152-800R (800 V, 13 A), diodes: D_1 – SiC GeneSiC Semiconductor GB07SHT12-247 (1.2 kV, 7 A), D_3 – IXYS DSEP30-12A (1.2 kV, 30 A).

Fig. 9 shows converter steady state buck-boost inductor current, decoupling capacitor voltage, 230 VAC line current and voltage. Decoupling capacitor voltage has ripple of around 213 V with peak value of 381 V and minimum of 168 V. This can be seen as a double-line frequency component in u_{C1} voltage. 230 VAC line current is in phase with voltage, resulting in 0.991 PF.

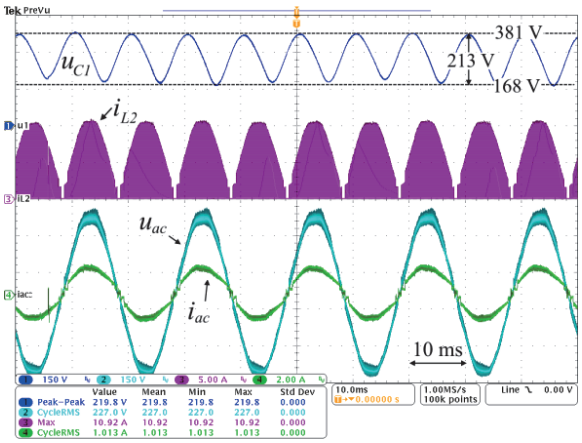


Fig. 9. DC-AC experimental results: decoupling capacitor voltage $u_{C1}(t)$, buck-boost inductor current $i_{L2}(t)$, 230 VAC line current $i_{ac}\ (t)$ and voltage $u_{ac}\ (t)$

Fig. 10 shows decoupling capacitor voltage, boost inductor current, buck-boost inductor current and 230 VAC line current with scope time-base comparable with switching frequency. Input current (i_{L1}) does not contain double-line frequency ripple and switching component of around 400 mA is within specification. This proves proper converter APD operation.

The converter working in DC-AC inverter mode has poor efficiency, reaching merely 73.7% (input power 315.4 W and output power 232.4 W) without considering the controller power

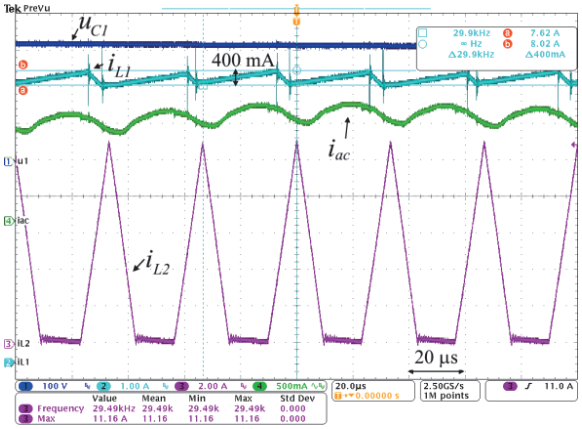


Fig. 10. DC-AC experimental results: decoupling capacitor voltage $u_{C1}(t)$, boost inductor current $i_{L1}(t)$, 230 VAC line current i_{ac} (t) and buck-boost inductor current $i_{L2}(t)$

dissipation. Poor efficiency is mainly caused by high switching losses of S_2 transistor. It can be increased by replacing IGBT transistor with low-switching losses SiC MOSFET transistor, together with replacement of thyristors for devices with higher critical rate of rise of off-state voltage $\mathrm{d}V_D/\mathrm{d}t$. A detailed explanation of this issue can be found in [13, 20].

All measurements were conducted with the same equipment and procedure as for AC-DC mode.

6. Conclusions

This paper presented a novel single-phase APD topology in AC-DC and DC-AC modes. Compared to other APD topologies it utilize classical boost and buck-boost converter topologies but with a different control algorithm. Experimental results confirmed proper Active Power Decoupling using polypropylene capacitors and elimination of double-line frequency components on DC side current/voltage. Further work on DC-AC mode should be conducted regarding power efficiency increase.

Acknowledgements

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