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Medium voltage electrical system research using DSP-based real-time simulator

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The paper presents the results of a simulation of operating conditions of a two-sectioned medium-voltage power line, with the use of a simulator based on a multi-core signal processor. It is a kind of type of a real-time digital simulator of electrical system. Steady states and transients were analyzed, as well as the switching operation of the load with zero initial conditions. The transient states of this electrical system was also analyzed during one and multi phase short-circuit. The oscillograms of steady and transient node system voltages and currents registered during simulator work were presented. The obtained results were compared to the ones received via Matlab simulation package. The estimated maximum errors of the simulator in steady and transition states were presented. The method of simulation, which is used in the implementation of discreet mathematical models of the complex electrical systems in real-time simulators, was applied. The main advantage of the simulator is the ability of its cooperation with real devices (e.g. regulators).

KEYWORDS: simulator working in real-time, DSP processor, simulation of electrical system

1. Introduction

For many years we could observe continuous development of microprocessor and computer technology. It allows for the evolution of the techniques and tools used for simulation in the field of electrical engineering. Due to the decreasing cost of computer technologies and the increase in computing power of processors, it is possible to create a variety of computer systems working as digital simulators of electrical systems. The development of real time simulators and the ability to work with real devices (eg. regulators) is still a valid issue. In [1, 2] a personal computer with multi-core processor and graphics processors was used. By contrast, [3, 4] focuse on DSP-based simulators. The study involved a sample of an electrical system.

The article describes the use of a simulator for the analysis of transient states occurring in the electrical system, consisting of an equivalent generator (MV switchgear in a 110/15 kV transformer station) two-sectioned MV transmission line and reception. This makes it possible to analyze the phenomena occurring randomly. An example of this could be the transient short circuits, of which detection and analysis in a real power system is difficult. In addition, the estimated maximum errors of the simulator in steady and transient states were presented.

2. Real time simulation of electrical systems

Referring to the IEEE [5] standard, it is possible to provide a definition of a simulator operating in real time (SOiRT). It is a digital platform in which calculations are performed simultaneously with the externally occurring process, in order to control, supervise and timely respond to events occurring in this process [5, 6].

Schematic diagram of the SOiRT simulator is shown in Figure 1.

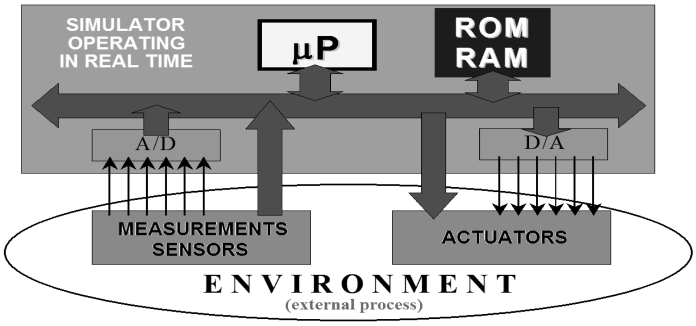

Fig. 1. Schematic diagram of the SOiRT simulator [1]

The main element of the simulator is the processor, which is the computing and controlling unit. As in any computer system, here you can also distinguish the program and data memory. The flow of signals from the external process to the simulator and vice versa is provided by the means of analog-to-digital (A/D) and digital-to-analog (D/A) converters. The sensors and actuators are placed in the external process.

The external process described in the article, runs in a real technical object (eg. a regulator of a reactive power compensation system). It allows to verify the accuracy of the algorithm implemented in the regulator (response to the processes occurring in the electrical system) or to analyze the operating conditions of the electrical system, particularly the transitional processes, taking into account the characteristics of a real regulator (connected to the simulator).

3. Signal processor based simulator

A simplified block diagram of a simulator based on the digital signal processor is shown in Figure 2.

The simulator has been developed on the base of the TMDSEVM6678L development module made by Texas Instruments. The main element of this module is an eight-core TMS320C6678 DSP processor. In addition, the module contains JTAG interface of XDS100 type, and numerous memory chips. Here it is possible to distinguish 512 MB of DDR3 RAM external dynamic memory and FLASH memory [7]. The computational power of a single core is 20 GFLOPS at a core clock frequency of 1.25 GHz. The given computational power is achieved by performing up to eight instructions in parallel. It is possible because single core of the C66XX processor includes several ALU computational units. This allows you to perform parts of the calculation parallelly in a single core. In addition, the processor supports 32-bit fixed and floating-point calculations (single precision) and 64-bit floating-point calculations (double precision). The parallel computing is supported here, including the classical support of the shared memory and hardware synchronization mechanisms [8].

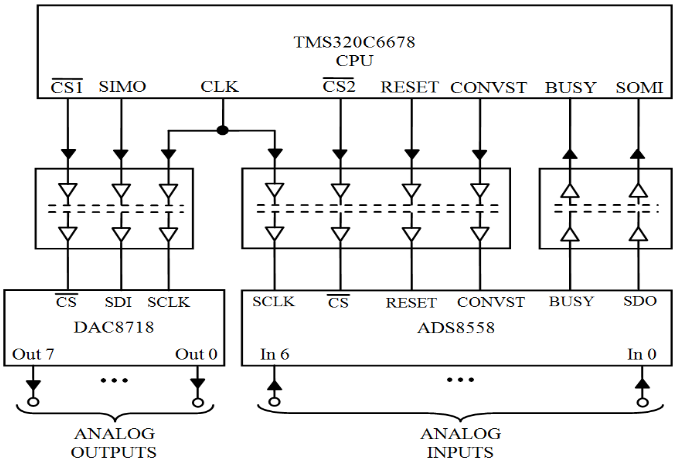

Fig. 2. Simplified block diagram of the simulator [3]

The communication with external devices was implemented with the use of an SPI hardware interface (Serial Peripheral Interface). This interface can work with a maximum clock frequency of 66 MHz and the data frame length in the range from two to sixteen bits [9]. The choice of peripherals was made via the CS1 and CS2 line.

The analog outputs use a 16-bit, 8-channel Digital/Analog D/A DAC8718 type converter. Symmetrical power supply, reference voltage of 2.5 V and a amplification of 6 was used. This allows to obtain changes in the output voltage ranging from -7.5 V to 7.5 V. The maximum operating frequency of the D/A SPI interface is 50 MHz [10]. In order to simplify the hardware part of the system the two-way communication was abandoned. The D/A converter allows to enter the selected signals into the real object working with the simulator.

In contrast, analog inputs were created through a 16-bit, six-channel analog/digital (A/D) ADS8558 type converter. The ADS8556 contain six successive approximation register (SAR) based analog-to-digital converters (A/D) with true bipolar inputs. Each channel contains a sample-and-hold circuit that allows simultaneous high-speed multi-channel signal acquisition. The additional control lines are essential here. RESET signal sets the converter to the initial state, while the line CONVST begins the process of sampling and converting the analog input signal. BUSY line can generate an interrupt to inform the processor about the end of the conversion [11]. This system configuration is adapted to the standard range of input voltages from -10 V to +10 V.

In order to ensure galvanic isolation an ISO7240M system was used between the processor and audio A/D and D/A converters. ISO7240M system is a quadruple optical isolator, which can operate at a maximum bitrate of 150 Mb/s [12].

4. Mathematical model of the analyzed system

The analyzed electrical system consists of a equivalent generator (MV switchgear in a 110/15 kV transformer station) - structural element ES1, two-sectioned MV power transmission line - structural elements ES2 - ES6 and the MV concentrated MV reception - structural element ES7. The power line model is the classical model of type π, with RL longitudinal branches and C transverse branches. In developed model serially with capacitors using for representing capacitance to ground and capacitances between phase wires was inserted in series connected resistors and inductors.

Presented mathematical model is based on multipole method which is one of the many known methods of modelling of electric circuits. In this method electric circuit is analyzed as n structural elements (SE) connected each other. On Figure 3 was presented internal structurals of multipoles using for created model of analyzed circuit.

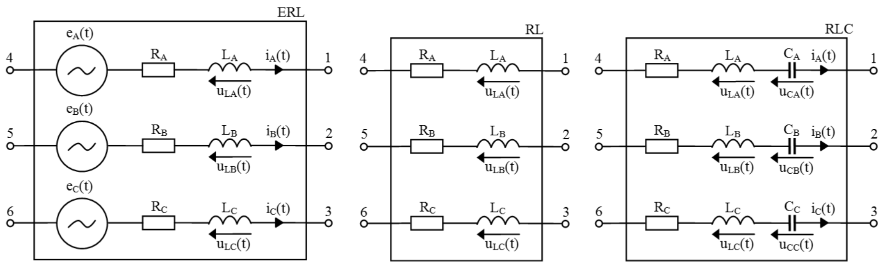

Fig. 3. Internal structurals of multipoles using for created model of power line

In this case structural elements are represent by six-terminal network (multipole). It is possible to specify internal structural types of ERL, RL and RLC depending on elements contained in following branches.

Model without LC elements was used. This kind of model is understood as a resistance model with currents sources. It is created by approximation differential equations which describe capacitance and inductance by selected algorithm of numerical integration. In their research, the author used the trapezoidal numerical integration algorithm [1].

In Figure 4 an equivalent schematic diagram of analyzed circuit with following structural element was explained.

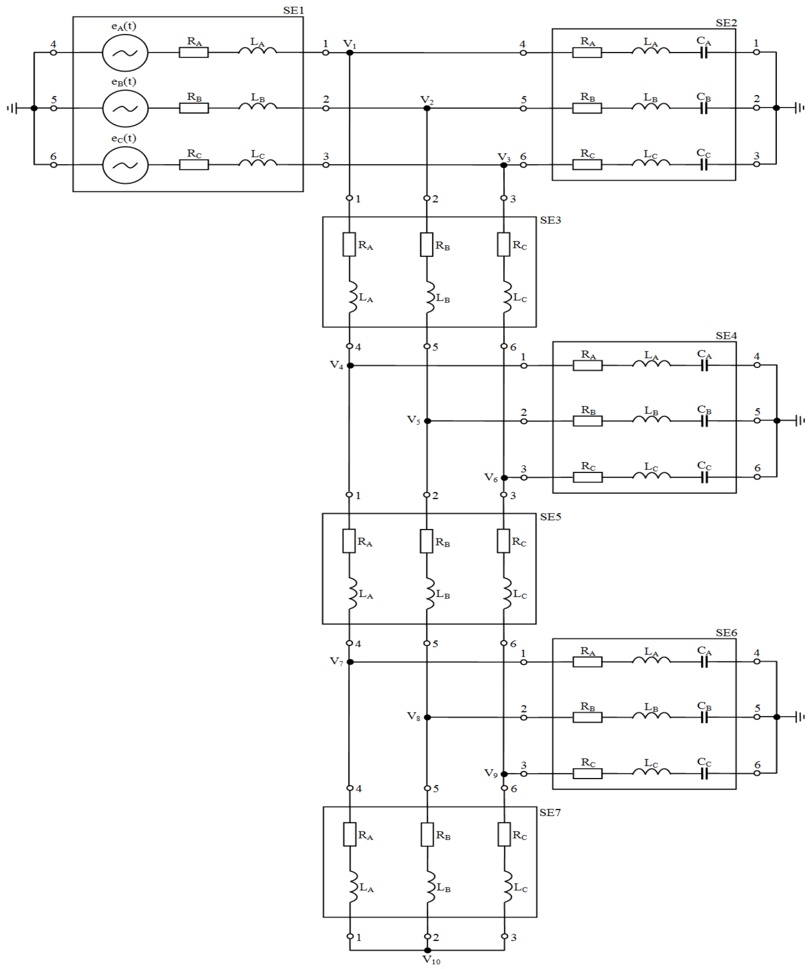

Fig. 4. Equivalent schematic diagram of analyzed circuit

This circuit consists of seven three-phased structural elements (SE1 – SE7). The element SE*k* is presented in the form of a multipole, for which the vector of potential external nodes can be explained

$$\boldsymbol{v}_{\mathrm{SE}k} = \left[v_{1\mathrm{SE}k} \quad v_{2\mathrm{SE}k} \quad v_{3\mathrm{SE}k} \quad v_{4\mathrm{SE}k} \quad v_{5\mathrm{SE}k} \quad v_{6\mathrm{SE}k} \right]^{\mathrm{T}}, \tag{1}$$

where: $v_{1\mathrm{SE}k}$, $v_{2\mathrm{SE}k}$, $v_{3\mathrm{SE}k}$, $v_{4\mathrm{SE}k}$, $v_{5\mathrm{SE}k}$, $v_{6\mathrm{SE}k}$ – potential of external nodes k-th structural element, as well as vector of external branches currents of element SEk

$$\boldsymbol{i}_{\mathrm{SE}k} = \begin{bmatrix} i_{1\mathrm{SE}k} & i_{2\mathrm{SE}k} & i_{3\mathrm{SE}k} & i_{4\mathrm{SE}k} & i_{5\mathrm{SE}k} & i_{6\mathrm{SE}k} \end{bmatrix}^{\mathrm{T}}, \tag{2}$$

where: $i_{1\mathrm{SE}k}$, $i_{2\mathrm{SE}k}$, $i_{3\mathrm{SE}k}$, $i_{4\mathrm{SE}k}$, $i_{5\mathrm{SE}k}$, $i_{6\mathrm{SE}k}$ – currents of external branches k-th SE.

Mathematical model of SEk element has to be realized in a way that allows to create the external vector equation as follows [1]

$$\boldsymbol{i}_{\mathrm{SE}k} + \boldsymbol{A}_{\mathrm{SE}k}\boldsymbol{v}_{\mathrm{SE}k} + \boldsymbol{B}_{\mathrm{SE}k} = \boldsymbol{0}, \tag{3}$$

where: $\boldsymbol{A}_{\mathrm{SE}k}$ – square matrix with size 6×6; $\boldsymbol{B}_{\mathrm{SE}k}$ – 6-element column matrix. Elements of matrices $\boldsymbol{A}_{\mathrm{SE}k}$ and $\boldsymbol{B}_{\mathrm{SE}k}$ used in (3) are defined by parameters and physical quantities inside SEk element.

Terminals of individual structural elements SE are connected in eleven nodes of electric circuit. Potential of one of these node equals zero. Therefore for remaining ten external nodes a vector of potential of electric circuit can be created

$$\boldsymbol{v}_{\mathrm{S}} = \begin{bmatrix} v_{1\mathrm{S}} & v_{2\mathrm{S}} & v_{3\mathrm{S}} & v_{4\mathrm{S}} & v_{5\mathrm{S}} & v_{6\mathrm{S}} & v_{7\mathrm{S}} & v_{8\mathrm{S}} & v_{9\mathrm{S}} & v_{10\mathrm{S}} \end{bmatrix}^{\mathrm{T}}, \tag{4}$$

where: $v_{1\mathrm{S}}$, $v_{2\mathrm{S}}$, $v_{3\mathrm{S}}$, $v_{4\mathrm{S}}$, $v_{5\mathrm{S}}$, $v_{6\mathrm{S}}$, $v_{7\mathrm{S}}$, $v_{8\mathrm{S}}$, $v_{9\mathrm{S}}$, $v_{10\mathrm{S}}$ – independent potential nodes of circuit.

Connection between potential of external nodes SE and potential nodes of circuit can be described using a matrix transpose in relation to the incidence matrix $\boldsymbol{P}_k$ k-th element [1]

$$\boldsymbol{v}_{\mathrm{SE}k} = \boldsymbol{P}_k^{\mathrm{T}}\boldsymbol{v}_{\mathrm{S}}. \tag{5}$$

Matrix $\boldsymbol{P}_{\mathrm{k}}$ using in (5) is constant for individual element. Number of rows is equal to numbers of independent nodes of electric circuit. Whereas number of columns is equal to numbers of branches individual SE. It means in analyzed example size of matrices $\boldsymbol{P}_{\mathrm{k}}$ is 10×6. After using Kirchhoff's current law for all independent nodes of circuit following equation can be created

$$\sum_{k=1}^{7}\boldsymbol{P}_k\boldsymbol{i}_{\mathrm{SE}k} = \boldsymbol{0}. \tag{6}$$

After determining current values of external branches of multipoles using (3) and substitution this values to (6) as well as using (5) nodal equation of circuit can be created [1]

$$\boldsymbol{A}_{\mathrm{S}}\boldsymbol{v}_{\mathrm{S}} + \boldsymbol{B}_{\mathrm{S}} = \boldsymbol{0}, \tag{7}$$

where:

$$\boldsymbol{A}_{\mathrm{S}} = \sum_{k=1}^{7}\boldsymbol{P}_k\boldsymbol{A}_{\mathrm{SE}k}\boldsymbol{P}_k^{\mathrm{T}}, \tag{8}$$

$$\boldsymbol{B}_{\mathrm{S}} = \sum_{k=1}^{7}\boldsymbol{P}_k\boldsymbol{B}_{\mathrm{SE}k}. \tag{9}$$

In case when element SEk is six-terminal network (multipole) matrix $\boldsymbol{A}_{\mathrm{SE}k}$ is getting by [1]

$$\boldsymbol{A}_{\mathrm{SE}k} = \begin{bmatrix} \boldsymbol{a}_{\mathrm{SE}k} & -\boldsymbol{a}_{\mathrm{SE}k} \\ -\boldsymbol{a}_{\mathrm{SE}k} & \boldsymbol{a}_{\mathrm{SE}k} \end{bmatrix}, \tag{10}$$

where:

$$\boldsymbol{a}_{\mathrm{SE}k} = \begin{bmatrix} \alpha_{\zeta\mathrm{SE}k} & 0 & 0 \\ 0 & \alpha_{\zeta\mathrm{SE}k} & 0 \\ 0 & 0 & \alpha_{\zeta\mathrm{SE}k} \end{bmatrix}, \tag{11}$$

where: ζ – number of individual SE branches (in this case ζ = 1, 2, 3).

In this case matrix $\boldsymbol{B}_{\mathrm{SE}k}$ is as follow [1]

$$\boldsymbol{B}_{\mathrm{SE}k} = \begin{bmatrix} \boldsymbol{b}_{\mathrm{SE}k} \\ -\boldsymbol{b}_{\mathrm{SE}k} \end{bmatrix}, \tag{12}$$

where:

$$\boldsymbol{b}_{\mathrm{SE}k} = \begin{bmatrix} \beta_{\zeta\mathrm{SE}k} \\ \beta_{\zeta\mathrm{SE}k} \\ \beta_{\zeta\mathrm{SE}k} \end{bmatrix}, \tag{13}$$

where: ζ – number of individual SE branches (in this case ζ = 1, 2, 3).

Physical quantities $\alpha_{\zeta\mathrm{SE}k}$ and $\beta_{\zeta\mathrm{SE}k}$ depend on internal structurals and physical parameters of individual SEk. Equations that are necessary for calculating $\alpha_{\zeta\mathrm{SE}k}$, $\beta_{\zeta\mathrm{SE}k}$ as well as physical quantities inside structurals elements SE are combined below with internal structurals.

Element type of ERL (SE1) [1]:

$$e_{\zeta\mathrm{SE}k}(t_n) = E_{\mathrm{m}\zeta\mathrm{SE}k} \sin(2\pi f t_n + \varphi_{\zeta\mathrm{SE}k}), \tag{14}$$

$$\alpha_{\zeta\mathrm{SE}k} = (R_{\zeta\mathrm{SE}k} + \xi^{-1} L_{\zeta\mathrm{SE}k}), \tag{15}$$

$$\beta_{\zeta\mathrm{SE}k} = \alpha_{\zeta\mathrm{SE}k}\left(-e_{\zeta\mathrm{SE}k}(t_{n+1}) - u_{\mathrm{L}\zeta\mathrm{SE}k}(t_n) - L_{\zeta\mathrm{SE}k}\xi^{-1} i_{\zeta\mathrm{SE}k}(t_n)\right), \tag{16}$$

$$u_{\mathrm{L}\zeta\mathrm{SE}k}(t_{n+1}) = L_{\zeta\mathrm{SE}k}\xi^{-1}\left(i_{\zeta\mathrm{SE}k}(t_{n+1}) - i_{\zeta\mathrm{SE}k}(t_n)\right) - u_{\mathrm{L}\zeta\mathrm{SE}k}(t_n), \tag{17}$$

where: ξ =0,5h; h – software integration step; ζ – A, B, or C for following phase of SEk; t_{n+1} – next moment of time; t_n – actual moment of time; $E_{\mathrm{m}\zeta\mathrm{SE}k}$ – amplitude of voltage source; f – frequency; $\varphi_{\zeta\mathrm{SE}k}$ – initial phase;

Element type of RLC (SE2, SE4, SE6) [1]:

$$\alpha_{\zeta\mathrm{SE}k} = \left(R_{\zeta\mathrm{SE}k} + \xi^{-1} L_{\zeta\mathrm{SE}k} + \xi C_{\zeta\mathrm{SE}k}^{-1}\right)^{-1}, \tag{18}$$

$$\beta_{\zeta\mathrm{SE}k} = \alpha_{\zeta\mathrm{SE}k}\left(u_{\mathrm{C}\zeta\mathrm{SE}k}(t_n) - u_{\mathrm{L}\zeta\mathrm{SE}k}(t_n) - \left(L_{\zeta\mathrm{SE}k}\xi^{-1} - \xi C_{\zeta\mathrm{SE}k}^{-1}\right) i_{\zeta\mathrm{SE}k}(t_n)\right), \tag{19}$$

$$u_{\mathrm{C}\zeta\mathrm{SE}k}(t_{n+1}) = \xi C_{\zeta\mathrm{SE}k}^{-1}\left(i_{\zeta\mathrm{SE}k}(t_{n+1}) + i_{\zeta\mathrm{SE}k}(t_n)\right) + u_{\mathrm{C}\zeta\mathrm{SE}k}(t_n), \tag{20}$$

$$u_{\mathrm{L}\zeta\mathrm{SE}k}(t_{n+1}) = L_{\zeta\mathrm{SE}k}\xi^{-1}\left(i_{\zeta\mathrm{SE}k}(t_{n+1}) - i_{\zeta\mathrm{SE}k}(t_n)\right) - u_{\mathrm{L}\zeta\mathrm{SE}k}(t_n). \tag{21}$$

Element type of RL (SE3, SE5, SE7) [1]:

$$\alpha_{\varsigma \mathrm{SE}k} = \left(R_{\varsigma \mathrm{SE}k} + \xi^{-1} L_{\varsigma \mathrm{SE}k}\right)^{-1}, \tag{22}$$

$$\beta_{\varsigma \mathrm{SE}k} = \alpha_{\varsigma \mathrm{SE}k}\left(-u_{\mathrm{L}\varsigma \mathrm{SE}k}(t_n) - L_{\varsigma \mathrm{SE}k}\xi^{-1} i_{\varsigma \mathrm{SE}k}(t_n)\right), \tag{23}$$

$$u_{\mathrm{L}\varsigma \mathrm{SE}k}(t_{n+1}) = L_{\varsigma \mathrm{SE}k}\left(i_{\varsigma \mathrm{SE}k}(t_{n+1}) - i_{\varsigma \mathrm{SE}k}(t_n)\right) - u_{\mathrm{L}\varsigma \mathrm{SE}k}(t_n). \tag{24}$$

The developed mathematical model of example electric circuit was implemented in digital simulator of electric circuit which was described briefly in point 3.

5. Analyzed electrical circuit simulation algorithm

In Figure 5 the author presents a mathematical modeling algorithm of analyzed electric circuit with the use of a model described in point 4, which was implemented in hardware structure explained in point 3. Research was carried out with the use of sequential computing based on one core of the processor. A.1 block is used for input data. It means the memory is initialized by values relating to parameters and physical quantities inside structural elements. Block A.2 realizes calculating values which are constant in the simulation process. It is necessary to distinguish differences between calculating time and software integration step. First is the time of executing calculating blocks from A.4 up to A.11. Second is the integration step of differential equations of mathematical model of electric circuit, which obviously depend of summing calculating time and time consumption for communicating with D/A converter. A.3 block is used for the configuration of the processor and peripheral devices. Clock rate of cores of the processor type TMS320C6678 is equal to 1 GHz. It is using real time operating DSP/BIOS from Texas Instruments. The time variable *t* is increasing in each iteration by value of software integration step *h*. RTI module (Real Time Interrupt) inside the structural of using processor is responsible for the software integration step. This module was configured for call periodically interrupt every time *h* (conditional operation W.1). There is a global variable set up in the subroutine of this interrupt. It causes the start of calculation inside main loop of program. Afterwards blocks A.4 and A.5 are realized using equations (5) and (3). In computing block A.6 internal physicals quantities of SE are determined, such as voltages on capacitors and inductors based on equations (17), (20), (21) and (24).

A.8 and A.9 blocks are responsible for calculating elements of matrixes $\boldsymbol{A}_\mathrm{S}$ and $\boldsymbol{B}_\mathrm{S}$ using calculation formulas (8) and (9). Final calculating block is A.10 which is used for numerical solving of linear equation system (7). In articles [3, 4] the simplest method for solving equation (7) was used. It was factorization of main matrix AS of linear equation system for lower triangular matrix L and upper triangular matrix U (LU factorization). This linear equations systems (for matrices L and U) was afterwards solved by forward and backward substitution algorithms. Factorization was carried out with the use of Doolittle's algorithm [13].

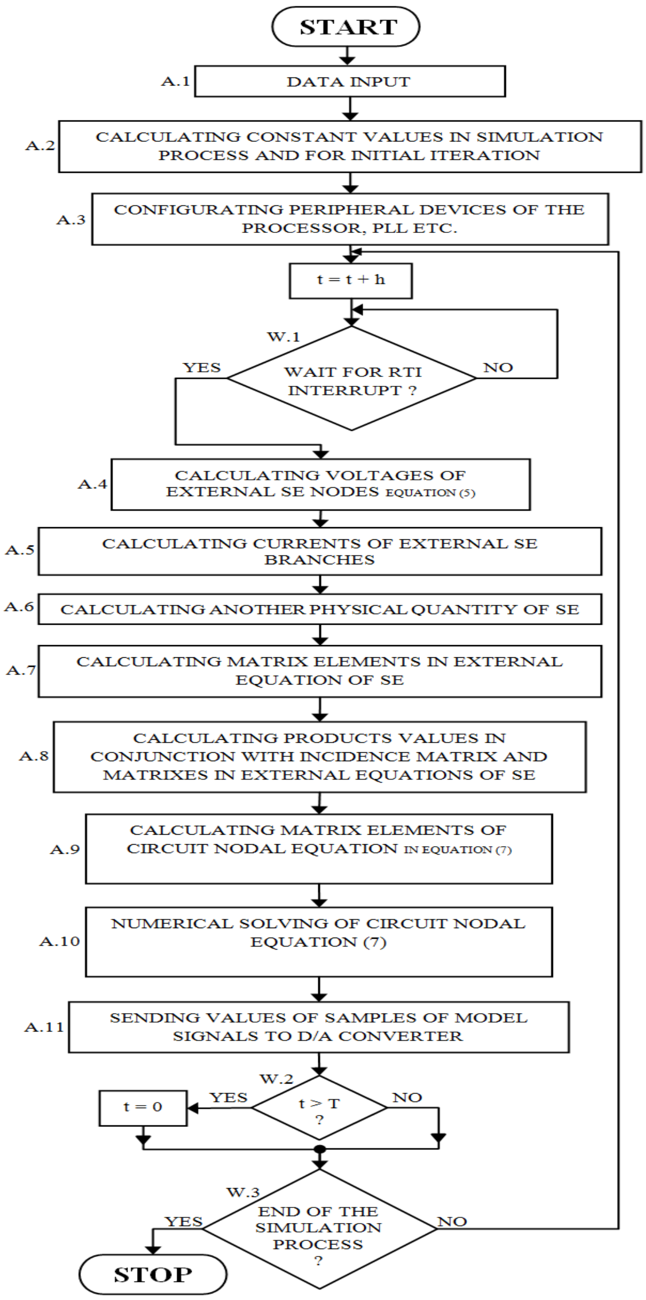

Fig. 5. Mathematical modeling algorithm of electric circuit [4]

In this article, aside from methods used previously, the Gauss-Seidel iteration method was used. Iteration methods for solving linear equation systems can achieve high performance in case of sparse matrix for main matrix of linear equations. For such method it is required to execute N iteration for improving initial solution for one iteration of electric circuit. In presented model matrix $\boldsymbol{A}_S$ consists of 100 elements. This matrix can be considered as sparse because only 28 elements are different than zero. In order to achieve high performance of iteration methods it is necessary special representation of matrix $\boldsymbol{A}_S$ without zero elements. In this case is using coordinate format. It means matrix $\boldsymbol{A}_S$ is represent by three vectors $\boldsymbol{I}$, $\boldsymbol{J}$, $\boldsymbol{V}$. Length of this vectors is equal to number of non zero elements. Vector $\boldsymbol{I}$ contains the rows numbers of nonzero elements, while the vector $\boldsymbol{J}$ column numbers. The last of the vectors $\boldsymbol{V}$ contains values of nonzero elements. Basic version of coordinate format does not require organized registration. Because in every iteration of the iterative method is required $\boldsymbol{A}_S$ matrix multiplication by the vector of initial solution is better stored in $\boldsymbol{V}$ the nonzero elements of the following rows. Such a multiplication algorithm makes iterative methods especially performance in the case of sparse matrices. It is achieve by to avoid multiplications by zero elements. As an initial solution vector used nodal voltages $\boldsymbol{V}_S$ from the previous iteration of the model. Therefore first iteration uses as an initial solution vector $\boldsymbol{V}_S$ filled with zeros. The calculation is terminated after reaching a predetermined number of iterations.

Due to increase the time variable t in each iteration by the value of the software integration step h it causes value of t can theoretically reaches infinity. It should be noted that the periodic signals are generated, so a conditional operation block W.2 can determine when a variable t exceeds period T of the signals occurring in the model. If it happens variable t is reset to zero. Calculations are executing up to end of the simulation. It is schematically illustrated as W.3 block. It can be association with expired time of simulation defined in A.2 block.

The last of blocks is A.11. It corresponds for sending signals of instantaneous values the specified signals of model to the D/A converter.

Source code of a program was developed in C language and compiled in Code Composer Studio 5.5 environment from Texas Instruments.

6. Experimental research

In Table 6.1. was combined parameter of elements of electric circuit (Fig. 4) which are using in experimental research. Value of integration step h is equal to 110 μs. This value of integration step was to chosen for possibility working model in real time. It is widely described in section 6.1.

Whereas parameters of voltage sources inside the SE1 element was shown in Table 6.2. This parameters to meet the conditions in three phase balanced networks of medium voltage and frequency 50 Hz.

Table 6.1. Parameters of structural elements

Structural element	Typ	$R_{\zeta ESk}$ [Ω]	$L_{\zeta ESk}$ [mH]	$C_{\zeta ESk}$ [nF]
ES1	ERL	0,195	6,21	-
ES2	RLC	0,01	1,00	36,5
ES3	RL	1,32	3,63	-
ES4	RLC	0,01	1,00	72,0
ES5	RL	2,64	7,26	-
ES6	RLC	0,01	1,00	36,5
ES7	RL	104	141	-

Table 6.2. Parameters of voltage sources of element SE1

$E_{m\zeta ES1}$ [V]	f [Hz]	φ_{AESk} [rad]	φ_{BESk} [rad]	φ_{CESk} [rad]
12247,4487	50	0	$-\frac{2\pi}{3}$	$\frac{2\pi}{3}$

During carry out research was analyzed nodal voltages of electric circuit and currents of external branches of element SE7. This signals was to put out to the environment of simulator by using D/A converters. Due to the acceptable output voltage range of D/A converter signals representing nodal voltages was divided by 1700 before sending procedure. Analyzed currents was converted to voltages signals using coefficient equal to 0,017 Ω. Given coefficients was calculated for achieve full scale of outputs voltages D/A converter. Measurements was carry out using Rigol DS1104B oscilloscope.

6.1. Calculation time for DSP processor

Comparison calculation times was carried out for LU factorization and Gauss-Seidel methods for solving linear equation system (7). Floating point computing was made for single-precision and double-precision floating point number representation. Table 6.3 include combination of calculation times for previously described cases. This times to pertain consecutive ten iterations of the model. In case of Gauss-Seidel iteration method constant number of twelve iteration improving initial solution was using.

In the case of double-precision computing is possible to obtain time for an iterative method lower by 13,545 μs than time for the LU factorization method. However for single-precision computing is to obtain time decrease time of computing by 5,729 μs. Whereas in the case of single-precision computing is to obtain decrease time of calculating by 5,729 μs. The difference between these values are causes by different computational complexity of using algorithms and more time for executing a double-precision arithmetic operations. Referring to times combined in Table 6.3, times the data transfer to the D/A converter and other delays existing in the DSP it is possible to achieve the previously specified software integration step amounting to 110 μs. Time fluctuations in following iterations are cases by working of operational system DSP/BIOS.

Table 6.3. Combination of the calculating time

Method's name	LU factorization – double precision computing	Gauss-Seidel - double precision computing	LU factorization – single precision computing	Gauss-Seidel - single precision computing
Calculation time of individual iteration	78,474	64,983	67,818	62,046
	78,511	64,618	67,817	61,612
	78,021	65,059	67,408	62,046
	78,427	65,014	67,405	61,612
	78,424	64,613	67,820	62,055
	78,424	65,316	67,409	62,043
	78,422	65,004	68,174	62,031
	78,794	65,030	67,406	62,043
	78,848	65,030	67,772	61,617
	78,388	64,613	67,409	62,042
Mean calculation time	78,473	64,928	67,644	61,915

6.2. Experimental accuracy estimation of simulation results

Accuracy estimation of simulation results was carried out for previously described methods for solving linear equations systems as well as single-precision and double-precision computing. Furthermore was analyzed accuracy computing for steady state and transition sates. In case transition states was chosen transition short circuit state. One phase short circuit in phase A of structural element SE7 as well as multiple phase short circuit was analyzed.

Signals recording was started after 500 ms from beginning simulation. As well as after that time transient states was to produced. Transient momentary short circuit duration was 40 ms. Whereas value of resistance in short-circuited branch was equal 2,00 Ω and value of inductance 141 mH. Waveforms and values of some variables was analyzed. It was nodal voltages of circuit $V_{S1} \ldots V_{S9}$ and currents of external branches of element SE7.

Errors of all variables was obtained as follows:

$$\delta_j = \max\left(\frac{\left|a_{\mathrm{jB}}(t) - a_{\mathrm{j}}(t)\right|}{\max\left(\left|\boldsymbol{A}_{\mathrm{jB}}\right|\right)}\right), \tag{25}$$

where: a_{jB}(t) – calculated instantaneous value j-th variable of base results; a_{j}(t) – calculated instantaneous value j-th variable; $\boldsymbol{A}_{\mathrm{jB}}$ – vector of base values of j-th variable.

Instantaneous values of base variables as well as instantaneous values of model variables was calculated in Borland Builder C++ environment with using as digital platform PC computer. In the same environment was also calculated values of maximal errors based on (25). It uses the model implementation for DSP processor using the portability of code in C. Carry out research by this method is possible due to the no of significant differences in the results of calculations for the PC and the DSP. In the case of calculating the instantaneous values of variables software integration step was 110 µs. Justification for the selection of this value is given in section 6.1. Whereas base variables were determined for 1 µs integration step, double-precision calculations and LU factorization method for solving a system of linear equations (7). For comparative purposes have been taken into account at 110-th the value of the base variable. In Figure 6 maximal errors calculated base on (25) was shown for steady state.

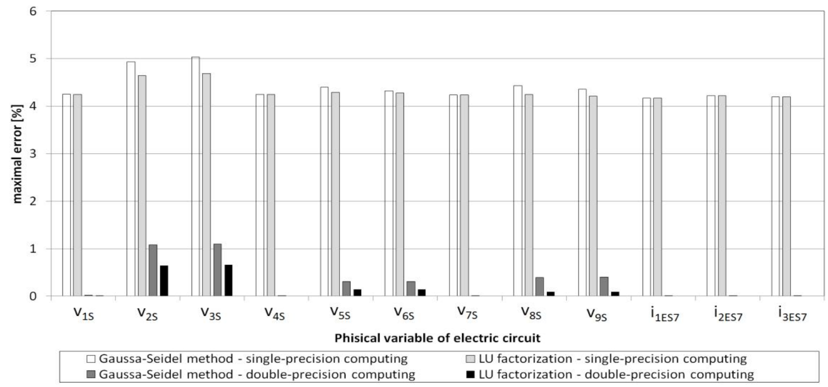

Fig. 6. Maximal errors for model variables in steady state

Afterwards on Figure 6 was shown maximal errors for one phase momentary short circuit. Whereas on Figure 7 was explained maximal errors for transient multiple phase short circuit.

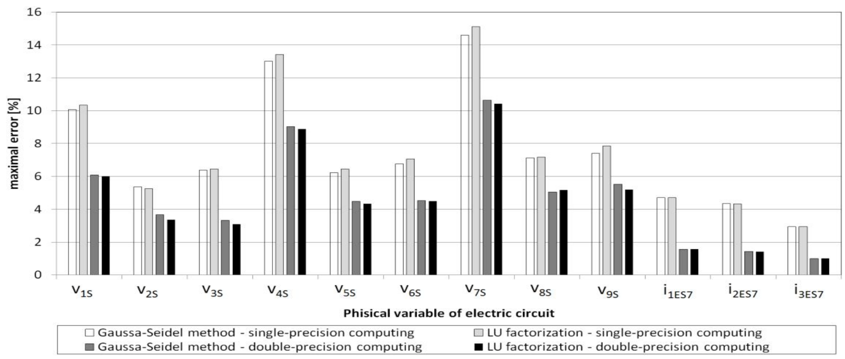

Fig. 7. Maximal errors for model variables in one phase transient short circuit

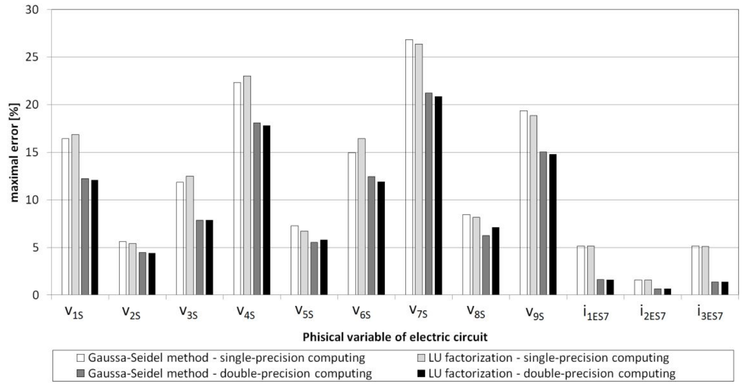

Fig. 8. Maximal errors for model variables in multiple phase transient short circuit

Calculation errors obtained for an iterative Gauss-Seidel and LU factorization method are similar (Fig. 6, 7 and 8). Using double-precision computing can reduce significantly values of errors (Fig. 6, 7 and 8). It relates in particular to the steady state (Fig. 6). Values of the error present in the transient state are much larger than in steady states. It is caused by larger changes the values of variables in the transient states between following iterations.

6.3. Steady state

Figure 8 shown some of the waveforms nodal voltages (Fig. 9a) and currents of external branches structural element SE7 (Fig. 9b) in steady state.

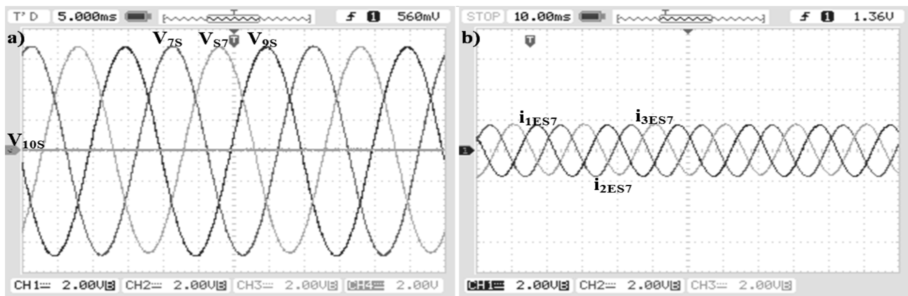

Fig. 9. Waveforms in steady states, a) some of the nodal voltages (3400V/div),
b) currents of external branches of structural element SE7 (120A/div)

Noticeable sinusoidal signals are shown with phase shift each other of angle to point in Table 6.2. Because simulated electric circuit is balanced (Tab. 6.1) that potential v_{10S} reaches zero value.

In order to verify the proper operation of developed digital simulator of the electrical circuit, a suitable simulation in Matlab was also carried out. This simulation was carried out with using the same methods like in digital simulator based on the signal processor. Figure 10 shows simulation results from Matlab.

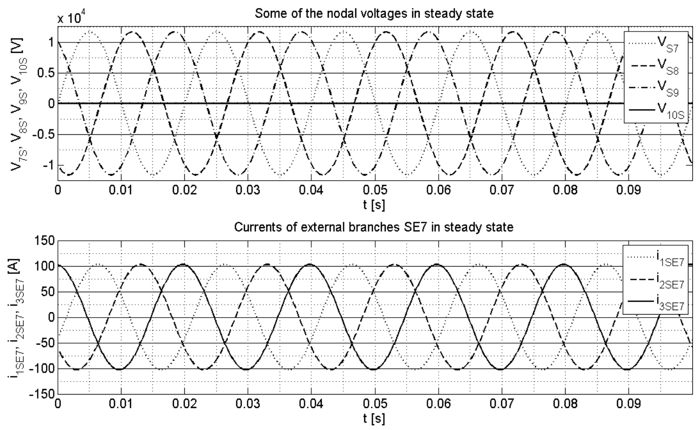

Fig. 10. Waveforms of some nodal voltages and currents of external branches SE7 (Matlab simulation)

After comparing the experimental results with results from simulator based on DSP it can be concluded that there are no significant differences between the instantaneous values in steady state. This proves the satisfactory adequacy of the simulation using a digital simulator developed for exemplary electric circuit.

6.4. Transient states

In Figure 11 was presented waveforms of currents of external branches SE7 element in to switch on load in programmed time. In this experiment first step was to switch on equivalent generator modeling by SE7 element. Second step was to switch on load SE7 after 500 ms from start of the simulation.

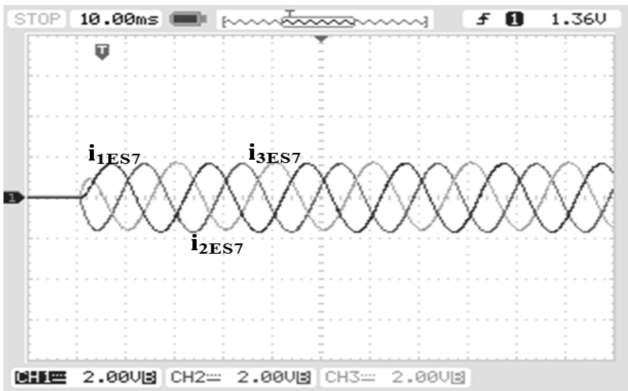

Fig. 11. Current waveforms of external branches SE7 in to switch on load state (120A/div)

Figure 12 shows some of the waveforms nodal voltages (Fig. 12a) and currents of external branches structural element SE7 (Fig. 12b) in one phase momentary short circuit in programmed time. Short circuit is created in phase A of SE7 element after 500 ms from start of the simulation. Transient momentary short circuit duration was 40 ms. In that time value of resistance R_{ASE7} = 2,00 Ω, a inductance of L_{ASE7} = 141 mH.

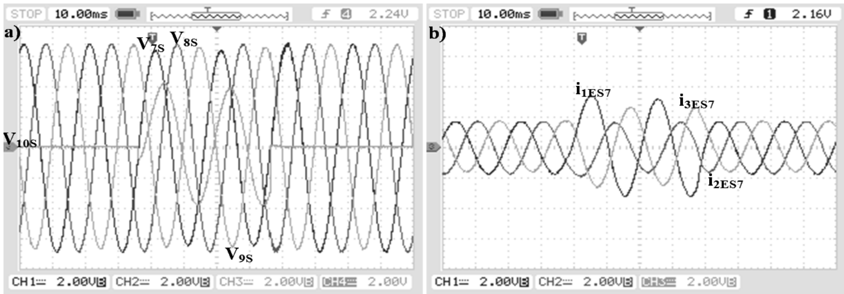

Fig. 12. Waveforms in one phase transition short circuit, a) some of the nodal voltages (3400V/div), b) Currents of external branches of structural element SE7 (120A/div)

Due to no grounding of node number 10 there are changes currents in other phases SE7 element. Furthermore imbalance causes v_{10S} potential reaches values greater than zero during the short circuit.

The last considered transient state was multiple phase transition short circuit in programmed time. Short circuit is created in all phases of SE7 element after 500 ms from start of the simulation (Fig. 13). Transient momentary short circuit duration was 40 ms. In that time value of resistance equals 2,00 Ω, and the inductance 141 mH in all branches of SE7 element.

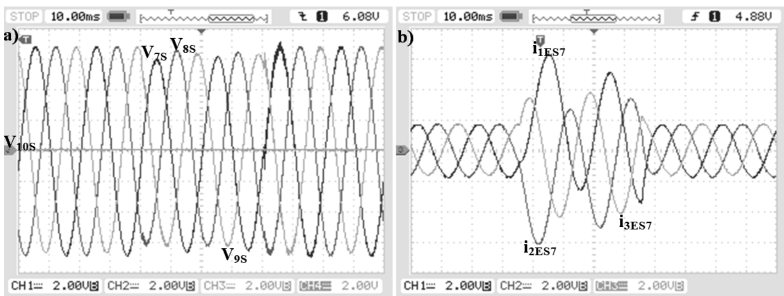

Fig. 13. Waveforms in multiple phase transition short circuit, a) some of the nodal voltages (3400V/div), b) Currents of external branches of structural element SE7 (120A/div)

In this case potential v_{10S} is zero all the time. It is caused by balanced during simulation of transient short circuit.

In this case as well, in order to verify the results a simulation in Matlab was carried out. In Figure 14 was presented waveforms of currents of external branches SE7 element in to switch on load.

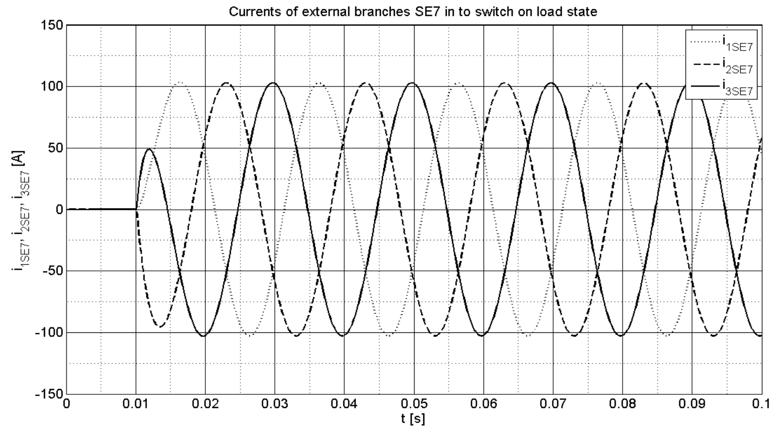

Fig. 14. Waveforms of phase currents SE7 element during to switch on load (Matlab simulation)

Figure 15 shows simulation results in Matlab for one phase transition short circuit.

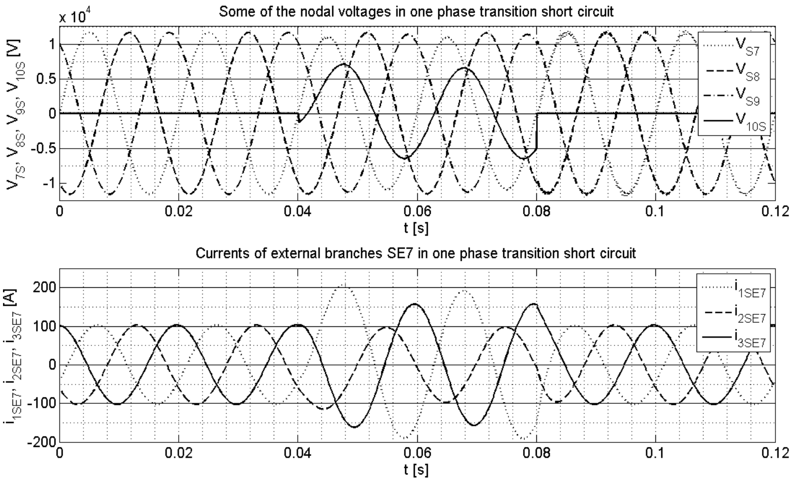

Fig. 15. Waveforms of some nodal voltages and currents of external branches SE7 in one phase transition short circuit (Matlab simulation)

The last analyzed issue of simulation in Matlab was the case of multiple phase transition short circuit. The results of this simulation was shown on Figure 16.

Also in the case of transient analysis can be concluded that digital simulator developed an exemplary electric circuit is working properly.

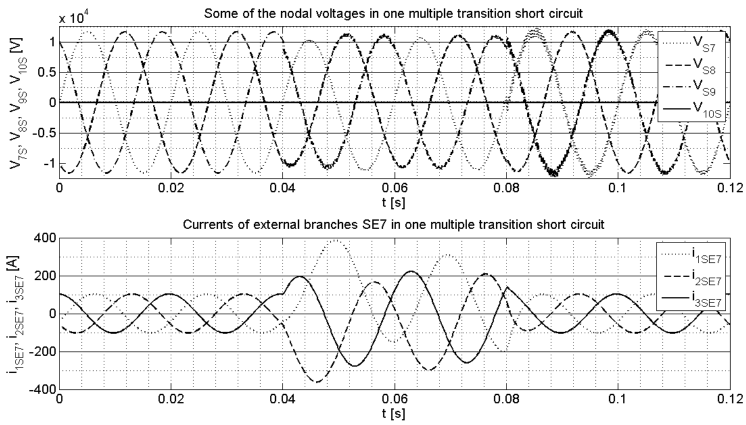

Fig. 16. Waveforms of some nodal voltages and currents of external branches SE7 in multiple phase transition short circuit (Matlab simulation)

7. Conclusions

The article presents the results of a simulation of operating states of an electric circuit based on a multi-core signal processor TMS320C6678. Due to the real time simulation, the created simulator can cooperate with real devices such as regulators. This type of operation is confirmed by the given waveforms from oscilloscope. The possibility of a simulation of a circuit in steady state as well as transient state was shown. It is important for the analysis of electric circuits because registering transient states in real circuit is difficult.

In author's opinion, simulation results created by Matlab are coincidental enough with the results received from simulator based on a signal processor. Moreover, maximal errors estimated for steady states and transient states (Fig. 6, 7, and 8) allow, in the author's opinion, to constitute satisfactory adequacy of the presented model.

This paper demonstrates the possibility of decreasing the calculation time with the use of Gauss-Seidel iteration method for solving linear equation (7). It allowed to decrease the calculation time in reference to the LU factorization method up to 17% (Table. 6.3). It is also important that there is no significant increase of the error calculation in the case of the iterative method (Fig. 6, 7 and 8). It was also shown that the use of double precision calculation can significantly reduce the calculation error (Fig. 6, 7 and 8), without significant increase of the error calculation (Tab. 6.3).

Presented results encourage the author to carry out further research, especially in the field of parallel computing. Another interesting aspect mentioned in the article, is the use of faster convergent iterative methods for solving system of linear equations (7). It could allow to receive bigger benefits from using the iterative method.

Reference

[1] Cieslik S., Obwodowe modele układów elektrycznych w cyfrowych symulatorach pracujących w czasie rzeczywistym, Wydawnictwo Politechniki Poznańskiej, 2013.
[2] Cieslik S., GPU Implementation of the Electric Power System Model for Real-Time Simulation of Electromagnetic Transients, Proc. of the 2-nd International Conference on Computer Science and Electronics Engineering, Atlantis Press, Paris, France, 2013, pp. 1114-1118.
[3] Fajfer M.: Symulacja stanów pracy układu elektrycznego z wykorzystaniem symulatora opartego na procesorze sygnałowym, Poznan University of Technology Academic Journal, 2014, nr 80, str. 35-46.
[4] Fajfer M.: Koncepcja cyfrowego symulatora układów elektrycznych pracującego w czasie rzeczywistym opartego na procesorach sygnałowych, Rynek Energii, 2014, Nr 5, str. 41-49.
[5] Glossary of Software Engineering Terminology, IEEE/ANSI Standard 729, 1983.
[6] Standard Computer Dictionary, IEEE Std 610, 1990.
[7] SPRUH58 - TMDSEVM6678L EVM Technical Reference Manual Version 2.0, Revised March 2012.
[8] SPRS691D - TMS320C6678 Multicore Fixed and Floating-Point Digital Signal Processor, April 2013.
[9] SPRUGP2A - KeyStone Architecture Serial Peripheral Interface (SPI) User Guide, March 2012.
[10] SBAS467A – Octal, 16-Bit, Low-Power, High-Voltage Output, Serial Input DIGITAL-TO-ANALOG CONVERTER, May 2009 – Revised December 2009.
[11] SBAS404B - 16-, 14-, 12-Bit, Six-Channel, Simultaneous Sampling ANALOG-TO-DIGITAL CONVERTERS, October 2006–revised January 2012.
[12] SLLS868O – ISO7240CF, ISO7240C, ISO7240M, ISO7241C, ISO7241M, ISO7242C, ISO7242M High speed quad digital isolators, September 2007 – Revised November 2012.
[13] Kincaid David, Cheney Ward, Analiza numeryczna w przekładzie i pod redakcją Stefana Paszkowskiego, Wydawnictwa Naukowo-Techniczne, Warszawa 2002.