Model predictive control of multilevel cascaded converter with boosting capability – experimental results

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Abstract. The main goal of this paper is to present a five-level converter with the feature of output voltage boosting capability. Thanks to its modular construction and single DC source usage, 5LCHB converter becomes an important alternative for two-level converters operating with DC-DC converters that use bulky inductors. Furthermore, model predictive control (MPC) method is presented, which allows for boosting output voltage of presented converter while providing three-phase load current control and flying capacitor voltage stabilization. The last section describes a 5kVA laboratory model of five-level hybrid converter interfacing RL load and shows experimental results confirming theoretical analysis derived in previous sections.

Key words: cascaded H-bridge (CHB), model predictive control (MPC), multilevel converters.

1. Introduction

Multilevel converters, by overcoming classical topologies limitations and presenting considerable advantages to typical two-level converters, have gained a lot of interest in academic and industrial world in recent years. This paper is a continuation of the simulation study published in [1]. Many papers with new multilevel topologies and their control have been presented. There are also industrial applications like electric drives ACS2000 by ABB [2] and ALSPA VDM6000 by ALSTOM [3], static synchronous compensators PCS 6000 STATCOM by ABB [2], TMEiC solar inverters SOLAR WARE 630 [4] and Eaton 93PM UPS [5].

Multilevel converters are well suited for medium-voltage and high power application because of connecting switching devices in series and using several lower voltage DC levels to synthesize a staircase output voltage waveform.

Such converter design gives advantages such as:
– lower output voltage distortion (lower),
– lower switching losses,
– lower $\frac{dV}{dt}$ in output voltage,
– reduced switching frequency for a given current distortion,
– reduced input filter size for the grid connected applications.

Three main topologies within multilevel converter family are [6, 7]:
– diode clamped converter (NPC),
– flying capacitor (FC),
– cascaded H-bridge converter (CHB).

Recently, a new family called modular multilevel converters (MMC) gained popularity thanks to its attractive features in high power applications [8–10].

By applying modifications to classic multilevel converter topologies, another branch called hybrid converters was created.

Hybrid converters integrate more than one converter topology into one. Each new topology has its own advantages and drawbacks and suits a certain application.

The following examples of hybrid converter topologies can be listed out:
– 5L-HNPC – cascaded connection of 3L-NPC converter [11],
– ANCP-5L – 3L-NPC converter connected with 3L-FC converter [12],
– 3L-NPC connected with H-bridge [13],
– 5L-MLC^2 – [14]

This paper presents an investigation of a novel hybrid converter topology – five-level cascaded H-bridge converter (5LCHB) with only one DC source and model predictive controller (MPC). According to [1, 15] this converter brings the following features:
– generation of boosted output voltage,
– good quality of output waveform with low THD,
– fast response to reference current change.

Utilization of the model predictive controller (MPC) for 5LCHB converter was tested in [1, 15]. The advantages of MPC control can be summed up as follows:
– simple solution for multilevel converter compared to other control strategies,
– elimination of PWM modulator,
– simple implementation of capacitor voltage balancing.

Among the disadvantages of the MPC control we may list:
– requirement of fast processor for on-line optimization,
– the knowledge of the load parameters.

Previous publication concerning 5LCHB converter with MPC control used only simulation model [1, 15–17]. This work examines 5 kVA laboratory model of 5LCHB with the MPC control.

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2. 5LCHB converter model

The 5LCHB converter topology is shown in Fig. 1. The proposed converter uses a standard three-leg two-level converter and a H-bridge in series with each converter leg. Each H-bridge uses a capacitor as a DC power source.
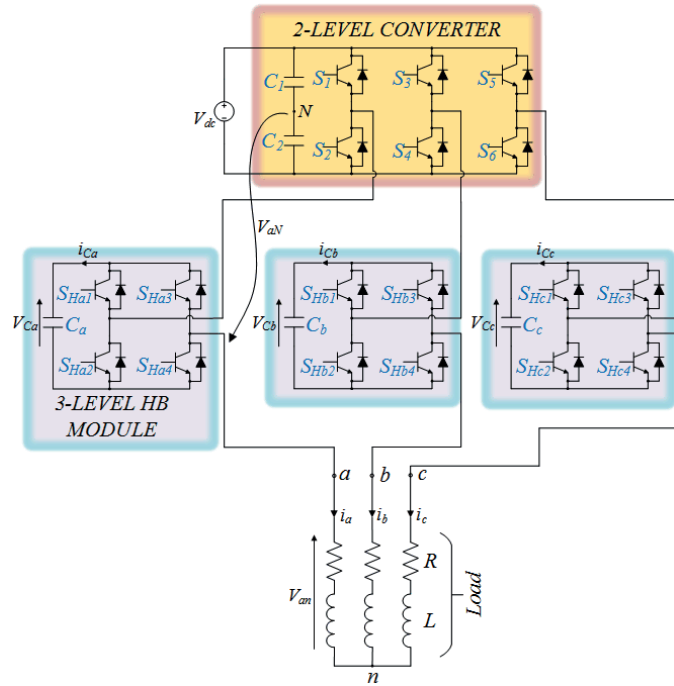

Fig. 1. Topology of five-level cascaded H-bridge converter (5LCHB)

If capacitors voltage V_{Ca}, V_{Cb}, V_{Cc} are kept by controller at voltage level $\frac{V_{DC}}{2}$ then converter generates five-level output waveform with voltage: $+V_{DC}$, $+\frac{V_{DC}}{2}$, 0, $-\frac{V_{DC}}{2}$, $-V_{DC}$ per phase when referenced to point N.

The switching pattern with the correspondent output voltage level for single phase a is given in Table 1.

Table 1
Switching pattern and corresponding output voltage level

S_1	S_2	S_{Ha1}	S_{Ha2}	S_{Ha3}	S_{Ha4}	Output voltage S_{aN}
1	0	0	1	1	0	$+V_{DC}$
1	0	1	0	1	0	$+V_{DC}/2$
1	0	0	1	0	1	
1	0	1	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	1	0	$-V_{DC}/2$
0	1	0	1	0	1	
0	1	1	0	0	1	$-V_{DC}$

3. Mathematical model

The load current dynamics for RL load can be described as follows:

$$V_{xN} = Ri_x + L\frac{di_x}{dt} + V_{nN} \tag{1}$$

$$V_{xN} = S_x V_{DC} \tag{2}$$

where $x = \{a, b, c\}$.

Voltage level indexes S_a, S_b, S_c, and individual level numbers k_a, k_b, k_c for phases a, b, c are defined in Tables 2–4.

Table 2
Converter output voltage level with corresponding voltage level index S_a and individual level number k_a

V_{aN}	S_a	k_a	Switches					
			S_1	S_2	S_{Ha1}	S_{Ha2}	S_{Ha3}	S_{Ha4}
$+V_{DC}$	1	7	1	0	0	1	1	0
$+V_{DC}/2$	0.5	6	1	0	1	0	1	0
$+V_{DC}/2$	0.5	5	1	0	0	1	0	1
0	0	4	1	0	1	0	0	1
0	0	3	0	1	0	1	1	0
$-V_{DC}/2$	−0.5	2	0	1	1	0	1	0
$-V_{DC}/2$	−0.5	1	0	1	0	1	0	1
$-V_{DC}$	−1	0	0	1	1	0	0	1

Table 3
Converter output voltage level with corresponding voltage level index S_b and individual level number k_b

V_{bN}	S_b	k_b	Switches					
			S_3	S_4	S_{Hb1}	S_{Hb2}	S_{Hb3}	S_{Hb4}
$+V_{DC}$	1	7	1	0	0	1	1	0
$+V_{DC}/2$	0.5	6	1	0	1	0	1	0
$+V_{DC}/2$	0.5	5	1	0	0	1	0	1
0	0	4	1	0	1	0	0	1
0	0	3	0	1	0	1	1	0
$-V_{DC}/2$	−0.5	2	0	1	1	0	1	0
$-V_{DC}/2$	−0.5	1	0	1	0	1	0	1
$-V_{DC}$	−1	0	0	1	1	0	0	1

Table 4
Converter output voltage level with corresponding voltage level index S_c and individual level number k_c

V_{cN}	S_c	k_c	Switches					
			S_5	S_6	S_{Hc1}	S_{Hc2}	S_{Hc3}	S_{Hc4}
$+V_{DC}$	1	7	1	0	0	1	1	0
$+V_{DC}/2$	0.5	6	1	0	1	0	1	0
$+V_{DC}/2$	0.5	5	1	0	0	1	0	1
0	0	4	1	0	1	0	0	1
0	0	3	0	1	0	1	1	0
$-V_{DC}/2$	−0.5	2	0	1	1	0	1	0
$-V_{DC}/2$	−0.5	1	0	1	0	1	0	1
$-V_{DC}$	−1	0	0	1	1	0	0	1

Capacitor currents can be defined as:

$$i_{cx} = H_x i_x \qquad (3)$$

where H_x can be defined as follows:

$$H_x = \begin{cases} 1 & for\ k_x = 0\ or\ 4 \\ 0 & for\ k_x = 1\ or\ 2\ or\ 5\ or\ 6 \\ -1 & for\ k_x = 3\ or\ 7 \end{cases} \qquad (4)$$

with $x = \{a, b, c\}$.

There are $8^3 = 512$ valid switching states. This rises a crucial problem for practical implementation of predictive controller. In order to choose the optimal state, all combinations need to be evaluated in the cost function. In this case, the execution time will exceed the sampling period, which typically reaches values of 10–200 μs. Therefore, in this work phase voltage is taken as control input. Thus there is $5^3 = 125$ different space voltage vectors. This is still a large number of mathematical operations that need to be performed within one sampling period. In order to reduce number of mathematical operations, further simplification of the mathematical model was performed. In this work it is assumed that common voltage v_{nN} is small and can be neglected in equation (1), then each phase can be considered separately and there are $3 \times 5 = 15$ voltage levels that need to be taken into account. The correctness of this assumption will be validated in experimental setup.

4. Predictive current control

Model predictive control (MPC) has appeared as a promising alternative to classical control algorithms with pulse width modulation (PWM) for power converters control [18, 19].

Predictive control can be divided into: deadbeat control, hysteresis based, trajectory based, model predictive control (MPC) [19]. Deadbeat control chooses optimal actuation that makes error equal to zero in the next sampling instant. Hysteresis based strategy is to keep the controlled variable within a boundaries of a hysteresis area. Trajectory based controller forces the variable to follow a predefined trajectory. This work utilizes finite-control-set model predictive current control (FCS-MPC). This strategy uses a discrete model of a converter and load to predict the behavior of the system for each possible voltage level generated by the converter for the predefined prediction horizon. The voltage level that minimizes a cost function is selected and applied during a whole sampling interval [20]. The application discussed in this paper have a horizon length of 1.

The current of a sample $k + 1$ for the model of the RL load from Fig. 1 with a sample time T_s can be expressed as [21]:

$$i_x^p(k+1) = \left(1 - \frac{RT_s}{L}\right)i_x(k) + \frac{T_s}{L}v_{xN}(k) \qquad (5)$$

Predicted capacitor voltage can be expressed as:

$$v_{Cx}^p(k+1) = v_{Cx}(k) + \frac{1}{C_x}i_{cx}(k)T_s \qquad (6)$$

where $x = \{a, b, c\}$.

To determine which output voltage level is an optimal one, the cost function needs to be evaluated. The proposed cost function g is a sum of squared current and capacitors voltage errors:

$$g = \frac{1}{I_N}\left(i_{xref} - i_x^p\right)^2 + \frac{\lambda}{V_{Cref}}\left(V_{Cref} - V_{Cx}^p\right)^2 \qquad (7)$$

where: I_N – nominal current, i_{xref} – reference current, i_x^p – the predicted current from (11), V_{Cref} – reference voltage of capacitor, V_{Cx}^p – predicted voltage of capacitors, $x = \{a, b, c\}$, λ – weighting factor that determines relation between terms dedicated to current tracking and capacitors voltage balancing. The squared error formula used in (7) gives better reference tracking than the use of absolute error [22].

The evaluation of the cost function is made for all 5 possible output voltage levels per phase. The voltage level that leads to a minimum cost is selected to control the system. Capacitors voltage errors in a cost function provide capacitor voltage regulation. The whole algorithm of MPC is illustrated in Fig. 2.
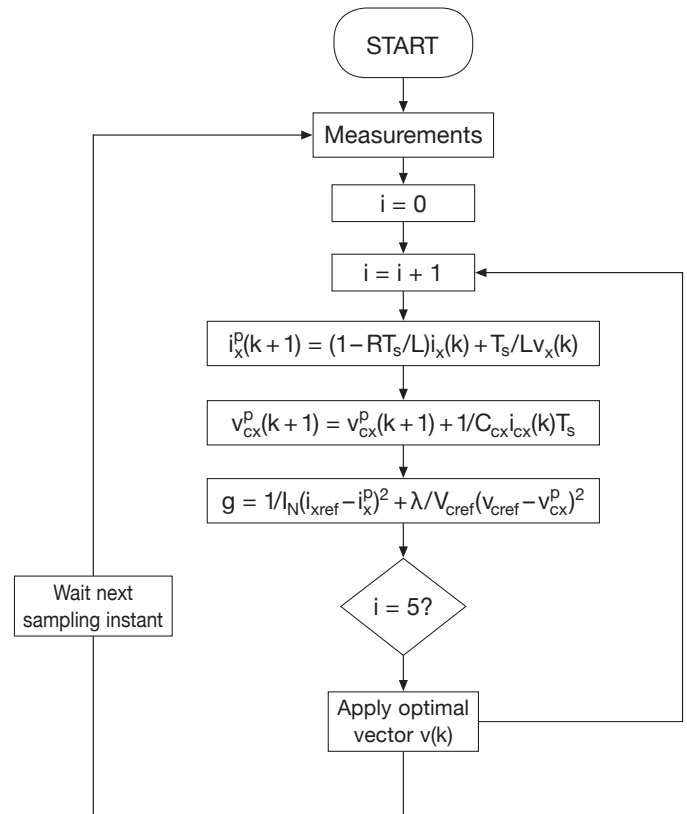

Fig. 2. MPC control algorithm

5. Experimental prototype

The 5 kVA laboratory model was developed to present converter operation in the system analyzed in previous sections. The three phase two-level converter is supplied by fixed voltage source V_{DC} split by two capacitors giving reference point N. Three-level H-bridges are connected in series to each of three-leg two-

level converter. DC side of the H-bridge modules is powered by electrolytic capacitors. The 5LCHB inverter is connected to symmetric load consisting of variable resistor and inductance that allowed to test converters features at different load displacement angles φ.

Figure 3 shows schematic of experimental setup of three-phase five-level cascaded H-bridge converter (5LCHB) powering RL load.
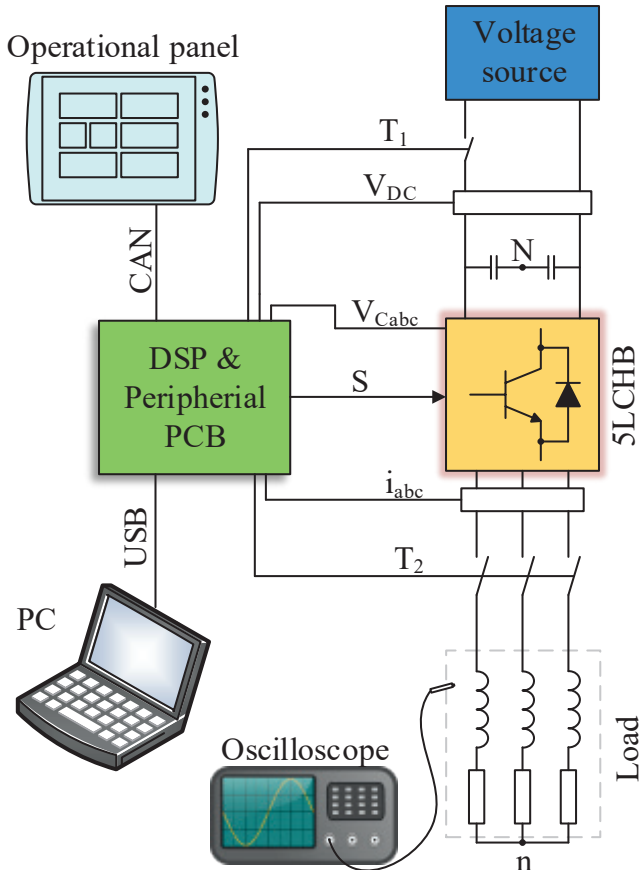

Fig. 5. View of the laboratory setup

The MPC algorithm with necessary calculations and controls have been implemented in Texas Instruments controlCARD with TMS320F28377D dual-core digital signal processor connected to peripheral board (Fig. 4).

The sampling frequency is set to 10 kHz for correct inverter operation. To maintain load current regulation and capacitor voltage balance, LEM LA-55p transducers and AMC1100 isolation amplifiers are used.

Eaton's operational panel with touch screen used to interface with operator is responsible for entire system control and ensures preview of main signals and setting reference values for control algorithm. It is connected with DSP via CAN bus.

6. Experimental results

6.1. Basic characteristics. An experimental test of the 5LCHB converter with model predictive controller for RL type of load was carried out. System parameters are shown in Table 5.

Fig. 3. Laboratory model schematic of 5LCHB converter with RL load
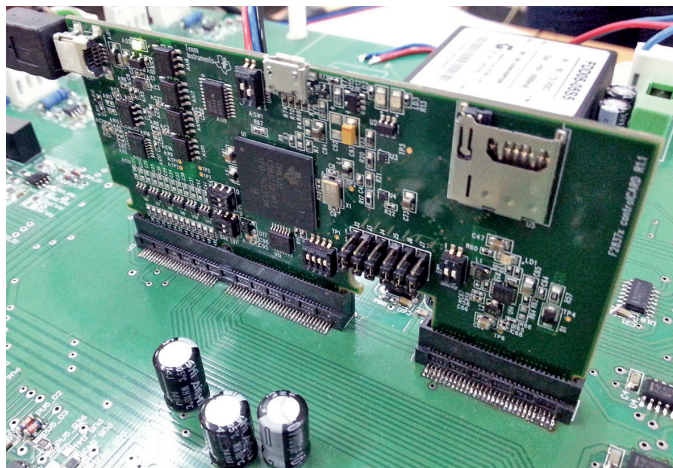
Fig. 4. Texas Instruments ControlCARD TMDSDOCK28377D

Table 5
System parameters

System parameters	Value	Description
V_{DC}	100 V	DC power supply voltage
V_{Cref}	50 V	Capacitors reference voltage
C	6800 µF	Capacitance of capacitors C_a, C_b, C_c
R	Depend on a phase displacement angle φ	Load resistance
L		Load inductance
T_s	100 µs	Sampling period
f	50 Hz	Reference current frequency

For measurements the Yokogawa WT1806 Precision Power Analyzer and Tektronix TPS2014 oscilloscope were used.

The modulation index definition used for the experiment is written as:

$$m = \frac{V_1}{V_{DC}/2} \tag{8}$$

where V_1 is the fundamental harmonic of the output phase voltage. Phase voltages, phase currents, capacitor voltages and currents for different modulation indexes and different phase displacement angles are depicted in Figs. 6–19.

The maximum modulation index for the tested converter for different phase displacement angles and corresponding

a) Results for phase displacement angle $\varphi = 58°$
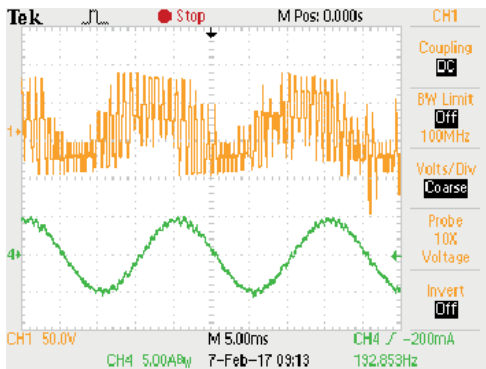
Fig. 6. Phase voltage V_{an} (top), phase current i_a (bottom) for $R = 2.9\ \Omega$, $L = 14.9\ mH$, $m = 0.5$, $\varphi = 58°$
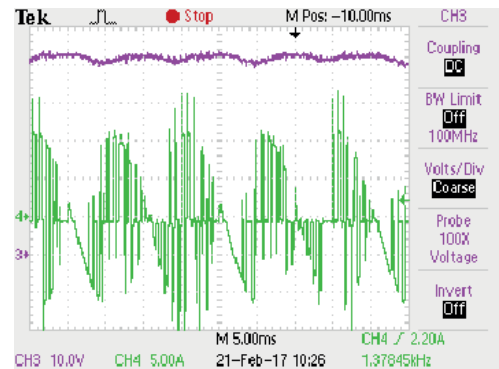
Fig. 9. Voltage (top) and current (bottom) of capacitor C_a for $R = 2.9\ \Omega$, $L = 14.9\ mH$, $m = 1.2$, $\varphi = 58°$
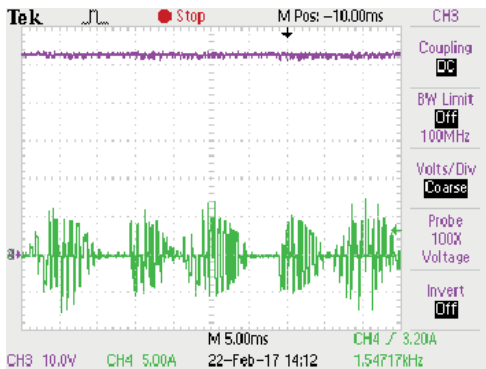
Fig. 7. Voltage (top) and current (bottom) of capacitor C_a for $R = 2.9\ \Omega$, $L = 14.9\ mH$, $m = 0.5$, $\varphi = 58°$
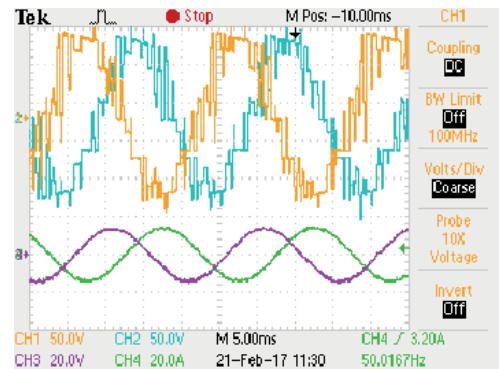
Fig. 10. Phase voltages V_{an}, V_{bn} (top), phase current i_a, i_b (bottom) $R = 2.9\ \Omega$, $L = 14.9\ mH$, $m = 1.55$, $\varphi = 58°$
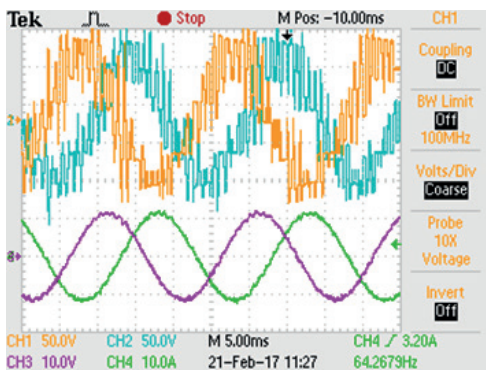
Fig. 8. Phase voltages V_{an}, V_{bn} (top), phase current i_a, i_b (bottom) for $R = 2.9\ \Omega$, $L = 14.9\ mH$, $m = 1.2$, $\varphi = 58°$
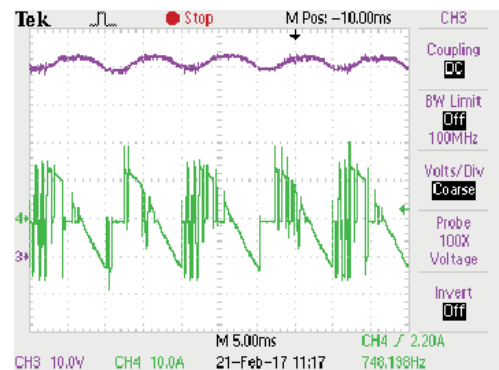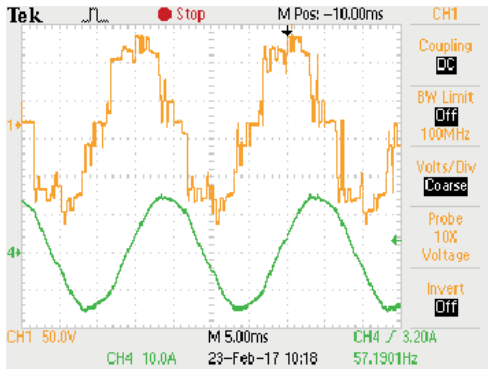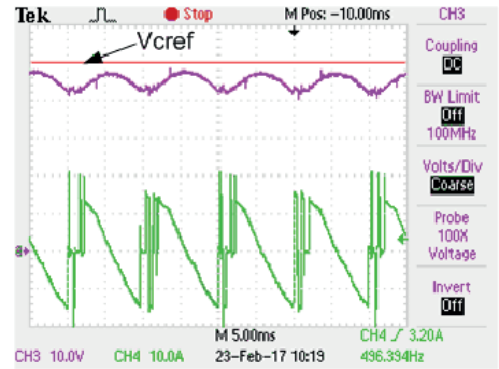

Fig. 11. Voltage (top) and current (bottom) of capacitor C_a for $R = 2.9\ \Omega$, $L = 14.9\ mH$, $m = 1.55$, $\varphi = 58°$

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Fig. 12. Phase voltage V_{an} (top), phase current i_a (bottom)
for $R = 2.9\ \Omega$, $L = 14.9\ mH$, $m = 1.8$, $\varphi = 58°$

Fig. 13. Voltage (top) and current (bottom) of capacitor C_a
for $R = 2.9\ \Omega$, $L = 14.9\ mH$, $m = 1.8$, $\varphi = 58°$
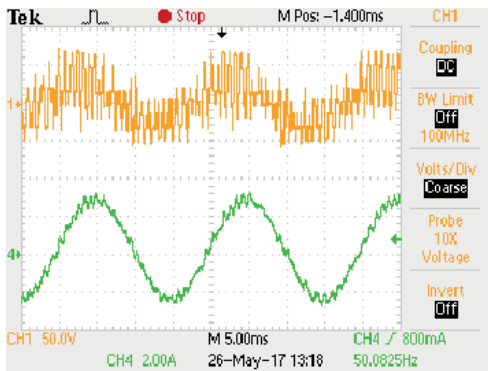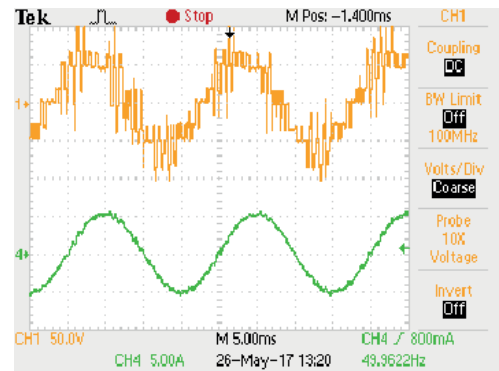
b) Results for phase displacement angle $\varphi = 28°$

Fig. 14. Phase voltage V_{an} (top), phase current i_a (bottom)
for $R = 8.7\ \Omega$, $L = 14.9\ mH$, $m = 0.5$, $\varphi = 28°$

Fig. 15. Phase voltage V_{an} (top), phase current i_a (bottom)
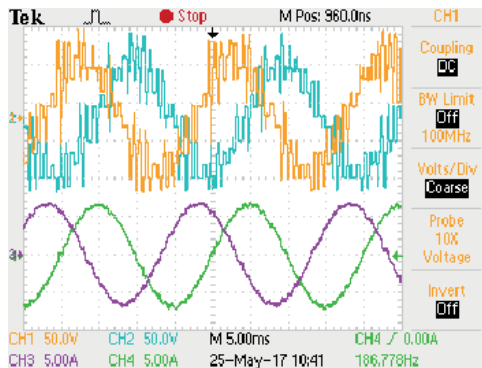for $R = 8.7\ \Omega$, $L = 14.9\ mH$, $m = 1$, $\varphi = 28°$

Fig. 16. Phase voltages V_{an}, V_{bn} (top), phase current i_a, i_b
(bottom) for $R = 8.7\ \Omega$, $L = 14.9\ mH$, $m = 1.3$, $\varphi = 28°$
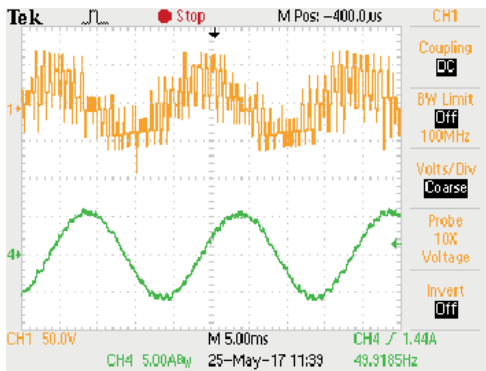
c) Results for phase displacement angle $\varphi = 76°$

Fig. 17. Phase voltage V_{an} (top), phase current i_a (bottom)
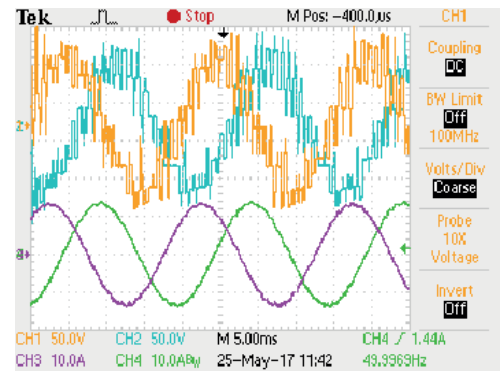for $R = 1.16\ \Omega$, $L = 14.9\ mH$, $m = 0.5$, $\varphi = 76°$

Fig. 18. Phase voltages V_{an}, V_{bn} (top), phase current i_a, i_b (bottom)
for $R = 1.16\ \Omega$, $L = 14.9\ mH$, $m = 1.2$, $\varphi = 76°$
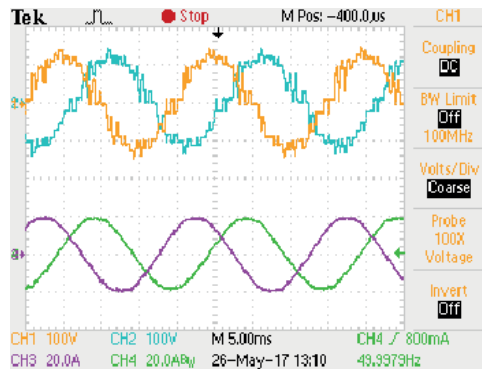

Fig. 19. Phase voltages V_{an}, V_{bn} (top), phase current i_a, i_b (bottom)
for $R = 1.16\ \Omega$, $L = 14.9\ mH$, $m = 1.8$, $\varphi = 76°$
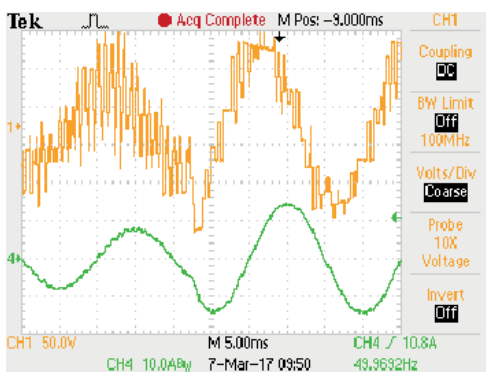
d) Dynamic behavior for $\varphi = 58°$

Fig. 20. Voltage (top), current i_a (bottom) for current reference
step which corresponds to modulation index from $m = 0.8$
to $m = 1.55$ for $R = 2.9\ \Omega$, $L = 14.9\ mH$, $m = 0.5$, $\varphi = 58°$
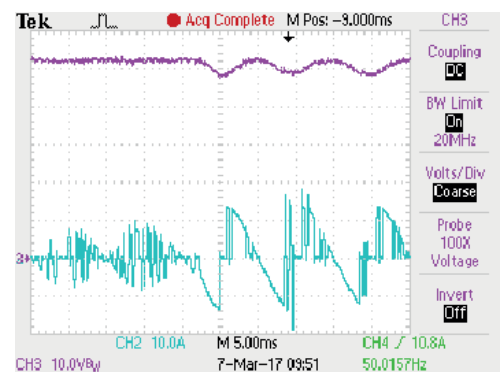

Fig. 21. Voltage (top) and current (bottom) of capacitor C_a
for current reference step which corresponds to modulation index
from $m = 0.8$ to $m = 1.55$ for $R = 2.9\ \Omega$, $L = 14.9\ mH$, $\varphi = 58°$

boosting ratio is shown in Table 6. Boosting ratio is defined as follows:

$$boosting\ ratio = \frac{I_{max\_5l}}{I_{max\_2l}} \tag{9}$$

where: I_{max_5l} – maximum current for a given load for 5LCHB converter, I_{max_2l} – maximum current for a given load for classical two-level converter.

Table 6

Maximum modulation index m	Boosting ratio	Phase displacement angle φ
1.3	1.13	28°
1.55	1.34	58°
1.8	1.56	76°

Maximum current for the 5LCHB converter is presented in Table 7.

Table 7

Maximum current for classical 3-phase two-level converter	Maximum current for 5LCHB converter	Phase displacement angle φ
5.83 A	6.57 A	28°
10.48 A	14 A	58°
11.97 A	18.66 A	76°

When modulation index exceeds the maximum from Table 6 converter goes beyond the linear region of operation. With the increasing of modulation index, capacitors voltage ripples also increases (Table 8). It is caused by the rise of the capacitor current. When modulation index is too high, phase current becomes distorted (Fig. 12) and the controller loses its capability to balance capacitor's voltage, which drops below the reference level (Fig. 13). In order to test the dynamic behavior of the system, the phase current step was performed (Fig. 20 and Fig. 21). It can be noticed that during the new reference current step the selected optimal voltage vector is kept as long as the load current achieves the reference value. Capacitors voltage ripple increases after current change but remains stable. That confirms an effective operation of capacitors voltage balancing.

Table 8
Capacitor voltage ripple

Capacitor voltage ripple [V]	Modulation Index m
2.1	0.8
3	1
4	1.2
5.12	1.5
6.12	1.8

Figures 6–15 confirm proper current control and capacitors voltage balancing capability by the model predictive controller
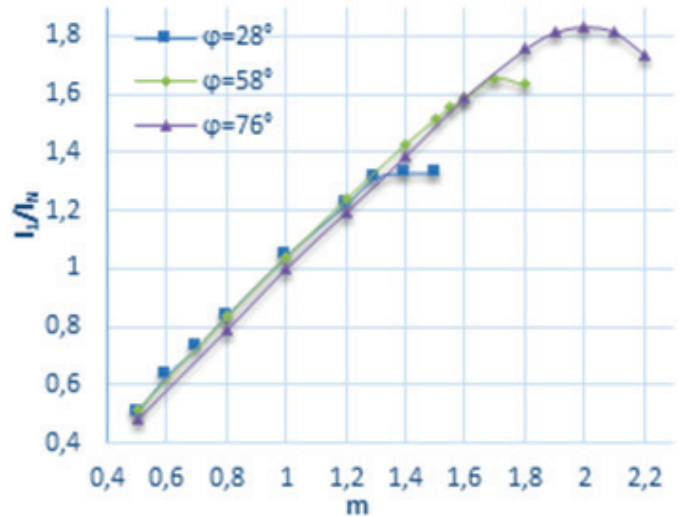
Fig. 22. Control characteristic of 5LCHB converter for different phase displacement angles φ

when common mode voltage is excluded from (1). Measuring fundamental harmonic mode of phase current for different modulation index, the control characteristic was designated (Fig. 22). Current I_N is the maximum phase current available in linear region of operation of the two-level converter with PWM for the given RL load.

The bigger the phase displacement angle φ is, the greater the linear part of control characteristic. That confirms theoretical considerations presented in [1].

6.2. Influence of weighting factor selection. The influence of weighting factor λ on control characteristic for angle $\varphi = 58°$ was measured and depicted in Fig. 23.
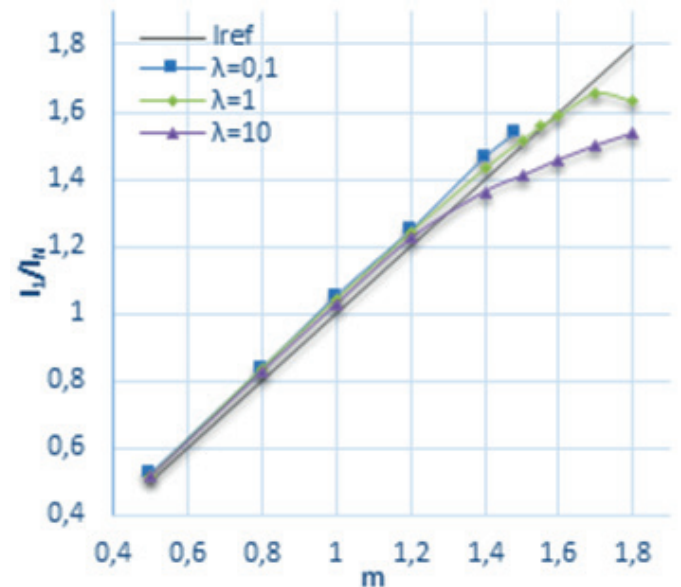
Fig. 23. Control characteristic of 5LCHB converter for different weighting factor values λ for $R = 2.9\ \Omega$, $L = 14.9\ mH$, $\varphi = 58°$

Current I_{ref} depics the ideal characteristic. The control characteristic for $\lambda = 0.1$ loses ability to balance capacitors voltage for modulation index higher than $m = 1.4$. It can be noticed that in the linear region there is a steady state error between the ideal characteristic of I_{ref} and the measured characteristics. It is caused by the lack of an integration action in predictive controller.

The quality of output waveforms was measured using THD_u, THD_i and mean absolute tracking error, which is defined as the mean value the absolute differences between the reference current and measured load current, within a given time interval of l samples:

$$e_i = \frac{1}{l} \sum_{k=0}^{l} |iref(k) - i(k)| \qquad (10)$$

Figure 24 shows the current error e_i versus modulation index for different weighting factor λ.
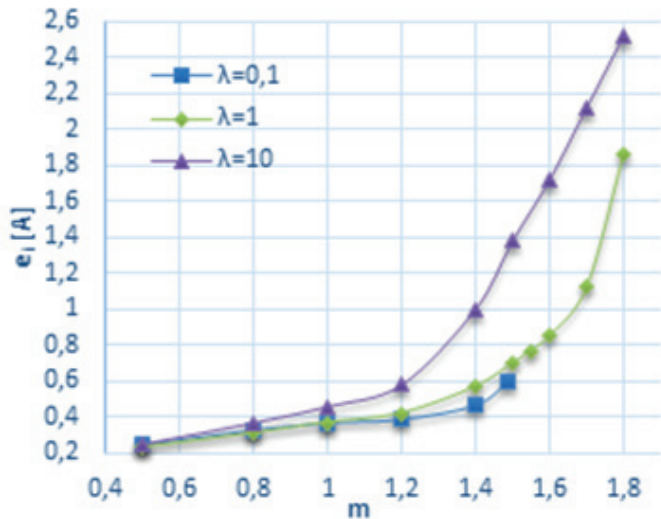

Fig. 24. Mean value of tracking error for $\lambda = 0.1$, $\lambda = 1$ and $\lambda = 10$ and $R = 2.9\ \Omega$, $L = 14.9\ mH$, $\varphi = 58°$

It can be seen that the smallest error in a wide range of modulation index changes is for $\lambda = 0.1$. When parameter λ is small, the capacitor voltage error has small impact on a cost function value and better current tracking is achieved. The drawback of low value of λ is lower maximum available modulation index. When the value of λ is high, the modulation index range is wide at the expense of higher current error e_i.

Figure 25 and Fig. 26 show a THD_u and THD_i versus modulation index m. The THD_u diagram can be divided into three regions. First region corresponds to the linear part of control characteristic from Fig. 23. For low modulation index, THD_u is high, because output voltage is not constructed with all possible voltage levels. When modulation index increases, additional levels are added to the waveform and the output voltage be-

comes a sinusoidal shape, so THD_u is getting lower. The second region corresponds to the nonlinear part of control characteristic. In this part capacitors voltage error greatly increases and capacitor voltage balancing is performed at the expense of current quality. That causes a sudden rise of THD_u. In the third region, output phase voltage saturates and the level flattens. The THD_u diagram for $\lambda = 0.1$ is located completely in region I. For modulation index m greater than $m = 1.48$ system loses ability to balance capacitors voltage.
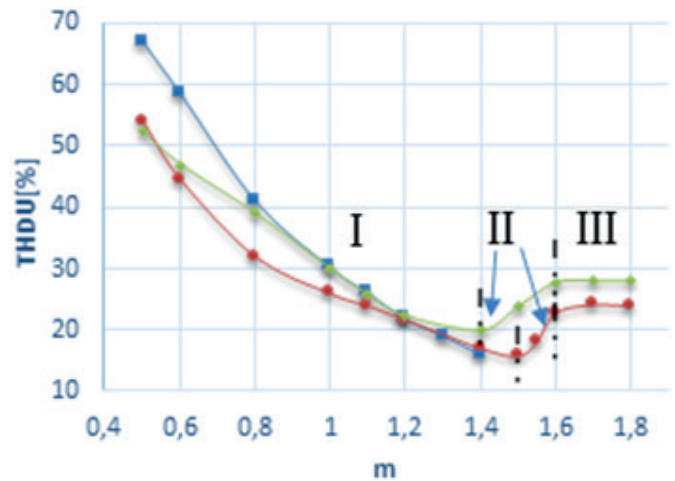

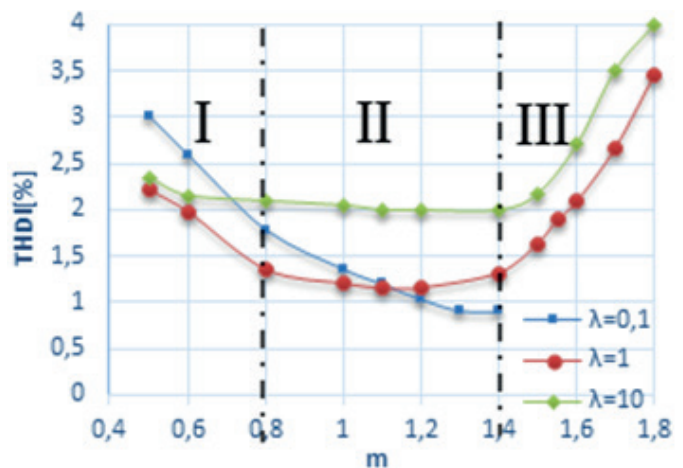Fig. 25. THD_u of phase voltage for $\lambda = 1$ and $R = 2.9\ \Omega$, $L = 14.9\ mH$, $\varphi = 58°$

Fig. 26. THD_i of phase current for $\lambda = 1$ for $R = 2.9\ \Omega$, $L = 14.9\ mH$, $\varphi = 58°$

The THD_i diagram can be divided into three regions as well. An example division was made for $\lambda = 1$. It can be seen that in the first region the THD_i gets lower with the modulation index increase. It is caused by the increase in number of levels in phase voltage. In the second region the THD_i reaches plateau. In the third region, due to voltage balancing, the phase voltage gets distorted, causing THD_i to increase.

6.3. Influence of model parameter errors. The impact of mathematical model parameters error was also examined. Applying different value of resistance than the actual value of the load resistance, the error e_i was measured. Figure 27 and Fig. 28 presents error e_i for different values of resistance R applied to load model (5).
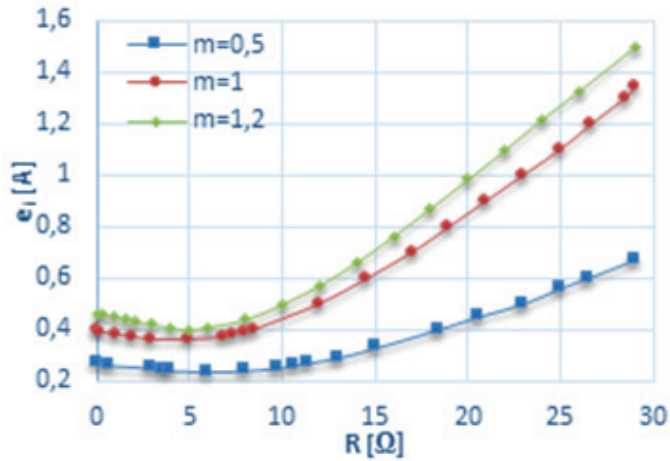

Fig. 27. Mean value of tracking error versus R for load resistance 5 Ω and inductance 14.9 *mH* and $\lambda = 1$
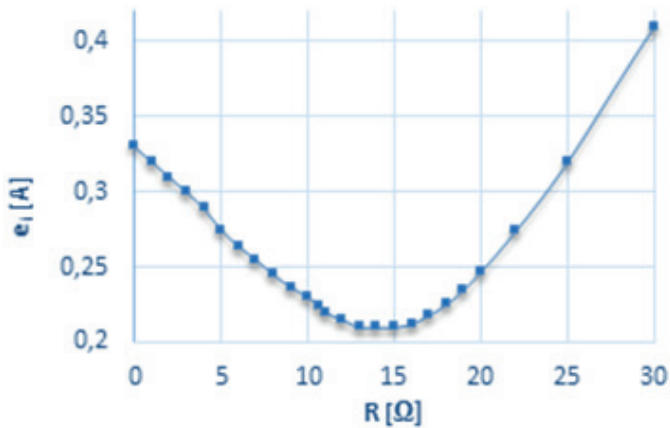

Fig. 28. Mean value of tracking error versus R change for load resistance 14 Ω and inductance 14.9 *mH* and $\lambda = 1$

The error e_i reaches minimum around the actual value of the load $R = 5$ Ω. The function of e_i versus load resistance R is symmetrical to the point of actual resistance. It can be seen that this function flattens around its minimum. That means that small error of load model resistance has small impact on the performance of the system.

Applying different value of inductance to the load model error e_i was measured and depicted in Fig. 29. It can be noticed that the function reaches its minimum around the point of the actual value of inductance. For smaller inductance than the actual one, the error e_i drastically rises. When bigger value
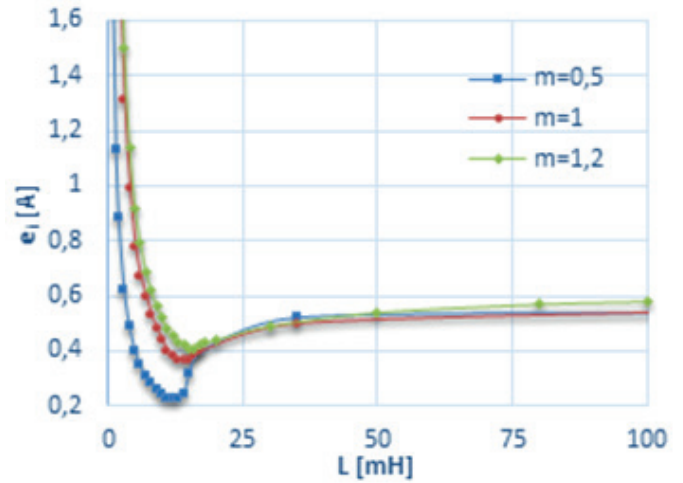

Fig. 29. Mean value of tracking error versus model L change for load resistance 14 Ω and inductance 14.9 *mH* and $\lambda = 1$

of inductance is applied, the error slightly increases but then function flattens. That means it is safer to apply bigger value of inductance when parameters of the load are not precisely known.

7. Conclusions

The paper analyzes cascaded H-bridge five-level converter with model predictive control (MPC). The proposed predictive algorithm performs output current control and capacitor voltage balancing. A simplification of mathematical model of the load with omitting the common-mode voltage V_{nN} made it possible to implement proposed MPC algorithm in Texas Instruments controlCARD with TMS320F28377D processor. The algorithm execution time was 16 μs with 100 μs sampling period. Experiments confirm proper current control and capacitors voltage balancing by the system. The examined 5LCHB converter with MPC control can boost output ac voltage with maximum modulation index $m = 1.8$ for phase displacement angle $\varphi = 76°$. The control characteristic of 5LCHB converter for different phase displacement angle φ and weighting parameter λ was presented. The quality of output phase current was measured using THD_u, THD_i and mean absolute tracking error e_i. Utilizing the error e_i (10), the sensitivity to mathematical parameters error was examined.

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