PROBLEMY KOLEJNICTWA
RAILWAY REPORT
Issue 186 (March 2020)
DOI: 10.36137/1867E
ISSN 0552-2145 (print) ISSN 2544-9451 (on-line)

Safety of Single-Channel Railway Traffic Control

Roman PNIEWSKI[1]

Summary
Reversible gates enable the creation of fault tolerant digital devices. The application of these gates allows safe control systems to be realized. At present, control systems based on relays are being replaced by systems based on computer technology. This technology allows the implementation of safe systems. Because this system is composed of many elements, it is very difficult to obtain a high safety level for it. The application of reversible logic in the synthesis of digital systems constitutes an alternative approach. The paper presents reversible gates along with examples of their usage in the synthesis of digital systems. The main advantage of reversible logic is the possibility of synthesis of self testing and fault tolerant circuits. The application of circuits based on reversible logic allows safe control systems to be developed. The paper also presents a proposal for the application of reversible logic in simple control systems.

Keywords: reversible logic, railway traffic control, safety

1. Introduction

In the 1970s, electronic systems were found to be useful for railway traffic control (SRK devices). The electronic systems, in particular digital systems, started supplanting the previously applicable key and relay-based systems. The increase in the integration of integrated circuits allowed SRK devices which fulfilled more and more functions to be built. The emergence of industrial controllers and industrial versions of PCs (along with real-time operating systems) allowed program solutions to be used for the fulfillment of algorithms of SRK devices. In contemporary digital SRK systems, the algorithms for controlling, processing and storing data are performed mainly in a systematic way, usually in micro-processor systems in which fulfillment of a specific algorithm follows a program stored in the memory.

The relay-based SRK systems were designed as safe systems based on the fail-safe rule. It meant that no single fault could lead to the erroneous adjustment of external devices (signaling device, switch). This is because, in the case of relay-based SRK devices, a single fault must force a change of the system status into one defined as safe. With regard to computer devices, redundancy is used. The solutions used in traffic control computer systems usually adopt two computers which fulfill the same control algorithm and which supervise each others' actions [9, 11].

An alternative to computer solutions (which, due to substantial expansion, result in limited reliability) may be a return to equipment solutions (electronic) or equipment-program solutions (System On Chip systems) [5, 8], due to the development of specialized integrated circuit technology. In modern railway automation systems (SRK), specialized digital systems are becoming more and more popular. The primary goal of SRK systems is to provide safety. For this reason, the methods of designing these systems deviate from commonly used digital systems synthesis methods. When designing digital systems, the greatest emphasis is placed on the minimization of logic functions which describe the system. As for SRK systems, the most important aspect is to specify the system operation mode in a determined way, and the designer must anticipate the operation of the system in every possible situation. Regardless of the way control algorithms are fulfilled, modern SRK devices and systems must satisfy relevant safety standards. For new systems, the requirements included in the following norms must be met:

1. PN-EN 50126: Railway applications – Specification of reliability, availability, maintainability and safety;

[1] Ph.D. Eng.,prof. UTH Rad; Kazimierz Pulaski University of Technology and Humanities in Radom, Faculty of Transport, Electrical Engineering and Computer Science; e-mail: e-mail: r.pniewski@uthrad.pl.

2. PN-EN 50128: Railway applications – Communication, signaling and control systems – Programs for railway control and security systems;
3. PN-EN 50129: Railway applications – Communication, signaling and control systems – electronic signaling systems related to safety.

The aforesaid norms define most requirements in relation to equipment solutions, program solutions and equipment-program solutions. The equipment used in SRK devices and systems must satisfy the requirements of the following norms: PN-EN50126 and PN-EN50129, while programs fulfilling control functions must comply with the requirements of the norm: PN-EN50128.

The above-stated norms do not demonstrate requirements concerning the computer-assisted specification process or generation of integrated circuits intended for SRK systems. An alternative to classic digital systems are reversible gates which allow the status of the digital system to be controlled. Thanks to this solution, it is possible to create single-channel safe dependency systems for the railway industry.

2. Reversible gates

Conventional computers adopt two-valued Boolean logic. The functions describing the digital system most frequently use two operators: AND and OR. These two operations have several input bits and one output bit, which leads to the limitation of information at the output. When the system has fewer available statuses, its entropy drops.[12] As the second law of thermodynamics prohibits the reduction of entropy in the closed system, the limitation of entropy in one place must be compensated with the generation of entropy in the other. The generated entropy as a result of deleting the bit of information is as follows:

$$\Delta S = k_b T \cdot \ln 2 .$$

Therefore, the computers which operate on the basis of Boolean algebra always disperse energy not smaller than $k_b T \cdot \ln 2$.

This generation of heat in the course of the computational process is the limitation of the potential PC speed due to the amount of heat generated. Fredkin and Toffoli proved that reversible logic gates can create a basis for a universal computer. Another advantage (aside from lower power dissipation) of reversible gates is the possibility of constructing self-testing systems and fault-tolerant systems out of them.

In the literature, we can find a number of examples of reversible gates-starting from basic ones developed many years ago, and ending up with the latest variants (considering the control of parity of inputs and outputs) [2, 3, 4]. Below, examples of basic reversible gates are presented along with tables of truth and code in VHDL.

The Feynman gate is one of the CNOT gates. The symbol of the gate is illustrated in Fig. 1, while Table 1 shows the gate passage function. Below, there is a description of the gate in the VHDL language.

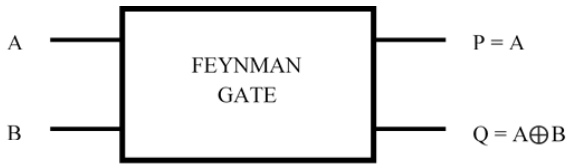

Fig. 1. Feynman Gate; own elaboration on the basis of [3]

Table 1

Feynman gate transition function

A	B	P = A	Q = A⊕B
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

[Own elaboration].

```
Library ieee[2];
Use ieee std_logic.1164..all;
Entity feynmang is
Port(A, B: in std_logic;
P, Q: out std_logic);
end feynmang;
architecture ckt of feynmang is
begin
P<= A;
Q<= A xor B;
End ckt;
```

The Toffoli gate is a CCNOT gate, also referred to as a "controlled-controlled-not" gate. The symbol of the gate is presented in Fig. 2. Table 2 shows the gate transition function.

[2] Standard data type library.

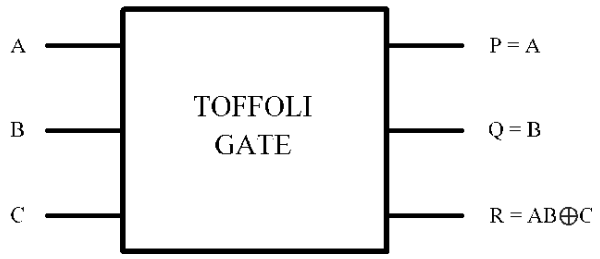

Fig. 2. Toffoli gate; own elaboration on the basis of [3]

Table 2

Toffoli gate transition function

A	B	C	P = A	Q = B	R = AB⊕C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

[Own elaboration].

```
Library ieee;
Use ieee std_logic.1164..all;
Entity toffolig is
Port(A, B, C : in std_logic;
P, Q, R : out std_logic);
end toffolig;
architecture ckt of toffolig is
signal s1 : std_logic;
begin
P<= A;
Q<= B;
S1<=A and B;
R<= S1 xor C;
End ckt;
```

As opposed to the Toffoli gate, which has two check bits and one target bit, the Fredkin gate has one check qbit and two target bits. Target bits swap if the check bit is 1, otherwise they remain unchanged.

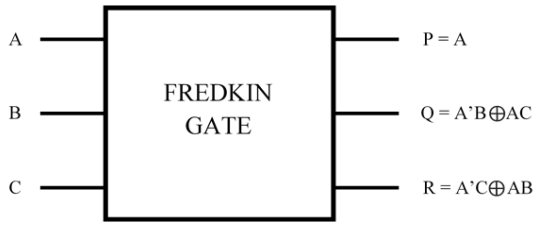

Fig. 3. Fredkin gate; own elaboration on the basis of [3]

Table 3

Fredkin gate transition function

A	B	C	P = A	Q = A⊕B	R = AB⊕C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

[Own elaboration].

```
Library ieee;
Use ieee std_logic.1164..all;
Entity fredking is
Port(A, B, C : in std_logic;
P, Q, R : out std_logic);
end fredking;
architecture ckt of fredking is
signal Abar, S1, S2, S3, S4 : std_logic;
begin
P<= A;
Abar<= not A;
S1<=Abar and B;
S2<= A and C;
Q<= S1 xor S2;
S3<= Abar and C;
S4<= A and B;
R<= S3 xor S4;
End ckt;
```

2.1. Gates which keep parity

There are many examples of reversible gates which keep parity that have been known for ages (such as the double Feynman or Fredkin gates), however, in the last couple of years there have been new ideas (such as fault-tolerant gates or the Islam gate) [1, 6, 7]. Further in the article, in the process of creating a fault-tolerant system, a new fault-tolerant gate is used. Below, there are symbols and tables of truth for the double Feynman gate and NFT.

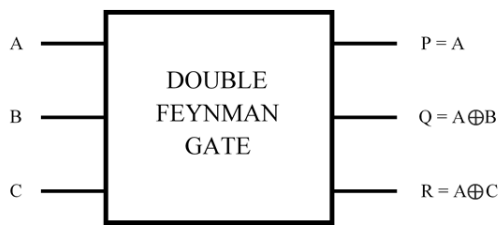

Fig. 4. Double Feynman gate; own elaboration on the basis of [1]

Table 4

Double Feynman gate transition function

A	B	C	P = A	Q = A⊕B	R = A⊕C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

[Own elaboration].

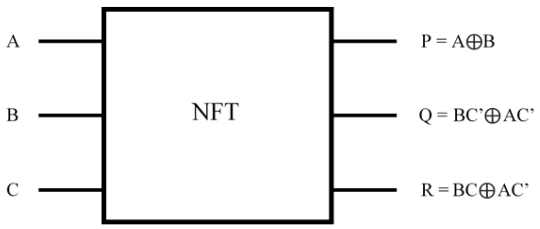

Fig. 5. NFT gate; own elaboration on the basis of [1]

Table 5

NFT gate transition function

A	B	C	P = A⊕B	Q = BC'⊕AC'	R = BC⊕AC'
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	1	0	0	1

[Own elaboration].

Taking into account the table of truth, we can easily notice that the selected gate satisfies the parity criterion. Performing the separate alternative operation for all values at the gate input ($A \oplus B \oplus C$) and comparing it with the same action for outputs ($P \oplus Q \oplus R$), we should always have equality. This dependence will prove to be very useful when specifying the correct operation of particular gates.

3. Simulation of systems with reversible gates

The analysis of SRK system safety requires their operation to be checked in various situations; it is necessary to identify the reaction of the system to errors and disturbances. Not all statuses of the system can be forced in laboratory conditions and therefore, when elaborating the safety proof, computer simulations are used. The Faculty of Transport Control Systems at the UTH developed simulation models of reversible gates for two simulators of digital systems, QUCS and Multisim.

The QUCS (Quite Universal Circuit Simulator) program is a free simulator of electronic, analog and digital systems. The first version of the program was dedicated to Linux systems. Current versions of the program are supported by Linux and Windows operating systems. The software is fully free-of-charge and there are software source codes available, which allows its modification. For the purposes of analog system simulation, the SPICE algorithm was used, while the digital simulation occurs at many stages. Based on the schematic diagram, the program generates a list of connections and saves it in the file netlist.txt. The list is saved in the VHDL language (VHSIC Hardware Description Language). Next, a conversion into C occurs (with the use of the FreHDL environment). To compile the source code, the Mingw compilator is used.

The simulation process in QUCS is "controlled" by the input file: "qucsdigi.bat". Thanks to modification of this file, it is possible to control the simulation freely. In this way, it is feasible to add other "input" programs to the simulator. The program allows files describing modules in the Verilog and VHDL languages to be included into the diagram. The symbol of the file attached is created automatically on the basis of the interface description. Fig. 6 demonstrates the screenshot from designing the model of the reversible gate.

Multisim serves to simulate and analyze electronic systems as well as design printed circuits. It is manufactured by Electronics Workbench, which is part of the National Instruments corporation. Multisim is a complete set of design instruments which encompass the following:

- graphic edition of diagrams,
- broad base of elements,
- simulation of analog systems,
- simulation of digital systems

The system is enriched with measuring instruments from the group of displays and indicators or series of tools. In the first case, these are voltmeters and ammeters, while in the second: a multimeter, signal generator, oscilloscope, curve tracer (Body's plotter),

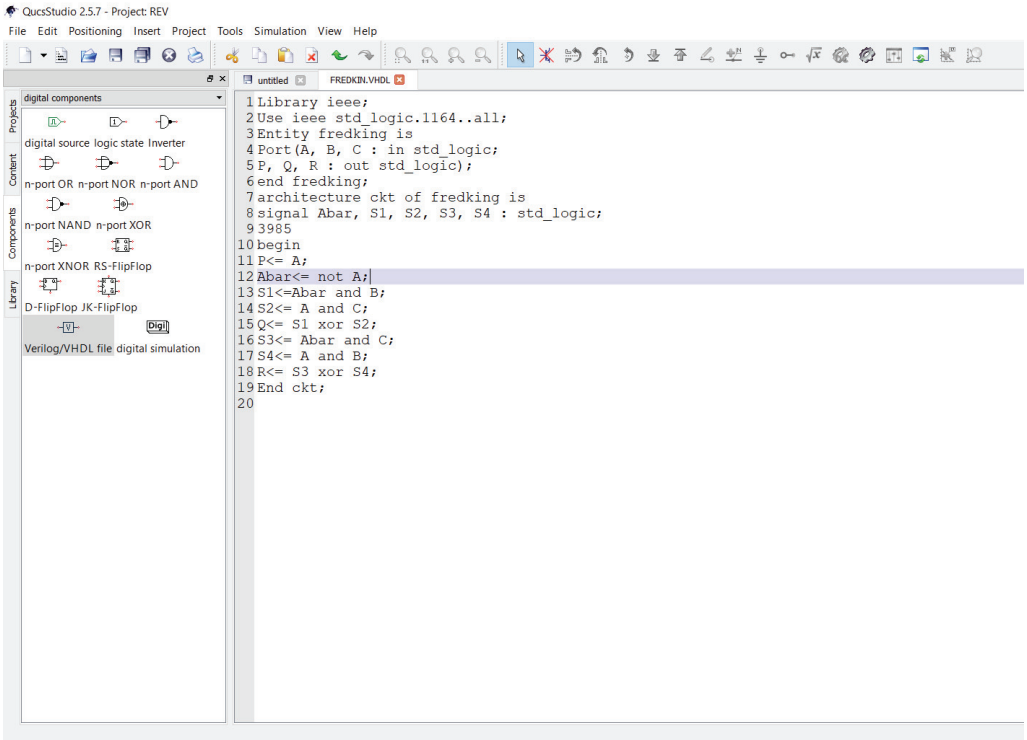

Fig. 6. Introduction of the Fredkin gate model in the QUCS program [own elaboration]

digital word generator, etc. This allows electric signals to be measured and observed in interesting points of the electric system. In the program, the process of defining new elements is simple. After selecting Tools/ Component Wizard in the options menu, the program guides you through the entire design process (jointly with symbols). Fig. 7 shows an example of creating a model for the Fredkin gate.

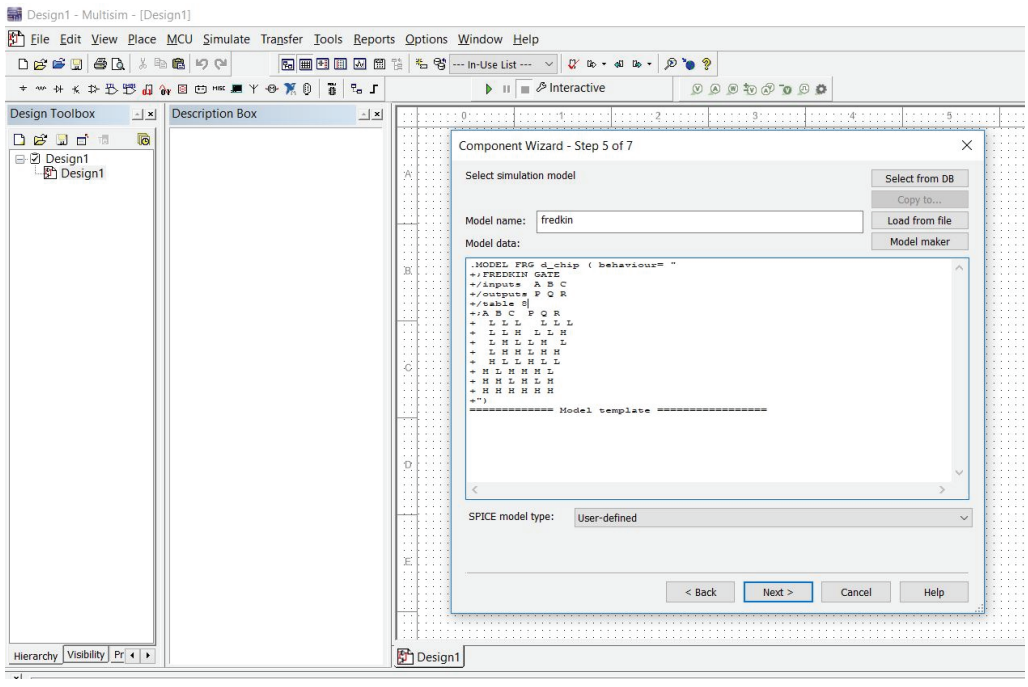

Fig. 7. Defining the Fredkin gate model in Multisim [own elaboration]

4. Safety of systems

The primary operation which ensures safety is the inspection of parity for all inputs and outputs of reversible gates. In its principles, this method is simple yet requires a considerable equipment surplus. Each input and output is connected to CNOT gates which perform operations for inputs and outputs. The result of the operation is stored on another signal line which starts with the value "0". If the test signal remains zero after going through all additional gates, the gate in question works properly. Otherwise it is possible to identify the faulty gate quickly and replace only the damaged element. However, this solution is not perfect; if any controlled negation fails (e.g. the last one), it will not be possible to detect the cause easily even in the case of a fault.

Being aware of potential hazards, such as a malfunctioning gate in the testing line, the classic method has been extended. If the parity is maintained, multiple XOR operation on the signal line will not change the initial value, the constant value "0" is changed into a signal whose value changes in time.

In such a situation, by changing logical "0" into logical "1" periodically – or by sending test impulses, you can check if CNOT elements work properly. This is a significant step in the process of building a reliable system.

As mentioned before, to ensure safety and reliable operation of the control system, a completely different technique is used. As a rule, input signals reach two independent processing channels (two separate systems performing the same function). For the outputs of these systems an active comparator is used to compare their results. If both values are identical, everything is fine. When there is a difference, it means one of the systems is erroneous or faulty. It is much less likely that both systems get damaged at the same time (and in the same way). As for reversible logic, we already know that it is possible to monitor the correct operation of each element separately. In addition, thanks to corrections made in the testing line, it is possible to check if its elements function correctly. Although the methods in question require considerable equipment load, they allow the identification of a fault to be fostered and improved substantially. Bearing in mind the features which result from reversibility, in one processing channel it is possible to achieve a similar effect to the one currently achieved in two. After creating a system from elements keeping parity (and supplementing it with testing), you can connect the same system in a reversed way in series. This is presented in Fig. 9.

In such a configuration, the same system is used twice, but in a mirror image. All outputs become in-

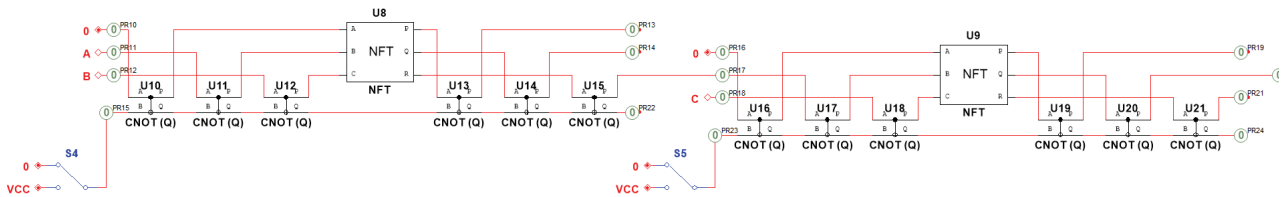

Fig. 8. Method of controlling parity in systems with reversible gates [own elaboration]

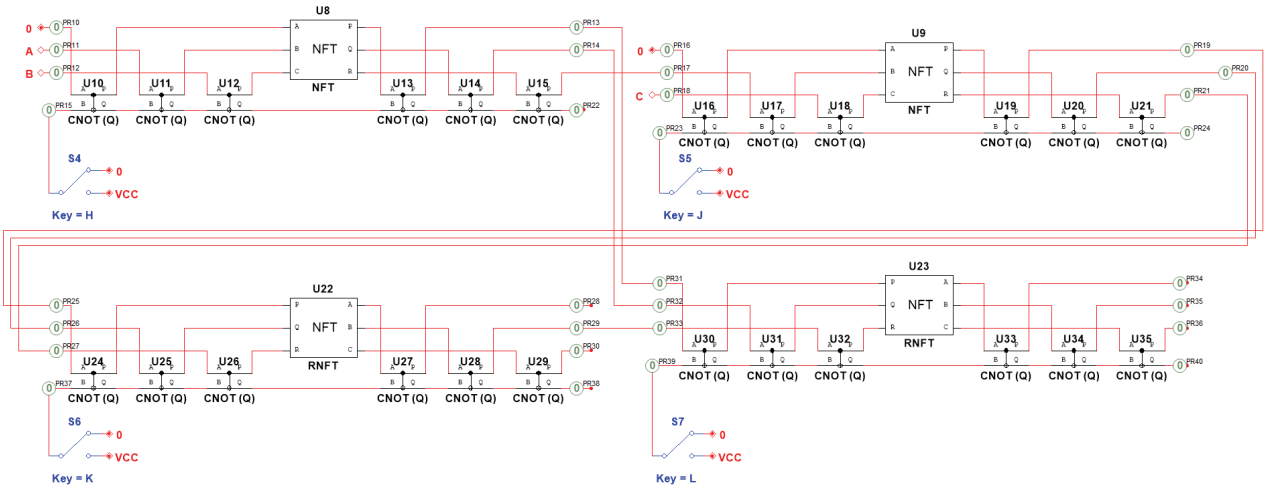

Fig. 9. Single-channel testing of proper system functioning [own elaboration]

puts, and the other way round. Using such a method, previously useless outputs become very important. Both parts of the system – standard and mirror – maintain parity and use the same testing methods in their operation. With such preparation, you can connect original inputs with mirror outputs via comparators – and thus monitor the correct calculation of each variable separately. In the event of a fault, you can easily identify the place of occurrence and its cause. Such an approach does not exclude the introduction of a new channel in order to have full redundancy in the event of any problems. Additionally, there is no need to abort operation even if the defect is eliminated easily.

5. Conclusion

Reversible logic, with its origins dating back to quantum physics, proves to have many applications in the world of two-value algebra. The substantially wider possibilities of systems with reversible logic in terms of testing and detecting faults (particularly when the system operates) are very useful in the case of synthesis of fault-tolerant digital control systems [10]. The dependence systems used in railway automatics systems usually perform simple logic functions (in the past a relay-based technique was sufficient for controlling). The use of reversible logic in SRK systems, as presented in the article, will allow safe single-channel systems to be prepared. This is of paramount important due to the possibility of performing control functions in digital programmable structures (FPGA), which will enable a substantial increase in the reliability of railway traffic control systems [5, 8].

Literature

1. Al Mahamud A., Begum Z., Hafiz M. Z., , Rahman M. M., Saiful Islam Md.: *Synthesis of Fault Tolerant Reversible Logic Circuits*, Proceedings of IEEE International Conference on Testing and Diagnosis, Chengdu, China, 2009, pp. 1–4.
2. Bruce J.W. et.al.: *Efficient adder circuits based on conservative reversible logic gates*. In Proceedings of IEEE Computer Society Annual Symposium on VLSI, Pittsburg, PA, 2002, pp. 83–88.
3. Haghparast M., Navi K.: *A novel fault tolerant reversible gate for nanotechnology based systems*. American Journal of Applied Sciences, Vol. 5, No. 5, 2008, pp. 519–523.
4. Haghparast M., Navi K.: *Design of a novel fault tolerant reversible full adder for nanotechnology based systems.* World Applied Sciences Journal, Vol. 3, No. 1, 2008, pp. 114–118.
5. Kawalec P., Szydłowski J., Mocki J.: *Realizacja wybranych algorytmów działania urządzeń srk w programowalnych strukturach logicznych* [Performance of selected algorithms of operation of SRK devices in programmable logic structures], International Scientific Conference Transport of the 21st century, Warszawa, 2001.
6. Landauer R.: *Irreversibility and heat generation in the computational process*, IBM Journal of Research and Development, Vol. 5, Issue 3, 1961, pp. 183–191.
7. Parhami B.: *Fault-Tolerant Reversible Circuits*, Proceedings of 40th Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, 2006, pp. 1722–1726.
8. Pniewski R.: *Metoda oceny bezpieczeństwa cyfrowych systemów automatyki kolejowej*. [Method of assessing safety of digital railway automatics systems], Monographs UTH, Radom 2013, ISSN 1642–5278.
9. Pniewski R., Kornaszewski M., Chrzan M.: *Safety of electronic ATC systems in the aspect of technical and operational*. 16th International Scientific Conference Globalization and Its Socio-Economic Consequences. Proceedings, Part IV. pp. 1729–1735. University of Zilina, The Faculty of Operation and Economics of Transport and Communications, Department of Economics, Rajecke Teplice, Slovakia, October 2016.
10. Santhi Swaroop V.G.: *Implementation of Optimized Reversible Sequential and Combinational Circuits for VLSI Applications*. Int. Journal of Engineering Research and Applications Vol. 4, Issue 4 (Version 1), April 2014, pp.382–388.
11. Siergiejczyk M.: *Wybrane zagadnienia systemów sterowania ruchem i łączności dla Kolei Dużych Prędkości w Polsce* [Selected issues of traffic control systems and communication for High-Speed Railway in Poland], Logistics 3/2012 pp. 1991–2022.
12. Taha S.M.R.: *Reversible Logic Synthesis Methodologies with Application to Quantum Computing*, Springer International Publishing, Switzerland, 2016.