Design of High-Performance PFD-CP for 403MHz CMOS Fractional-N Frequency Synthesizer

Sherif Saleh, Ghada Hamdy, Hamed Elsemary, and Amal Zaki

***Abstract*—This brief discusses the challenges and employs a novel charge-pump and a PFD/CP linearization technique to improve the performance of a 403MHz fractional-N PLL. Techniques are proposed to improve the linearity of the PLL by forcing the PFD/CP to operate in a linear part of its transfer characteristics, while the charge-pump minimizes the current mismatch between the up and down currents by using feedback. The circuit is designed in 0.13µm CMOS process and consumes a total power of 2.6mW. The simulation results show that the synthesizer has a phase noise of -128dBc/Hz at 1MHz offset.**

***Index Terms*—N-PLL; charge pump; current matching; PFD/CP**

I. Introduction

PHASE-LOCKED loop (PLL) is perhaps the most widely used mixed-signal circuit block in a silicon-on-a-chip and is regarded as one of the most power-consuming components. Fractional-N PLLs are employed in many applications. Unlike an integer-N PLL, the output frequency of a fractional-N PLL is not limited to integer multiples of a reference frequency. It has the benefits of fast locking, fine frequency resolution, and is able to accommodate various reference frequencies.

The operation principle of a fractional-N PLL lies in agitating the divide ratios to generate a fractional divider. The classical fractional-N PLL uses an accumulator to agitate the divide ratio [1]. However, this methodology suffers from the existence of fractional spur and the cancellation of quantization noise, which can be created due to periodical phase error and the existence of finite matching accuracy. In order to meet the strict performance requirements, a linearization technique for a phase frequency detector (PFD)/charge-pump (CP) is proposed. The proposed method tends to improve the linearity of the PLL by forcing the PFD/CP to operate in a linear part of its transfer characteristics, while the feedback is employed to minimize the current-mismatching in the charge-pump. This paper is organized as follows. Basics and challenges of fractional-N PL are described in section II. Section III discusses the circuit nonlinearity and linearity enhancement techniques. The proposed charge-pump design is reported in section IV. The simulation results and discussions are reported in section V. Finally, conclusion is drawn in section VI.

S. Saleh, G. Hamdy, H. Elsemary and A. Zaki are with the Department of Microelectronics, Electronics Research Institute - ERI, Al-Tahrir Street, Dokki, Giza, Egypt (e-mail: sherif_36@yahoo.com).

II. Fractional-N PLL Basics and Challenges

A fractional-N PLL, which is basically a variant of the prevalent integer-N PLL, is shown in Fig.1. Similar to an integer-N PLL, the control voltage Vctrl is adjusted by using a negative feedback and, hence, the oscillation frequency Fout of a voltage-controlled-oscillator (VCO). As depicted in Fig. 1 with the help of the PLL's output waveforms, illustrated in Fig. 2, the PFD compares the arrival times of the rising edges of the frequency divider output Fdiv with those of a low-noise periodic reference signal Fref. A charge-pump drives the low-pass loop filter with current pulses whose widths are proportional to the phase difference between the two signals. The pulses are filtered by the loop filter and the resulting waveform drives the VCO by adjusting the Vctrl.

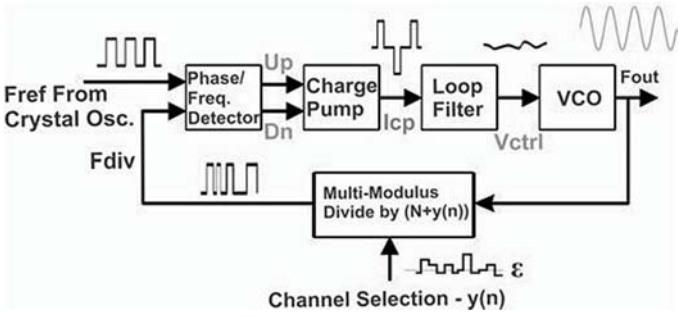


Fig. 1. A functional block diagram of a fractional-N PLL: It describes the operation principle of a fractional N-PLL, and the generation of the fractions y(n) through the use of a delta-sigma modulator in the feedback loop

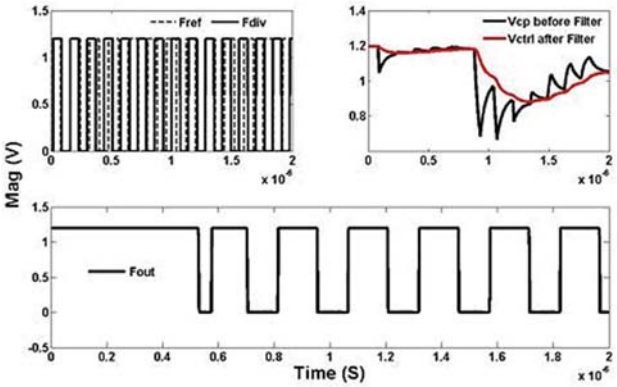


Fig. 2. Waveforms of the PLL explaining the circuit operation

III. Circuit Nonlinearity and Linearity Enhancement Techniques

Non-ideal circuit behavior and inescapable matching errors cause strong fractional spurs and quantization noise ”fold-in” in fractional-N PLLs.

A. PFD/CP Nonlinearity

Ideally, for every reference period, the combination of PFD and charge-pump injects an amount of charge into the RC-loop filter that is linearly proportional to the difference in phase (or time) between the PFD’s inputs. Certainly, the existence of many sources of error results in a nonlinear PFD/CP transfer characteristic. As shown in Fig. 3a, for small Δ T, the PFD may not respond at all resulting in the so-called PFD dead-zone.

The problem of the dead-zone is represented in the PFD transfer function in Fig. 3b. When the time difference between these signals is small (the PLL is locked), the first rising edge (Fref or Fdiv) will set the flip-flop. Due to propagation delays in the PFD, the second rising edge will reset the flip-flop before the signal has propagated to the output and the phase difference between Fref and Fdiv will not appear at the PFD output. Since the PFD is not able to detect phase differences smaller than ϕdz (Fig. 3b), the phase at the PLL output varies freely within this range, results in increased phase noise.

Moreover, the charge-pump might not immediately turn on fully, even though the PFD does respond. This result in an effective slope that is smaller than the nominal CP current ICP. Both of these issues can be alleviated by increasing the delay of the reset path inside the PFD loop [2]. This allows more time for the PFD and the charge-pump to respond. Charge-pump up/down current mismatch is a major contributor of non-linearity in a ΔΣ fractional-N PLL. Conventionally, long-channel devices are employed to avoid the effect of channel-length modulation and, consequently, improve current-matching accuracy. Nevertheless, the channel width must be scaled proportionally to maintain a low overdrive voltage. Hence, large transistors are used in the CP. This will occupy a large area and slow the circuit transient response; moreover this will require large switch buffers, which can greatly degrade the noise performance.

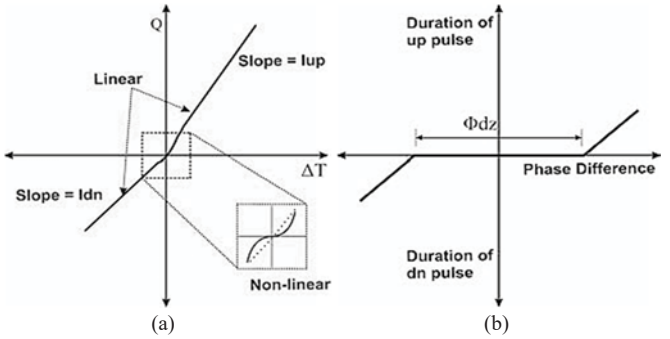


Fig. 3. (a) Sample nonlinear characteristics of the PFD/CP combination, (b) illustration of the dead zone

The mismatching in transistor size and the finite value of output impedance of the charge pump (CP), results in different slope up/down currents (Iup and Idn) for positive and negative time differences. A nonlinear error charge at every reference period will appear due to this mismatching. A popular solution for overcoming this issue, is to use amplifier-based negative feedback to match currents [3], but this technique is not an acceptable compromise due to headroom limitations.

Adding a dc offset current to the charge-pump [4], avoids nonlinearity by operating away from the nonlinear or the center region, i.e., ΔT=0. This increases the phase noise contribution of the charge-pump, which results in an undesirable hard reference spur. A sampled loop filter is presented in [4], which contributes to suppressing the reference spur. But this has its own particular challenges, such as charge injection and clock Feed-through effects. Another technique for repealing the reference spurs is to insert a notch filter between the loop filter and the VCO [2]. However, this approach introduces additional noise and changes the PLL closed-loop transfer function.

Using a variable-delay element in the PFD reset path is proposed in [5]. In this approach, to set the locked pulse width approach to zero, a feedback circuit is used to adjust the delay. Whereas the feedback of the added circuitry ensures that the overall PFD delay will be positive, but at the expense of increasing the size of the resistor in the feedback loop, this will introduce additional thermal noise, this resulting in phase noise degradation.

B. PFD/CP Linearization Technique

The design of PFD/CP presents nonlinearity. The conventional fractional-N PLL operates near a zero phase error center region while the loop is locked. However, the linearity near the center is frequently the worst [5]. Several efforts have addressed, by moving the operation region to a linear part of the transfer curve. This improves the system linearity. The shifting principle can be achieved by adding a dc offset current at the output of the CP [5], which moves the PFD/CP operation point from the center to a linear region. However, adding another active circuit at the charge-pump output will directly inject extra noise to the loop filter and may even alter the loop characteristics. In this work, a new approach is proposed to realize the shifting operation, whereby adding a dc current can be avoided. This is employed inside the PFD circuit rather than on the charge pump.

In Fig. 4a, an extra delay τ is added to the up reset path. This added delay forces the charging current of the charge-pump to remain ”on” for an extra duration τ , as shown in the timing diagram of Fig. 4b. This has the same purpose as adding a gated offset current to the PFD/CP, whereby, using the use of the actual current source is averted. Therefore, the same linearization effect as if an offset current were added is realized.

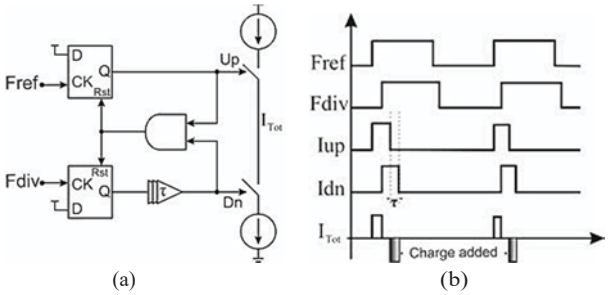


Fig. 4. PFD/CP linearization technique: (a) Adding a reset delay (τ) to the charging path, equivalent to as a virtual offset current, (b) timing diagram indicating the charge added due to τ

This method has one challenge: When the PLL is locked, a non-zero average phase error between F_{ref} and F_{div} may occur. This result in increasing the reference spurs. But certainly this is usually not a great issue, since the reference frequency is much higher than the PLL bandwidth and the designed high-order loop filter can suppress the reference spurs.

C. Proposed Charge-Pump Design

In this section, different techniques for improving the performance of the charge-pump are addressed. Feedback is employed to improve the mismatching in the charging and discharging current. Suppression of the output current variation and transient glitches are the most serious issues in designing the charge-pump. The Iup/Idn mismatch of the charge-pump is a major source of fluctuations in the input signal of the VCO, which results in large phase noise on the PLL output signals. Traditionally, long-channel devices have been employed to avoid the effect of channel length modulation and improve current- matching accuracy [1]. However, the transistor's width must be scaled proportionally to keep the overdrive voltage low. Therefore, large transistors are used in the charge-pump. Actually, large devices occupy a larger chip area. Moreover, this slows the circuit transient response and large switch buffers are needed, which can greatly degrade the circuit noise performance.

Compare the conventional charge-pump (represented with transistors Mn1, Mn2, Mp1, and Mp2), with the improved charge-pump circuit, shown in Fig. 5. Two additional feedback transistors, Mfn and Mfp, are added. The main idea is to incorporate a feedback into a small-sized charge-pump. This will achieve good current matching for area efficiency and minimizing unwanted transient effect. The operation of the modified circuit can be explained as follows: When the output voltage rises, the down current (Idn) increases, whereas the up current (Iup) decreases, based on the phenomenon of channel-length modulation. When the voltage increases further, the transistor Mfn enters the triode region eventually.

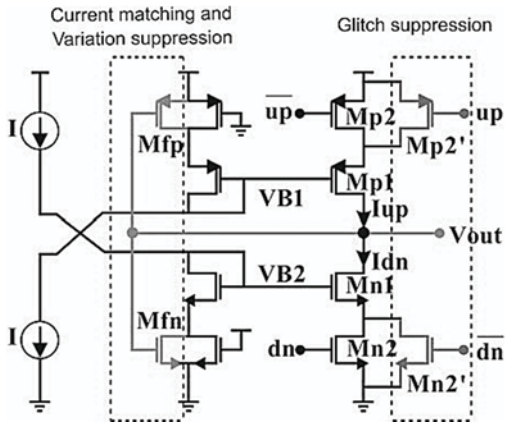


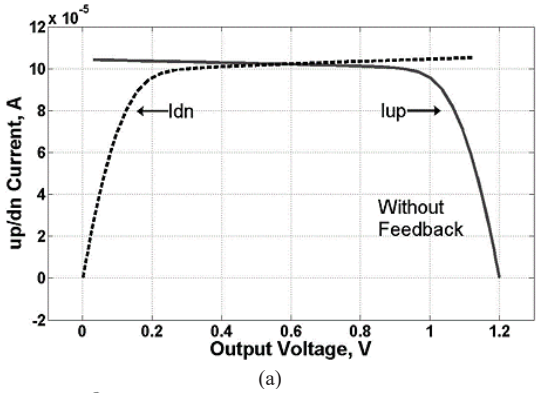
Fig. 5. Schematic diagram of the of the improved version of the conventional charge-pump circuit

The lowered device on-resistance reduces the amount of current mirrored to the output down-current branch, hence it reduces the difference between (Iup) and (Idn). Similarly, if the charge-pump output voltage decreases, the transistor Mfp enters the triode region. The lowered device on-resistance reduces the current mirrored to the output up-current branch and improves the Iup/Idn current matching.

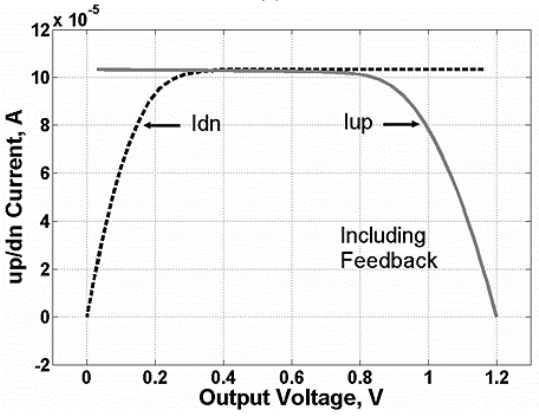
In order to suppress the glitches produced in the the charge-pump, two additional switch transistors (Mn2t and Mp2t) driven by the inverse of the signal driving the output node switch transistors are added. The transistors Mn2t and Mp2t match the size of the transistors of (Mn2 and Mp2). When both Mn2 and Mn2t stay in saturation region, they have the same overlap capacitance, Cgd. Thus, the glitches on the discharging current induced by the switching of the dn and dn cancel out each other. The same thing happens for glitches produced on the charging current provided by the pMOS devices (Mnp and Mnpt). Another advantage of this structure is that when the output switches (Mp2 and Mn2) are turned off, the currents Iup and Idn remain constant and are just steered to the other branch. This means that the voltages at the drain of the switching transistors stay approximately constant, which minimizing the charge sharing.

IV. Simulation Results and Discussions

Fig. 6a and 6b show respectively, the simulation results of the charge-pump Iup/Idn output currents without and with the feedback circuit, employed to suppress the current variation. By applying the feedback, the Iup/Idn current mismatch is reduced significantly and the current matching is improved without employing Op-amp to regulate the currents. It is also noticed that the variation suppression circuit significantly extends the range of the output voltage for a given variation tolerance.



(a)



(b)

Fig. 6. Simulated output current (a) without feedback circuit and (b) with feedback circuit

The phase noise is obtained when the PLL is configured as a fractional channel. The simulation results, shown in Fig. 7, reveal that the PLL has a phase noise of -130dBc at 1MHz offset with a carrier frequency of 403 MHz. The plot indicates that the synthesizer is quite linear; hence, the noise folding has no effect.

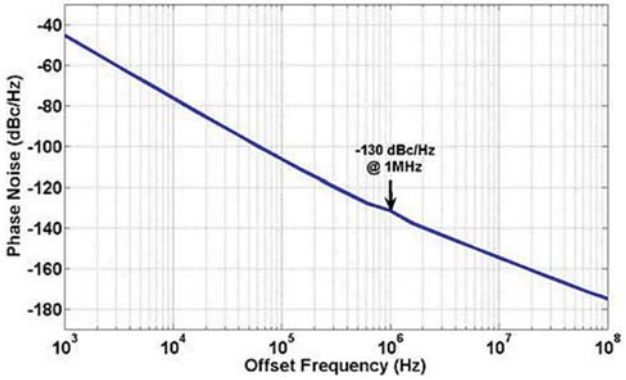


Fig. 7. Measured phase noise at 1 MHz offset from the 403 MHz carrier frequency

Fig. 8 shows the Monte Carlo analysis of the current matching characteristics when the output resistance of the nMOS and pMOS is not identical. The maximum difference of the Idn current decreases by 20% from the nominal value at 0.2V output voltage, when the 10% variation in the size of transistors is introduced to assume the process variation. From Monte Carlo simulation, and due to the process variation, it has also depicted that, there is a 2% mismatching between the charging and discharging currents in the voltage range from 0.2-0.8V.

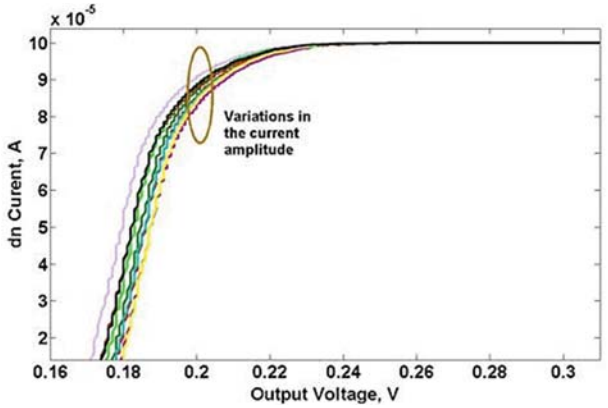


Fig. 8. Simulated results of the current matching (down current) characteristics

V. Conclusion

The fundamental operation and the current state of the art of fractional-N PLL-based frequency synthesizer has been presented with particular emphasis on fractional spur suppression. A novel charge-pump and a PFD/CP linearization technique are reported to improve the performance of a fractional-N PLL. The Iup/Idn current matching has been improved without using large current source devices. Furthermore, by simply adding an extra delay in the charging reset path, the PFD/CP operation is moved to a linear region, which avoiding the dead-zone and other non-linearity. With a carrier frequency of 403MHz, the simulated phase noise is -130dBc at 1MHz offset. The design consumes 2.6mW power from a 1.2V supply.

References

[1] H. Wang, G. Shou, and N. Wu, "An adaptive frequency synthesizer architecture reducing reference sidebands," IEEE Internationals Symposium on Circuits and Systems, 2006.

[2] K. Lakshmikumar, "Analog PLL Design With Ring Oscillators at Low-Gigahertz Frequencies in Nanometer CMOS: Challenges and Solutions," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 56, no. 5, pp. 389 –393, May 2009.

[3] J.-S. Lee, M.-S. Keel, S.-I. Lim, and S. Kim, "Charge pump with perfect current matching characteristics in phase-locked loops," Electronics Letters, vol. 36, no. 23, pp. 1907 –1908, Nov 2000.

[4] K. Wang, A. Swaminathan, and I. Galton, "Spurious-Tone Suppression Techniques Applied to a Wide-Bandwidth 2.4GHz Fractional-N PLL," IEEE International Conference on Solid-State Circuits, ISSCC, pp. 342–618, Feb. 2008.

[5] C. Charles et el., "A Calibrated Phase/Frequency Detector for Reference Spur Reduction in Charge-Pump PLLs," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 53, no. 9, pp. 822 –826, Sep 2006.

Sherif Saleh Mohamed received his BSc and MSc in Electrical Engineering, with emphasis on Electronics and Communications in 1999 and 2003, respectively, with honor degree from Al-Minia University, Egypt. Sherif Mohamed received the Dr.-Eng. degree from the Albert-Ludwigs-University, Freiburg, Germany, in 2012, both with highest honors. In 2000, he joined the Electronics Research Institute, ERI, Cairo, Egypt, where he was working as a research assistant in the field of low power analog circuit designs. In 2001, he awarded a scholarship from the Information Technology Institute, ITI, to study the VLSI diploma supported by the company of Mentor Graphics, Cairo, Egypt. In 2006, he moved to the Institute of Microsystem Technology, IMTEK, Albert-Ludwigs-University, where he was working toward the Ph.D. degree in the field of RF wireless receivers for medical implantable communication systems until 2012. Since March 2012 Dr. Mohamed is a Posdoc at the chair of microelectronics, IMTEK at the University of Freiburg. Dr. Mohamed' main research interests include analog-signal circuit design, RF wireless transceiver circuits for biomedical applications and Organic Thin-Film Transistors. He is an associate professor at the Electronics Research Institute.

Ghada Hamdy Ibrahim was awarded Bsc, Msc. and PhD from Faculty of Engineering, Cairo University, Electronics and Communications Department, 2000, 2005 and 2013 respectively. During this period, Ghada worked for R&D department, Bahgat group and then moved to Electronics Research Institute, Microelectronics department, where her research interests focused on RF circuit design for wireless sensor networks applications. Ghada joined MIMOS BHD, Malaysia from 2006 to 2008. Currently, Ghada is a junior fellow at Freiburg University, Germany, funded by FRIAS cofund program. She has more than 18 published papers. Her research interests spans RFIC design, printed electronics and MEMS design and microfabrication

Amal Zaki is currently a full professor at the Electronics Research Institute, Cairo, Egypt. She is the chairperson of VLSI Dept. She received her PhD degree from the University of Washington, Seattle, WA, USA & Cairo University in 1996. Her research interests include embedded system and real-time systems for Space applications, intelligent systems techniques. She runs several projects in cooperation with other universities and/or industry funded by NSF&EU. She teaches several courses on computer sciences and digital circuit design.

Hamed Elsimary is currently a professor at the college of computer engineering and science, Prince Sattam Bin Abdulaziz University, KSA. He received PhD. Degree in 1993from Cairo University and Rochester Instate of Technology, USA. His Research interest includes, low power VLIS design, and computer architecture.