Analysis and Investigation of Schottky Barrier MOSFET Current Injection with Process and Device Simulation

Mike Schwarz, Laurie E. Calvet, John P. Snyder, Tillmann Krauss, Udo Schwalke, and Alexander Kloes

***Abstract*—In this paper we focus on the implementation of a process flow of SB-MOSFETs into the process simulator of the Synopsys TCAD Sentaurus tool-chain. An improved structure containing topography is briefly discussed and further device simulations are applied with the latest physical models available. Key parameters are discussed and finally the results are compared with fabricated SB-MOSFETs in terms of accuracy and capability of process simulations.**

***Index Terms*—2D Poisson equation, device simulation, field emission, modeling, MOSFET, process simulation, Schottky barrier, Synopsys, TCAD, thermionic emission, tunneling current**

I. Introduction

NOWADAYS, the semiconductor industry is dominated by device structures such as Intel's tri-gate [1], and fully-depleted SOI devices [2]. These multi-gate devices enhance electrostatics and address short-channel effects (SCEs) and device performance degradation. Today gate lengths in FinFET technology below 10nm are state-of-the-art [3], [4].

However, there remain some important issues that still need to be considered. One of these technological limits that continues to present an important obstacle is the increased impact of source/drain (S/D) parasitic resistances [5]. One solution is to consider changes in device technology and in particular the device structure.

In this context the Schottky barrier (SB) MOSFET is a very promising candidate to enhance the transistor performance due to its metallic S/D electrodes with low specific resistances and high scalability even down to the sub-10nm region. Its good process compatibility with standard CMOS technologies makes this concept still very attractive.

Schottky barrier MOSFETs offer additional advantages such as substrate leakage improvements and low temperature enhancements due to the presence of the Schottky barrier. These lead to a reduced channel doping, typically used to control the off-state leakage currents and thus improved mobility, as well as reduced junction and gate capacitances. This results in substantial power and speed performance improvements [6], [7].

Besides, more effects like the important Schottky barrier effect of the image force induced lowering of the barrier, also known as the Schottky barrier lowering (SBL) effect [8] have to be taken into account [9], [10].

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As the reader now can observe, various effects impact the device performance of Schottky barrier devices. All these effects have to be considered in a numerical analysis of Schottky barrier MOSFETs by implementing the process flow and using appropriate physical models in a TCAD tool in order to allow eventually for an accurate analysis of the device's performance.

The demand and challenges of such technologies encourage researchers and device designers to optimize devices with the help of process and/or device simulations. As shown by the various publications [5], [11], steps such as channel implants to suppress leakage current in bulk devices are required to enhance device performance behavior. However, these proposals are a guess from experiences. Process simulation can optimize these questions in a way, to define the optimal implant in terms of dose, energy, tilt, etc. Furthermore, diffusion and thermal budget process steps are taken into account during the optimization process and for the optimal process design. Especially, for and in industry one should remember that before a device is built into silicon, more than 80% of the work is supported by simulation and yield predictions.

In the past, various numerical studies of Schottky barrier MOSFETs have been published based on device simulators like Synopsys TCAD Sentaurus [12]. In general such numerical studies [9], [13], [14] deal with ideal device geometries. They for example assume optimal metal-to-semiconductor junctions for the Schottky barriers, which finally lead to an ideal device performance under perfect conditions. Such simulations always offer the best case of those device simulations

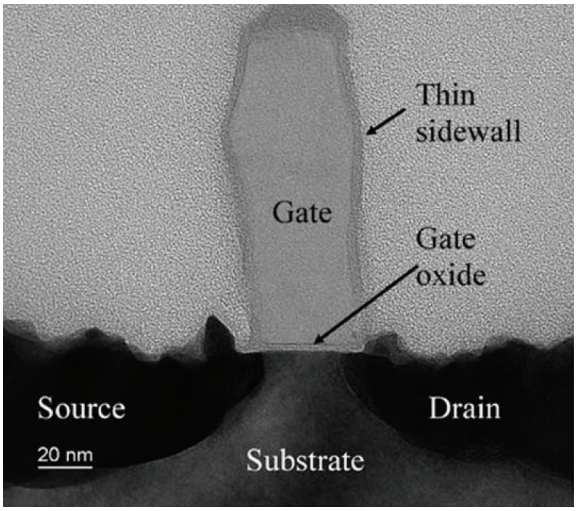

Fig. 1. High-resolution cross-section TEM of a 22nm SB-PMOS device [5], [11].

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from the geometrical point of view. However, reality shows that such interfaces are not ideal, they consist on interfacial effects and topography which result during the silicidation process and the interaction between metal/silicide and the semiconductor caused by lattice mismatches, etc. as shown in Figure 1 by [5], [11].

To account for such topography and interfacial impacts, in this paper a first implementation of a bulk Schottky barrier MOSFET into the process simulation of the Synopsys TCAD tool-chain is presented to account for a more precise estimation, as shown in Figure 2. Furthermore, different important process steps are analyzed in terms of their impact and linked with expectations from experienced process engineers. To the best of our knowledge, this is done for the first time. Furthermore, effects such as ambipolar behavior from e.g. the drain as shown in Figure 3 are taken into account in the analysis.

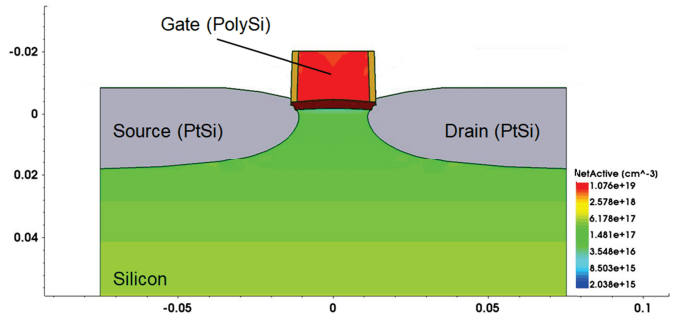

Fig. 2. Simulation of a 25nm SB-PMOS device with retrograde channel implant due to the process flow of [5], [11].

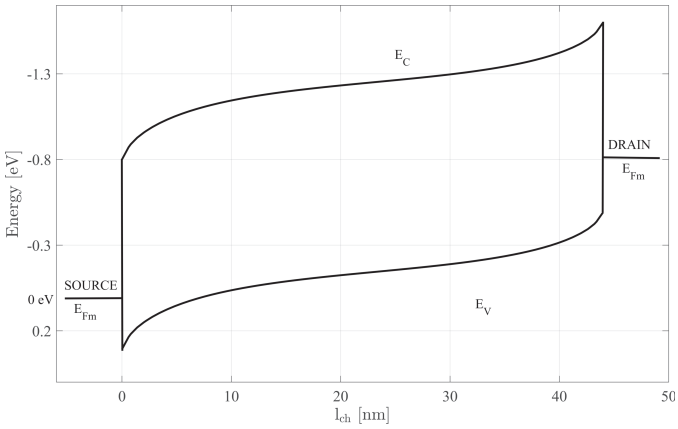

Fig. 3. Typical band diagram of a PMOS Schottky barrier MOSFET including ambipolar behavior for bias $V_{ds} < 0$ at the drain junction.

II. Process Simulation

In this section the aim is to implement a typical process for Schottky barrier devices into a process simulation compatible language. Therefore, we focus in a first step on Schottky barrier bulk devices, however it is optional to translate the flow also into multigate or fully-depleted SOI structures. An alternative model process flow compared to [16] for a PtSi Schottky barrier MOSFET with channel length of $l_{ch} = 25nm$ is given in Figure 4.

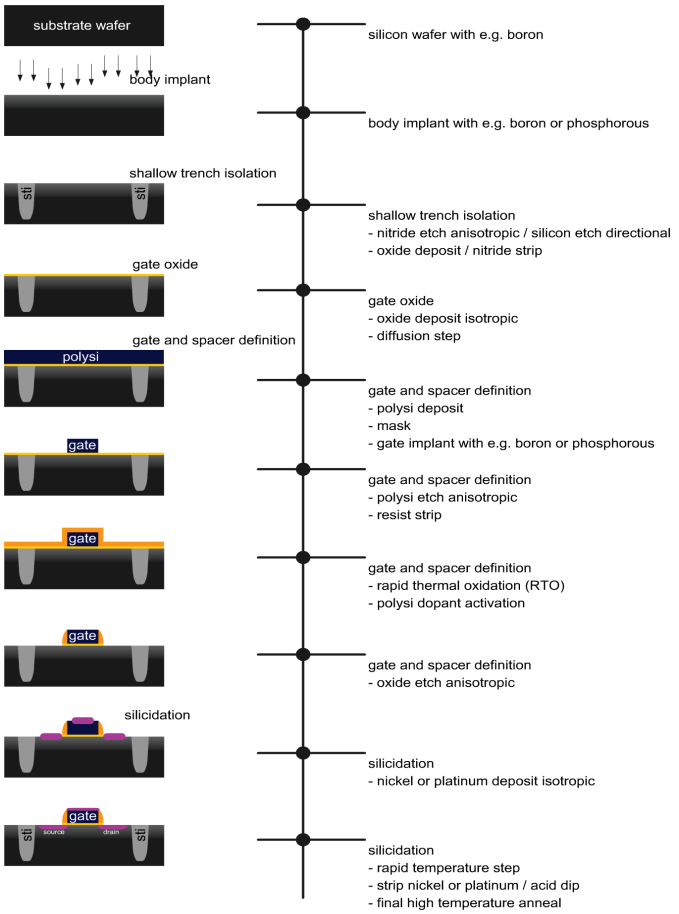

Fig. 4. Possible process flow for a PtSi Schottky barrier MOSFET with channel length of $l_{ch} = 25nm$.

A. SB-MOS Process Flow

The Schottky barrier device differs slightly compared to a standard CMOS process. Larson and Snyder [5] give some detailed overview of the various process steps and differences. In the following a brief introduction is given with the focus on the process simulation flow. It is obvious, that some process steps can be changed in their order.

The CMOS process starts with the bulk silicon wafer. First, a body implant is provided by standard well implants and channel implants. According to [5] a retrograde channel implant with a peak dopant concentration of approximately $10^{18} - 10^{19}cm^{-3}$ located at a depth of approximately $25 - 100nm$ below the gate insulator is required to suppress leakage from the substrate in bulk devices. Additionally, the retrograde channel implant should provide a dopant concentration of $10^{16} - 10^{17}cm^{-3}$ below the gate insulator $(0 - 10nm)$. Here, a majority of the mobile charge flows from source to drain and by the reduced channel doping an improved effective carrier mobility is obtained.

After the channel implant a local oxidation of silicon (LOCOS) or shallow trench isolation (STI) process follows, while here the second one is considered. First a shallow trench isolation (STI) etch, which is done generally by a nitride deposit, a mask definition and an anisotropic etch of the nitride plus a directional etch of the silicon is provided. Afterwards, a fill of the STI is made by an oxide deposition and a final strip of the nitride.

It follows a dual-doped polysilicon or metal-gate process. An oxidation process step to build the gate oxide is provided. Afterwards, polysilicon is deposited, the gate mask applied and then the polysilicon is structured anisotropically. An isotropic nitride deposit and an anisotropic nitride etch are then followed by an anisotropic oxide etch. The spacers consist of nitride. Alternatively, lithography and etch can be used to form the gate in combination with the oxidation process. A thin ($< \ 10\text{nm}$) sidewall spacer is formed on the gate and an anisotropic sidewall spacer etch exposes the active regions.

The thin sidewall spacer helps minimize S/D-to-gate underlap so that the SB junctions to the channel region are in close proximity to the gate electrode. The result is an optimized capacitance due to junction proximity to the gate minimizing the parasitic junction resistance induced by underlap, a minimized overlap capacitance, and minimizing the gate-induced drain-leakage current [5].

Different from a standard CMOS process flow the implant and diffusion process is replaced by a silicidation process step. Here, depending on the body implant and the target Schottky barrier the material silicidation varies from platinum, nickel or erbium, etc. A standard sputter-deposition tool can be used for platinum or erbium deposition to thicknesses of approximate $10 - 50\text{nm}$. A $400 - 500°\text{C}$ 1h furnace anneal forms the silicide. Unreacted platinum, nickel or erbium unreacted with silicon is removed by a selective strip. Alternatively, a RTA (rapid thermal anneal) process with a shorter annealing time of $5 - 10\text{min}$ can be used for silicidation.

B. Process Flow to Simulation

To account for the process flow as explained above, one has to translate into the language that is supported by the vendor of the simulation tool. Independently of the vendor, the commands to account the different process steps are rather simple. For example the wafer is initialized as follows:

```
init wafer.orient= 100 field= Boron concentration= 2e15
```

The channel implant which is used to realize a retrograde channel implant may look like:

```
implant Boron dose= 2e13 energy= 70 tilt= 7 rotation= 22
```

There exists a various set of command which are used to translate the process flow to process simulation. These commands are found within the manual, e.g. Synopsys TCAD Sentaurus Process [12]. A brief overview is given in Table I.

TABLE I
PRIMARY USED SYNOPSYS TCAD SENTAURUS PROCESS COMMANDS TO REPRESENT THE SB-MOS PROCESS FLOW

command	function
deposit	deposition of a defined material including a defined thickness
etch	anisotropic or isotropic etch of defined material including a defined thickness
mask	mask definition for etch, implant, deposition, etc.
diffuse	diffusion process, e.g. single step or a ramp
strip	strip of a defined material
implant	implantation process of species, e.g. boron or phosphorous
contact	contact definition, e.g. for a silicidation area

A silicidation process for e.g. nickel silicide is represented partially as follows:

```
deposit Nickel type= isotropic thickness= 0.03
...
diffuse time= 3600<s> temp= 450<C>
strip Nickel
```

The difficulty begins with the calibration of the process itself. Here, the vendors offer a set of various parameters for each command to adjust the models to reality. This is caused by the difference in each process. Even, if the e.g. the implant models behind the process simulator are calibrated by the Tasch Tables [15], [17], [18] for Dual Pearson models, the process differ from fab to fab and tool to tool. This is the reason why measurement techniques such as SIMS (Secondary Ion Mass Spectrometry), SPR (Spreading Resistance), TEM (Transmission Electron Microscope), STEM (Scanning Transmission Electron Microscope), REM (Reflection Electron Microscope) are required to calibrate the process in terms of diffusion and/or segregation coefficients.

C. Model Process Simulation

The model process flow of Figure 4 is applied in Synopsys TCAD Sentaurus Process and various steps of a half model are visualized for further discussion.

In Figure 5 one can observe the process steps of channel implantation, STI, polysilicon gate process, and nitride sidewall spacer. The structure of shallow trench isolation (brown), polysilicon gate (magenta) and nitride spacers (gold) are clearly visible.

An intermediate process step is shown in Figure 6, where the silicidation process is running. One can see the silicidation progress of the nickel silicide (silver) in the source/drain and gate region. On top the overall deposited nickel (beige) offer is visible.

After the final diffusion the remaining non reacted nickel is striped away and a final RTA follows. This process step is shown in Figure 7, where one easily can see the resulting silicidation areas at source/drain and gate.

Finally, the half model is extended to a full model as shown in Figure 8. Here, it is obvious where the source and drain regions are. Additionally, one can clearly see the resulting topography of the silicide, spacers, etc. and may compare to the TEM of Figure 1.

With such results for a SB process now one can apply the device simulation with all the different physical models for e.g. Schottky barrier lowering, non-local tunneling, etc. as many papers [10], [19], [20], [9] offered for ideal structures and investigate different aspects of a Schottky barrier device. Especially, the impact of sidewall spacers on device performance caused by the under/overlap can be analyzed, or the retrograde channel implant as suggested by [5] can be understood in more detail and improved if necessary. Also, the study of physical insights, e.g. where the maximum tunneling of carriers at the metal-to semiconductor interface occurs can be used to improve and simplify compact models and/or equations. This can be a huge benefit of more detailed structure implementations by process and device simulations.

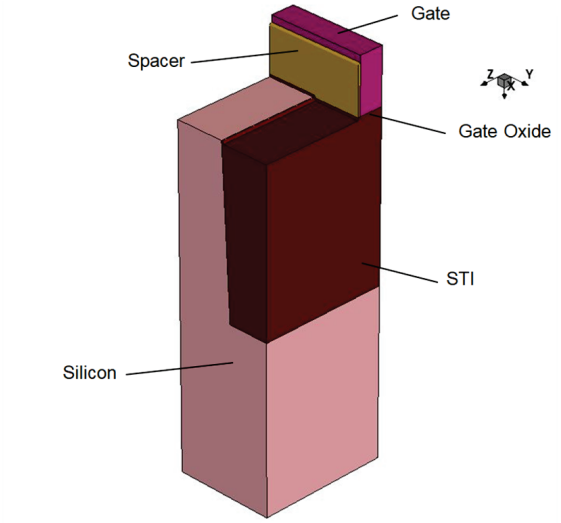

Fig. 5. Half model of the process steps: channel implantation, STI, polysilicon gate process, and nitride sidewall spacer.

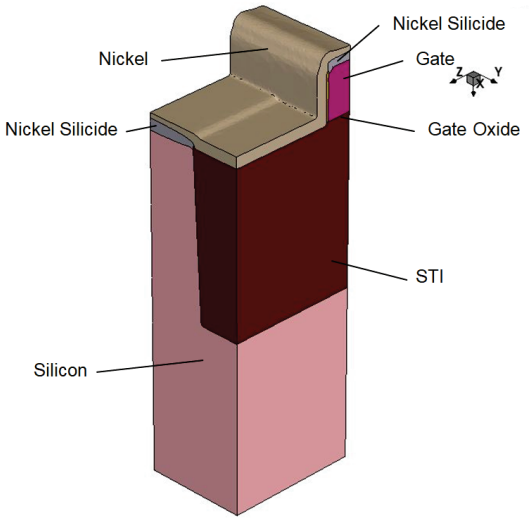

Fig. 6. Half model of the process steps: nickel deposition and nickel silicidation.

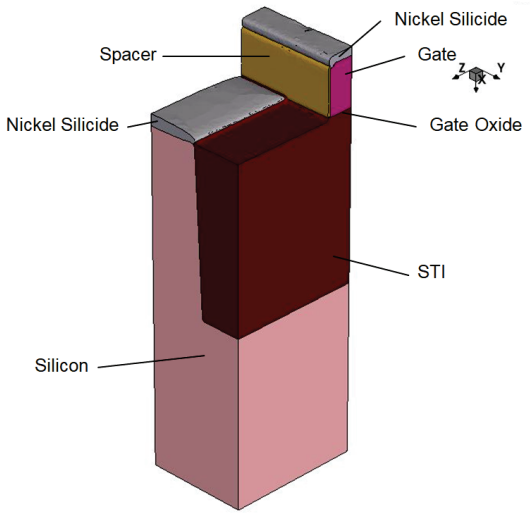

Fig. 7. Half model of the process steps: nickel strip and RTA.

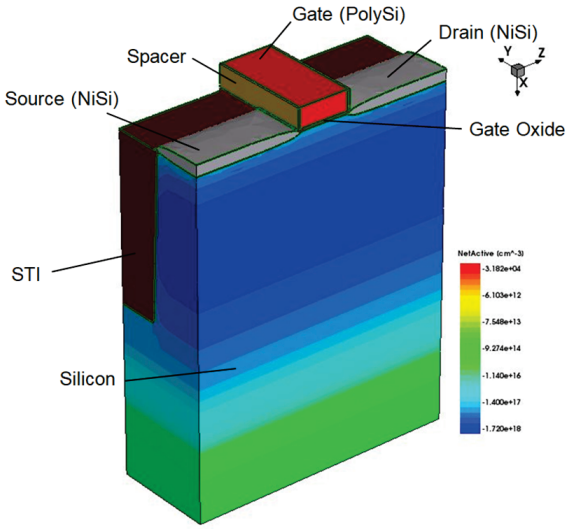

Fig. 8. Full process model after the model process flow.

III. Investigation with Device Simulation

Within this section the device created by the process simulation above is further investigated with device simulations. Here, especially the tunneling generation rate at the silicide interfaces for different bias conditions is in focus.

Within the TCAD simulation environment the following models were activated: Fermi distribution, doping dependency on mobility, high field saturation on mobility, mobility degradation at interfaces, bandgap narrowing on effective intrinsic density in terms of old Slotboom model, lattice temperature, nonlocal tunneling at metal-semiconductor interfaces including SBL.

In the Figures 9 to 12 a model PtSi Schottky barrier MOSFET is shown, where the contacts of platinum silicides are hidden for better visualization.

If one compares Figures 9 and 10, the Tunneling Generation Rate (TGR) for holes at the source and drain interfaces are visualized. Both plots differ in terms of bias conditions for V_{ds}, where the shown operational points visualize the on-state behavior for the Schottky barrier PMOS. Here, one can see that the main impact is concentrated underneath the contacts with a proximity to the gate. This finally leads to the behavior shown in Figure 3 if one slices from source to drain (z-direction) underneath the gate oxide. In the on-state the impact mainly corresponds to holes at the aligned gate to source. This is also observed in the legend, which shows the large amount of carriers from the TGR.

Furthermore, one can see the difference in terms of V_{ds}. For low $V_{ds} = 0.05V$, the tunneling current density is smaller, as expected from the band bending, which results in a smaller tunneling probability due to the larger distance for the carriers at a specific energy level to tunnel. The larger the V_{ds} (Figure 3), the higher the band bending at the source for the valence band, the higher the TGR for the holes. The amount and distribution along the source contact in the change is observed as well. The corresponding electron TGR (not visualized) is of several magnitude lower and therefore does not significantly contribute to I_d.

The situation changes, if one analyze and investigate the TGR in the off-state as shown in Figures 11 and 12. In the

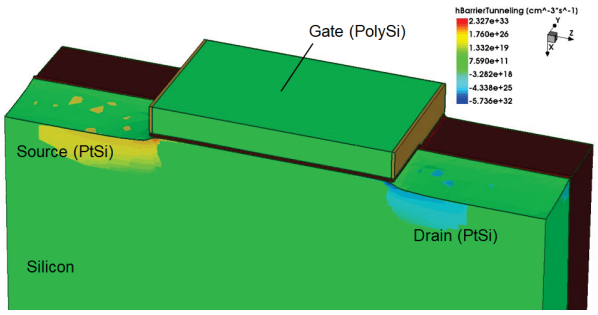

Fig. 9. Tunneling generation rate for holes at the source and drain interfaces. Bias conditions: $V_{ds} = -0.05V$, $V_g = -2V$ (on-state).

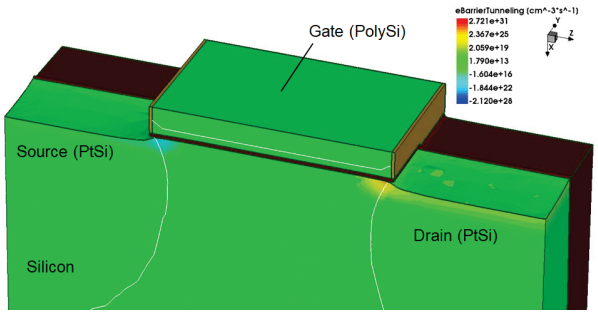

Fig. 11. Tunneling generation rate for electrons at the source and drain interfaces. Bias conditions: $V_{ds} = -0.05V$, $V_g = 1V$ (off-state).

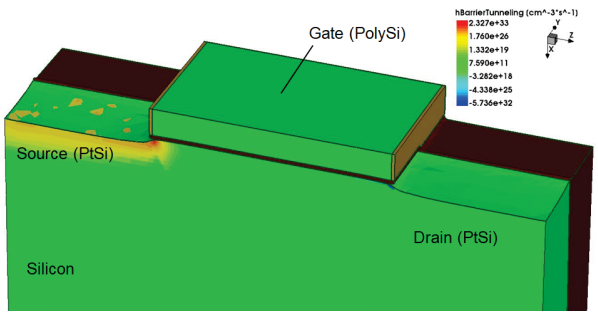

Fig. 10. Tunneling generation rate for holes at the source and drain interfaces. Bias conditions: $V_{ds} = -1V$, $V_g = -2V$ (on-state).

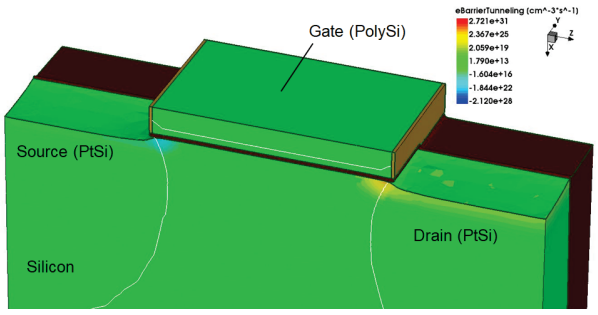

Fig. 12. Tunneling generation rate for electrons at the source and drain interfaces. Bias conditions: $V_{ds} = -1V$, $V_g = 1V$ (off-state).

off-state the ambipolar behavior dominates. The hole TGR is decreased and negligible (not visualized) and the electron TGR increases caused by the drain-side band bending impact. As one can observe for the plots with $V_{ds} = 0.05V$ (Figure 11) and $V_{ds} = 1V$ (Figure 12), the main impact occurs at the drain contact in the proximity of the gate, where the influence of the gate is highest. The more one moves away, the less TGR results. This explains why ambipolar impact can be suppressed by gate to drain spacer engineering.

However, one has to consider further influences besides the ambipolar behavior. The leakage current influence from the substrate plays a significant role the shorter the channel length becomes. This is caused by lowering the influence of the gate on the channel. This finally leads to an increased leakage current for this modeled process flow. Nevertheless, the Fermi distributions for a final statement have to be taken into account.

In general, if one wants to improve the ambipolar impact by a decrease of several orders of magnitude, it is obvious to degrade the gate impact onto the drain contact. Finally, it can be derived by comparing Figures 9 and 10, that the amount is mainly concentrated for the on-state nearby the gate region, where the Tunneling Generation Rate for holes at the source and drain interfaces are visualized. This is clear, because the Schottky barrier for the electrons is in the range of $\phi_{Bn} \approx 0.8eV$, while it is for the holes in the area of $\phi_{Bp} \approx 0.22eV$ for PtSi.

IV. Comparison with Measurements

Figure 13 illustrates the $I_d - V_g$ device simulation results for a process flow from [21] for PtSi Schottky barrier MOSFET devices with layout channel lengths of $l_{ch} = 500nm$ and $l_{ch} = 240nm$.

SEM/TEM measurements revealed that the long channel length devices with layout $l_{ch} = 500nm$ had effective channel lengths of $l_{ch,eff} \approx 300nm$, $t_{ch,eff} \approx 20 - 30nm$, $t_{ox,SiO_2} \approx 2.5nm$ and for the short channel device effective channel lengths of $l_{ch,eff} \approx 50nm$.

Within the simulation environment a channel length of $l_{ch,simulation} \approx 180 - 200nm$, $t_{ch,eff} \approx 20nm$, was used to accurately fit the slope of the thermionic emission (TE) from the measurements. The transition point (Fig. 13) of thermionic emission (TE) to field emission (FE) was almost unaffected by the channel length change, because it primarily depends on barrier height for longer channel devices. The small channel device within the simulation was adjusted to $l_{ch,simulation} \approx 40nm$ to fit the measurements.

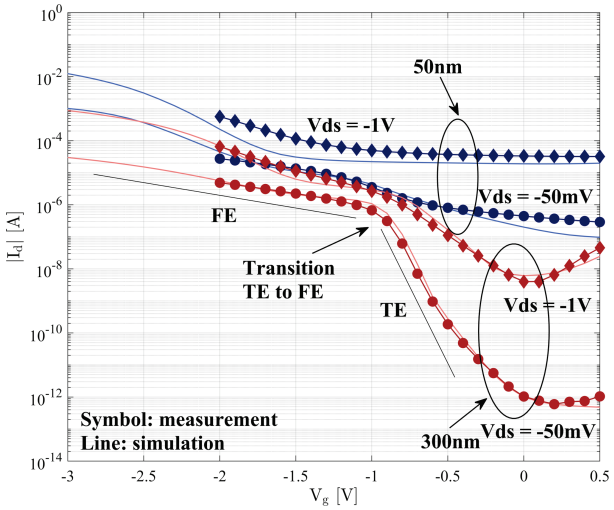

Fig. 13. $I_d - V_g$ with $\phi_{Bp,PtSi} \approx 0.22eV$ from [21] for SB devices with channel layout length of $l_{ch,eff} = 300nm$ and $l_{ch,eff} = 50nm$.

As one can clearly see, the general behavior of the simulation in terms of transition between thermionic emission and field emission and slope fits well with the measurement data of Calvet et al. However, especially for the long channel device the difference between layout and simulation is significant and does not fit to the experiments. This is caused by a too optimistic gate influence, which finally suggests that the active gate length is far less than the layouted one.

What one also may observe from the $I_d - V_g$ curves, the shorter the channel length, the higher the leakage current from the substrate. If one wants to improve the device behavior and suppress the leakage current, a channel implant to suppress the leakage influence from the substrate is required.

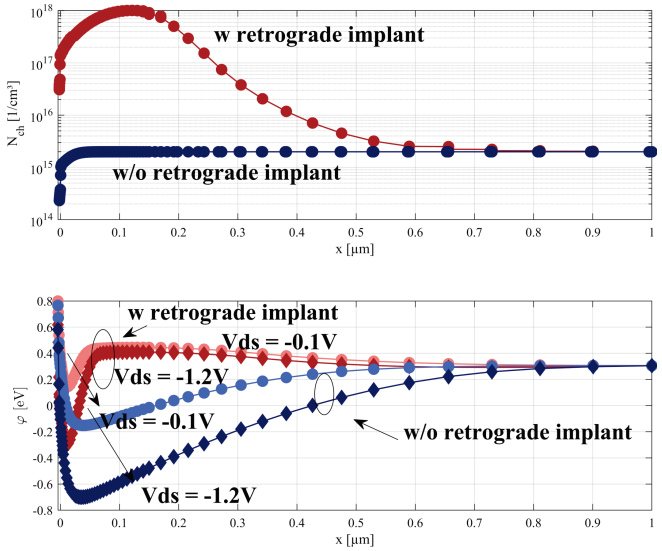

Fig. 14. Channel doping N_{ch} with and without a retrograde channel implant and electrostatic potential φ for a SB device with channel length of $l_{ch,eff} = 25nm$ with $\phi_{Bp,PtSi} \approx 0.22eV$ from [5].

This can be observed for a retrograde channel implant with phosphorus and a dose of $2 \cdot 10^{13}/cm^2$ with an implant energy of $120keV$ for a PtSi Schottky barrier MOSFET device with a channel length of $l_{ch,eff} = 25nm$ and a barrier height of $\phi_{Bp,PtSi} \approx 0.22eV$ from [5].

Figure 14 shows the doping distribution of the simulated device with and without channel implant for a slice gate oxide to bulk silicon in the middle of the device. Below the corresponding electrostatic potential is shown for $V_{ds} = -0.1V$ and $-1.2V$ with $V_g = 0.5V$ for the off-state. One can clearly see, that the channel implant influences the solution of Poisson's equation and therefore the electrostatics e.g. the threshold voltage, etc. The influence of the substrate is screened by an increased potential barrier.

In Figures 15 and 16 one can see the hole current density distributions within a slice of the device described before but without the retrograde channel implant. The hole current density is of interest, because the leakage current in Figure 13 for $V_g = 0.5V$ is caused by holes. One observe that for both $V_{ds} = -0.1V$ and $V_{ds} = -1.2V$ an increased current density occurs within the bulk silicon, which is orders magnitudes higher compared to the current density underneath the gate oxide. The space charge region (not visualized) is located deep in the bulk, which has an increased impact from the substrate potential for the short channel device. This is a common behavior for bulk short channel devices, where the impact of source and drain impedes the electrostatic control of the gate on deeper channel regions.

In Figures 15 to 18 the corresponding results for the off-state current densities indicating where the substrate leakage current occurs are given for simulations with/without the retrograde channel implant as described before.

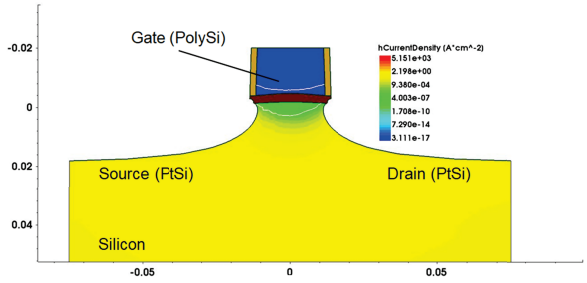

Fig. 15. Hole current density distribution for a SB-MOSFET with $\phi_{Bp,PtSi} \approx 0.22eV$ from [5] with a channel length of $l_{ch,eff} = 25nm$ and a retrograde channel implant. Bias conditions: $V_{ds} = -0.1V$, $V_g = 0.5V$ (off-state).

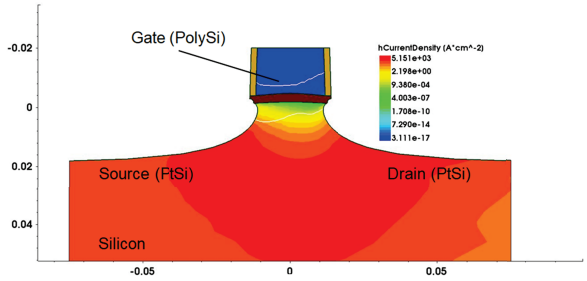

Fig. 16. Hole current density distribution for a SB-MOSFET with $\phi_{Bp,PtSi} \approx 0.22eV$ from [5] with a channel length of $l_{ch,eff} = 25nm$. Bias conditions: $V_{ds} = -1.2V$, $V_g = 0.5V$ (off-state).

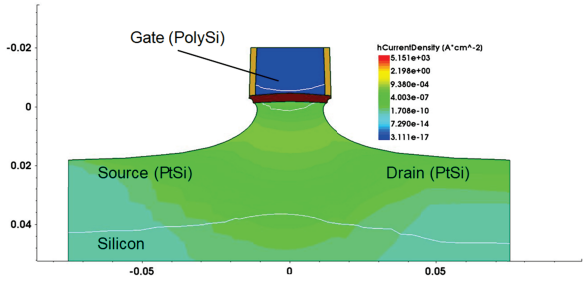

Fig. 17. Hole current density distribution for a SB-MOSFET with $\phi_{Bp,PtSi} \approx 0.22eV$ from [5] with a channel length of $l_{ch,eff} = 25nm$. Bias conditions: $V_{ds} = -0.1V$, $V_g = 0.5V$ (off-state).

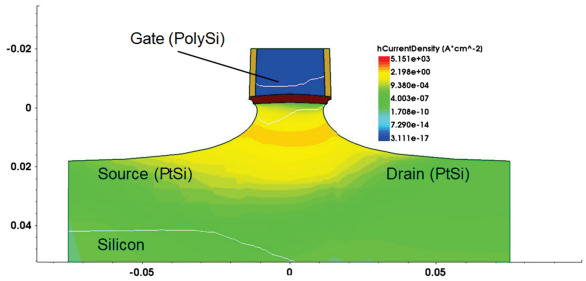

Fig. 18. Hole current density distribution for a SB-MOSFET with $\phi_{Bp,PtSi} \approx 0.22eV$ from [5] with a channel length of $l_{ch,eff} = 25nm$ and a retrograde channel implant. Bias conditions: $V_{ds} = -1.2$, $V_g = 0.5V$ (off-state).

If one now implants a retrograde channel, e.g. a channel implant with phosphorus and a dose of $2 \cdot 10^{13}/\mathrm{cm}^2$ with an implant energy of $120\mathrm{keV}$, the behaviors as visualized in Figures 17 and 18 result. The hole leakage current is reduced several orders of magnitude for both $\mathrm{V_{ds}} = -0.1\mathrm{V}$ and $\mathrm{V_{ds}} = -1.2\mathrm{V}$. The channel implant, located with its peak concentration approximately between $50\mathrm{nm}$ to $100\mathrm{nm}$ screens the influence from the substrate (Fig. 14) and reduces therefore the leakage current. The dominating current flow results between the source and drain silicides, approximately $10\mathrm{nm}$ to $20\mathrm{nm}$ underneath the gate oxide. This indicates still an increased short channel impact. However, the retrograde channel implant improves the device off-state behavior.

This improvement is clearly observable by the comparison of the $\mathrm{I_d} - \mathrm{V_g}$ curves as shown in Figure 19. If one considers e.g. a retrograde channel implant and some minor process changes as a final high temperature anneal, one receives an improved device behavior. The improvement is clearly observed even lower channel lengths compared to the devices of [21], where no retrograde channel implant was considered within the process flow to suppress the substrate leakage current. Within the figure one can observe two major statements. First, process simulation is able to capture the device behavior in good agreement to measurement data. Second, physical effects on the device performance due to process improvements as discussed above are accurately predicted.

As one can observe, the small process change within the simulation explains from the physics point of view the device behavior. It enables further analyses in terms of device improvements by process and device simulations. Especially for limited design of experiments (DOEs) where experimental variations are rarely available due to limited resources.

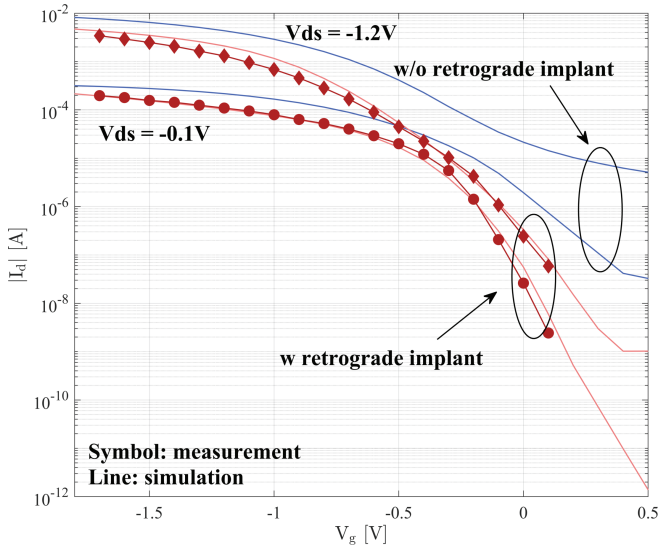

Fig. 19. $\mathrm{I_d} - \mathrm{V_g}$ with $\phi_{\mathrm{Bp,PtSi}} \approx 0.22\mathrm{eV}$ from [5] for a SB device with channel length of $\mathrm{l_{ch,eff}} = 25\mathrm{nm}$ with and without a retrograde channel implant of $\mathrm{N_{ch}}$.

V. Conclusion

A methodology to account for more precise and realistic SB-MOSFET process simulations was presented. We demonstrated the capability of such simulations to match experimental data.

Furthermore, the physical impact of retrograde channel implants on the device off-state behavior of the substrate leakage current was explored. These results show how an improvement in the current estimations in the on/off regions can be obtained.

The quality of the process and the selection of the correct calibration can have an important influence on Schottky barrier device simulations. Important parameters such as the mass and channel length are critical for final device performance and significantly enhances the possibilities for accurate modeling of these devices.

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