Test Interface for Piezoelectric Vibration Energy Harvesters

Bartosz Pękosławski, Patryk Skibiński, and Andrzej Napieralski

***Abstract*—The paper presents microcontroller-based interface for testing of piezoelectric vibration energy harvesters testing and measurement of their parameters. The interface is proposed as a low-cost solution for laboratory stands with electrodynamic shakers. The proposed system contains power processing circuits for piezoelectric harvesters. The microcontroller sets circuit interconnections suitable for a given test, controls circuitry operation, acquires measurement results and presents them to a user. The investigated piezoelectric harvester parameters include optimal load resistance, maximum generated power, resonant frequencies and mechanical damping coefficient. Output power gain can be also examined for AC/DC converter topology with nonlinear voltage processing SSHI circuit.**

***Index Terms*—piezoelectric harvester, vibration energy harvesting, measurement stand, laboratory equipment**

I. INTRODUCTION

VIBRATION Energy Harvesters (VEH) are transducers that convert mechanical vibration energy into electric energy which can be used to power e.g. electronic devices. Generated power levels are usually low due to small ambient vibration amplitudes and limited harvester efficiencies. One of the most promising applications of VEHs is generation of power for Wireless Sensor Network (WSN) nodes. Under constant or periodical excitation by nearby machines or traffic, VEHs can produce enough energy for battery-free low-power nodes [1-3]. The nodes usually stay for most of the time in a sleep mode and are activated only when sufficient energy is stored in their internal supercapacitors to perform data acquisition, processing and radio transmission. However, although widely described in literature for over decade, vibration energy harvesting solutions are not popular in practical implementations.

The main difficulties related to VEHs application are the need for excitation vibration spectrum and time-variation analysis, VEH resonant frequencies tuning, as well as proper selection and design of power processing circuits. Moreover, a VEH maximum size and weight is often very limited and as a result, a careful study and/or modeling of different VEH structures is required. The studies may involve laboratory measurements with vibrations produced by electrodynamic shakers.

There are three main types of VEHs – electromagnetic, electrostatic and piezoelectric ones. The last ones – piezoelectric VEHs (PVEHs) offer relatively high output voltages and can be easily constructed basing on various piezoelectric actuators. Thus, they are the best choice for experiments with VEH structures. PVEHs are usually constructed in the form of a bending beam with a tip mass and one end of the beam clamped [1, 2], as shown in Figure 1, but other structures are also possible [4]. PVEHs can be also simply integrated in MEMS [5-7], which is much more difficult for electromagnetic VEHs (EMVEHs). Both piezoelectric and electromagnetic VEHs are commercially available as off-the-shelf products but they do not offer design flexibility required in many applications. Hence, it is reasonable to choose a custom design approach.

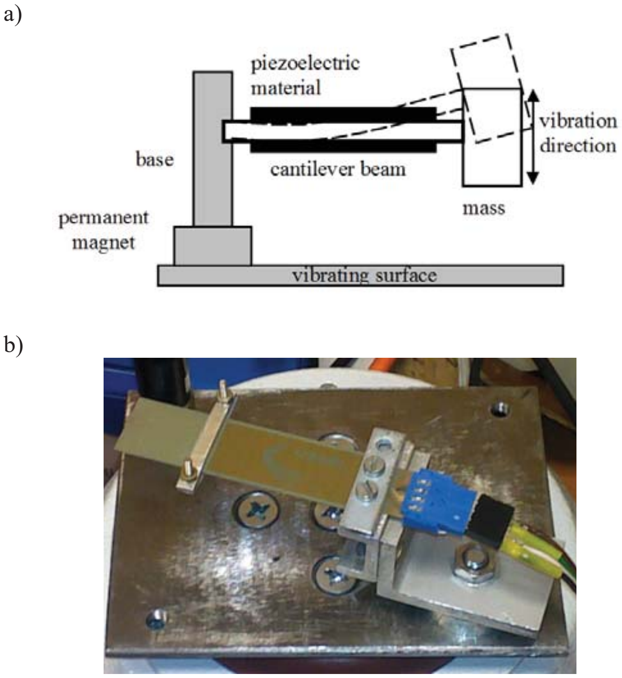

Fig. 1. Piezoelectric Vibration Energy Harvester: example structure (a), actual view (b)

The authors of this paper propose a microcontroller interface device that can facilitate experiments and design of PVEHs. It is an extension of typical laboratory measurement stands with electrodynamic shakers that are frequently used for research [8, 9]. This kind of setup can be an alternative to automated stands based on proprietary test equipment and software [10]. For instance, the automated test stand for VEHs can be based on National Instruments CompactRIO measurement and control equipment. The estimated cost of a configuration including all necessary modules (chassis with controller, AI and AO module, thermocouple, piezoelectric accelerometer, relay and SSR modules) and software is ca. 8000 EUR.

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ISSN 2080-8755

II. LABORATORY MEASUREMENT STAND

A. *Structure*

The measurement stand for which the described microcontroller interface was created consists of:

- electrodynamic shaker (TiraVib S51110, 1.5 m/s maximum velocity, 13 mm maximum peak-peak displacement, frequency range 2 Hz – 7 kHz),
- shaker power amplifier (TiraVib BAA120),
- piezoelectric accelerometer (PCB Piezotronics IMI Sensors 608A11),
- closed-loop vibration amplitude control circuit,
- DDS function generator (GW Instek SFG-2120),
- 2-channel digital oscilloscope (Owon PDS5102),
- precise multimeters (Fluke 8846A, 6.5 digits resolution).

The stand structure and photography is shown in Figure 2. The equipment used in the stand is exemplar and the test interface is intended to operate also with other models. Moreover, oscilloscope and multimeters are additional devices used only for performance verification.

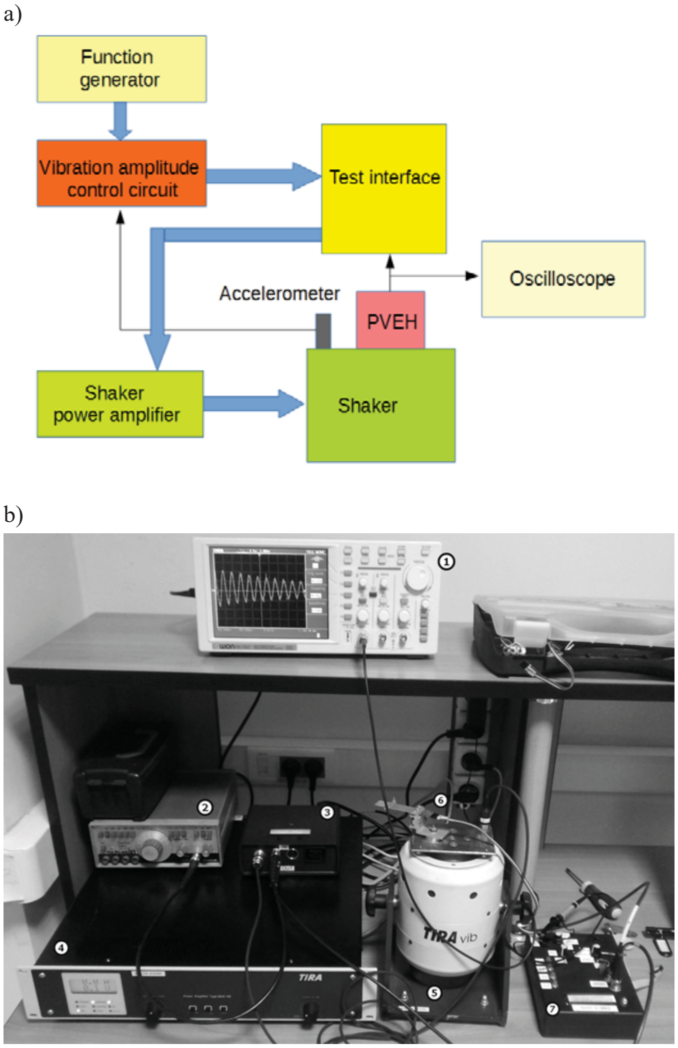

Fig. 2. Laboratory measurement stand: structure (a) and actual view (b)

B. *Closed-loop Vibration Amplitude Control*

Vibration amplitude could be controlled manually by changing the power amplifier amplification or the signal generator settings. However, when new vibration frequency is set or shaker payload weight is varied, vibration amplitude changes. This creates a necessity for vibration amplitude adjustments whenever shaker operation conditions vary. The best solution of this issue is the use of automatic controller of vibration amplitude. The closed-loop control circuit applied in the measurement stand was constructed [11] and its block diagram is presented in Figure 3.

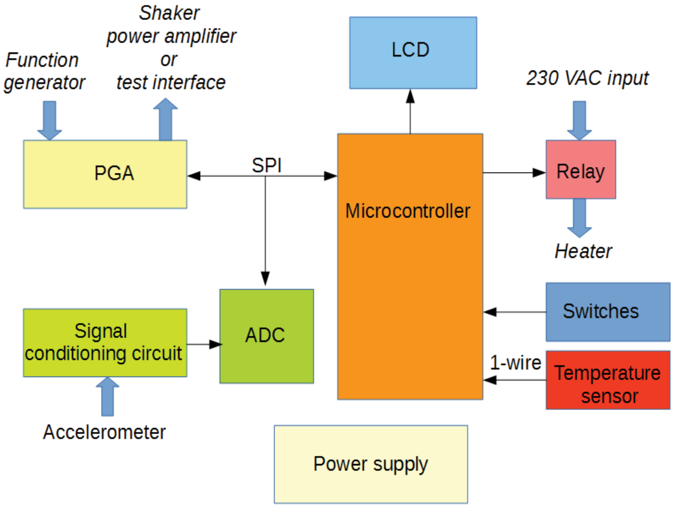

Fig. 3. Block diagram of the vibration amplitude control circuit

The output signal of the controller, which is a signal from external signal generator amplified or attenuated by programmable gain amplifier (PGA) in the controller, can drive the input of the shaker power amplifier.

The controller measures vibration amplitude using the piezoelectric accelerometer. The accelerometer signal is filtered (by low-pass 4-pole Butterworth active filter with cut-off frequency of 7 kHz and bandpass amplification of 2 V/V), DC offset is added (to fit ADC input voltage range) and the signal is converted into digital domain. The 10-bit MCP3001 ADC operating with 200 ksps sampling frequency and 2.5 V external voltage reference is used. The samples are read by ATmega32 microcontroller via SPI and signal amplitude is calculated.

Basing on a comparison of the calculated and preset vibration amplitudes, the microcontroller either increases or decreases amplification factor of the PGA, which is built of AD825ATZ operational amplifier and MCP41010 digital potentiometer (256 taps, 10 kOhm resistance) in feedback loop. As a result, the amplifier gain factor can be adjusted (in a wide range of 3.9 mV/V up to 255 V/V) so that vibration amplitude remains almost constant. In fact, the amplification factor can be varied only in stepwise manner and for input signal amplitudes that are within appropriate voltage range (above PGA input offset and noise level which is equal to about 3 mV, and below maximum input voltage equal to 5 V). The most favorable conditions occur when input voltage amplitude is close to 1 V and this value should be set on the signal generator (the input signal may be AC as the PGA uses symmetrical supply voltage). The power amplifier amplification factor setting should correspond to a desired vibration amplitude range so that the PGA amplification factor can be kept by the controller close to the optimal value of 1 V/V (for higher values the amplified signal may be distorted and for lower ones it can be more noisy).

Moreover, the controller is equipped with digital temperature sensor input and 230 VAC output relay. This enables temperature control for PVEH tests in elevated or low temperatures, depending on whether a heating or cooling component is used in a chamber surrounding a PVEH.

III. PROPOSED TEST INTERFACE

A. Block diagram

The main functional blocks of the proposed test interface are AC/DC converters block, DC/DC converter, microcontroller unit and power supply block. Apart of them, the circuit contains user interface components (LCD, LEDs and switches), digital potentiometer and solid-stare relay (SSR). The block diagram of the test interface circuit is shown in Figure 4.

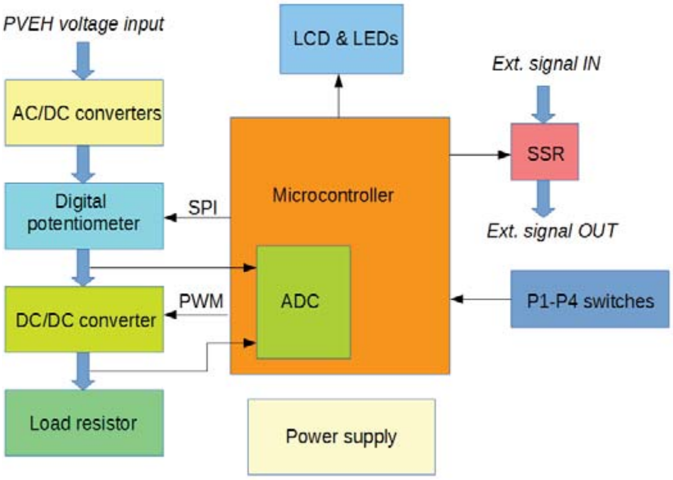

Fig. 4. Block diagram of the test interface circuit

The AC/DC converters block includes three topologies that can be selected by a user:

- diode full bridge rectifier,
- diode voltage doubler,
- diode full bridge rectifier with SSHI (Synchronized Switch Harvesting on Inductor) circuit [12].

In all the AC/DC converters Schottky diodes (BAT43) are used to minimize voltage drops. The self-powered SSHI circuit was chosen instead of a microcontroller-based one with external power supply [13] in order to achieve more realistic generated power measurement results.

The DC/DC converter has a step-down topology with MOSFET switch controlled with a PWM signal generated by the microcontroller (via MOSFET driver).

The microcontroller also controls resistance of the digital potentiometer (MCP41100, 256 taps, 100 kOhm resistance – larger than the one used in the vibration amplitude control circuit) via SPI and the SSR state.

Voltages at the DC/DC converter input and output can be measured with a built-in ADC. Voltage dividers are used in order to obtain suitable voltage range.

Output of the DC/DC converter is connected to 1 kOhm resistor which plays a role of its load.

B. Functions

The interface offers the following functions:

- optimal load resistance measurement,
- maximum generated power measurement,
- mechanical damping coefficient measurement,
- resonant frequencies estimation for open-circuited and short-circuited VEH output.

During the optimal load resistance measurement, the test interface changes resistance of the digital potentiometer from minimum to maximum one. Resistance value at which power is maximum is stored in memory and displayed. DC/DC converter remains in off state (MOSFET is off for all the test).

When maximum generated power is measured, the microcontroller sets the digital potentiometer to shutdown mode (open-circuit) and adjusts PWM duty signal to a value at which the DC/DC converter output voltage (and power) is maximum provided that the voltage is within useful 1.8-3.3 V range (typical supply voltage range of low-power WSN nodes). The calculated output power value is displayed.

During the mechanical damping coefficient measurement, the test interface turns off the SSR (which stops the shaker due to input signal disconnection) and measures two subsequent voltage amplitudes. Basing on their values the mechanical damping is calculated (as a natural logarithm of a ratio of two voltage amplitudes) and displayed. This simplified measurement method is valid when electrical damping can be neglected. Therefore, the digital potentiometer is in shutdown mode and DC/DC converter is off during the test.

When resonant frequencies are measured, the digital potentiometer resistance is set either to minimum value (short-circuit) or to shutdown mode (open-circuit), depending on which resonant frequency is selected by a user. Next, the test interface measures both voltage amplitude and period. When the period is constant (within ±1% range), these values are averaged. When larger period change is encountered, voltage amplitude and frequency are recalculated (after 5 seconds which may be necessary for the vibration amplitude controller to stabilize vibrations). The highest average voltage amplitude value is displayed together with corresponding frequency. A user can change function generator output signal frequency every 5 or more seconds (flashing LED indicates the interface readiness for the frequency change). As a result, power maximum in an investigated frequency band can be found, both for open- and short-circuited output (with zero or maximum electrical damping). Basing on the two resonant frequencies values electromechanical coupling coefficient can be calculated later [14].

C. *Prototype implementation*

The proposed interface was implemented as a prototype version for tests and possible further improvements. It is based on 8-bit ATmega32A microcontroller operating with 16 MHz clock frequency. Figure 5 presents actual view of the device.

Fig. 5. Actual view of the interface circuit prototype

Due to a fact that the internal 10-bit ADC is used with 5 V reference voltage, the ADC voltage resolution is 4.88 mV and sampling frequency is limited to 9.6 kHz. This results in a limit of measured voltage maximum frequency of circa 1 kHz.

FastPWM function of ATmega32 8-bit timer 0 is used for PWM signal generation. The PWM frequency is equal to 62.5 kHz. This switching frequency value was assumed for the DC/DC converter component selection and parameters calculations (especially inductor as well as input and output capacitors).

Timer 1 (16-bit one) is used for long delays generation (2 and 5 seconds).

Timer 2 (8-bit one) is applied for generated voltage period measurements. Since prescaler equal to 128 is set and timer clock frequency is 125 kHz, the timer resolution is 8 µs (which results in sufficient accuracy for 1 kHz input signal frequency) and period is 2.048 ms.

Analog comparator is used for generated voltage zero detection and timer 2 software triggering.

A user can also manually control AC/DC converter load resistance with additional analog potentiometer or external resistor, instead of using the digital potentiometer, which may be a useful feature when the digital potentiometer resistance range is insufficient.

D. *Control program*

The control program for the prototype interface circuit was written in C language. The *main()* function of the program presents user menu, processes user requests and presents measurement results as shown in general flowchart diagram in Figure 6.

According to a function (P1-P4) selected by a user, appropriate measurement procedure starts and is performed (according to function description in B section) until it is finished or until P4 switch is pressed for 2 seconds.

The control program handles interrupts from timers 1 and 2. Global variables incremented in interrupt routines enable generation or measurement of delays exceeding timer count registers lengths.

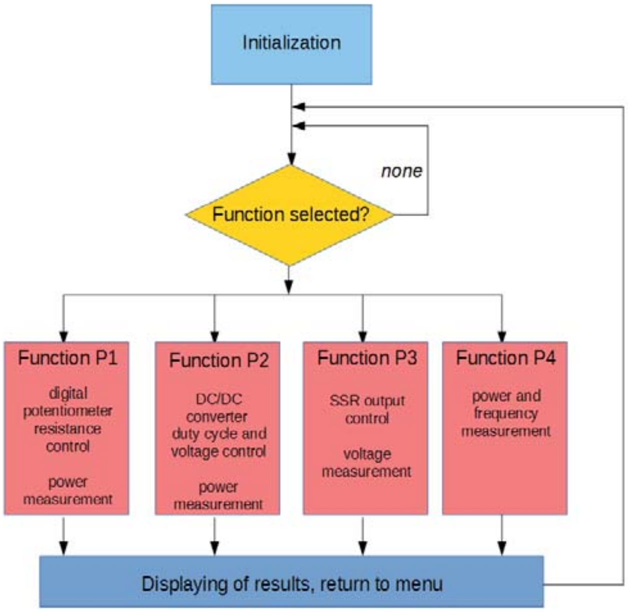

Fig. 6. Control program flowchart diagram

E. *Test results*

The constructed test interface operation was examined on the laboratory measurement stand described in section II, for two PVEHs. Prior to these tests, the vibration amplitude control had been verified using the control circuit without the test interface.

The control circuit tests had revealed that vibration amplitude accuracy (for amplitudes in 5÷10 ms^{-2} range) is ±4% when input signal amplitude, frequency or shaker payload weight are changed. The control circuit stabilizes vibration amplitude in less than 20 seconds after a sudden change of input signal amplitude (by a factor of 10) and in less than 5 seconds after a sudden change of input signal frequency (by a factor of 10) or shaker payload weight (0.5 kg mass placement), as shown in Figure 7.

Table I presents values of parameters for the two PVEHs, measured using the test interface and in a manual way. Differences in values measured that can be observed for both methods result from both vibration amplitude stabilization errors and inaccuracies in measurements performed by the test interface (ADC inaccuracy, digital potentiometer resistance inaccuracy and quantization, timer resolution and analog comparator offset). Estimated worst-case inaccuracies at room temperature are: ±13.81 mV for generated voltage measurement, ±1,4 kOhm for resistance setting and ±1.32 Hz for 100 Hz frequency measurement.

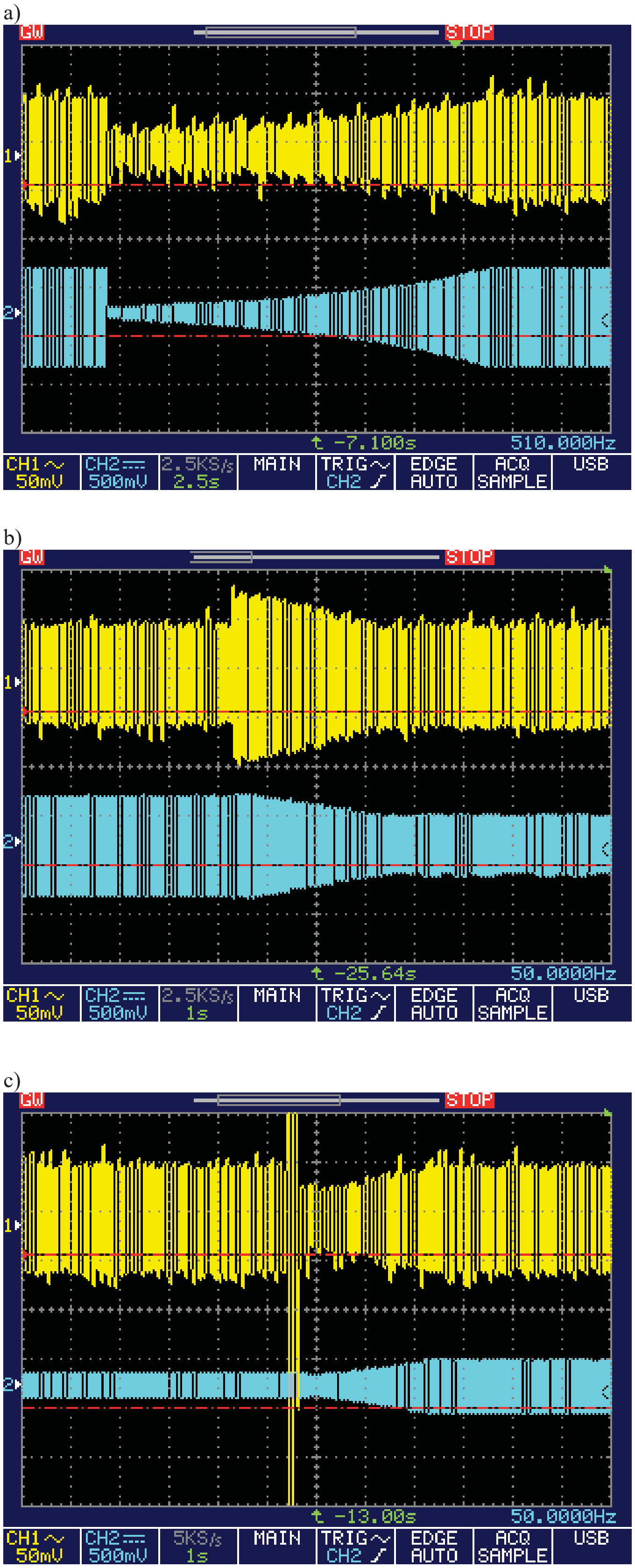

Fig. 7. Vibration amplitude (yellow waveform) and control circuit output signal (cyan waveform) for 10 times input signal change (a), 10 times frequency change (b) and 0.5 kg mass placement (c)

TABLE I
COMPARISON OF PVEH PARAMETERS VALUES

PVEH	Parameter name	Value measured manually	Value measured with test interface
PVEH based on Midè V25WG	Optimal load resistance [kΩ]	10.0	8.3
	Max. generated power [mW]	6.49	6.05
	Mechanical damping c. [Ns/m]	0.022	0.024
	Resonant frequency [Hz]		
	- open load	52.1	52.0
	- short circuit	51.2	51.0
PVEH based on Midè V21BL	Optimal load resistance [kΩ]	30.0	24.0
	Max. generated power [mW]	1.15	1.26
	Mechanical damping c. [Ns/m]	0.012	0.005
	Resonant frequency [Hz]		
	- open load	99.2	100.0
	- short circuit	97.9	98.0

F. *Future improvements*

Possible future improvements of the proposed circuit include automatic change of the function generator output signal frequency. This would make the test circuit operation easier and faster. Since not all function generators are programmable nor have appropriate voltage-controlled frequency input, it would be better to use a DDS generator module (e.g. based on AD9850 IC) in the test interface. Thanks to this solution, there would be no longer a necessity for generated voltage period measurements.

Moreover, ADC with better voltage resolution and higher sampling rate would make generated voltage and power measurements more precise. Therefore, an external, SPI-compatible ADC may be used. Alternatively, the microcontroller may be replaced by a model with fast, 12-bit or more precise ADC.

IV. CONCLUSIONS

In conclusion, the proposed interface can be a useful tool for studies on PVEHs, their development and parameters measurement. Several basic PVEH structure parameters can be easily measured with the use of the interface. These parameters values may be used in PVEH models or they may be compared to model simulation results. The laboratory stand equipped with the test interface can also serve educational purposes e.g. to illustrate differences in operation of various AC/DC converter topologies used for PVEH output power processing.

However, the proposed improvements in the interface circuit seem to be justifiable and they will be introduced in future.

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Andrzej Napieralski received the M.Sc. and Ph.D. degrees from the Lodz University of Technology (LUT) in 1973 and 1977, respectively, and a D.Sc. degree in electronics from the Warsaw University of Technology (Poland) and in microelectronics from the Université de Paul Sabatié (France) in 1989. Sice 1996 he has been the Director of the Department of Microelectronics and Computer Science. Between 2002 and 2008 he held a position of the Vice-President of LUT. He is an author and co-author of over 1100 publications and editor of 25 conference proceedings and 13 scientific journals. He supervised 54 Ph.D. theses; six of them received the price if the Prime Minister of Poland. In 2008 he received the Degree of Honorary Doctoe of the Yaroslav the Wise Novogrod State University (Russia),