BULLETIN OF THE POLISH ACADEMY OF SCIENCES
TECHNICAL SCIENCES, Vol. 61, No. 3, 2013
DOI: 10.2478/bpasts-2013-0073

Rapid prototyping of algorithmic A/D converters based on FPAA devices

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Abstract. A rapid prototyping method for designing mixed signal systems has been presented in the paper. The method is based on implementation of the field programmable analog array (FPAA) to configure and reconfigure mixed signal systems. A serial algorithmic analog digital converter has been used as an example. Three converter architectures have been selected and implemented FPAA device. To verify and illustrate converters operation and prototyping capabilities, implemented converters have been excited by a sinusoidal signal. Analog sinusoidal excitations, digital responses and sinusoidal waveforms after reconstruction are presented.

Key words: rapid prototyping, FPAA, A/D converter.

1. Introduction

Rapid progress in a very large scale integration (VLSI) technology at the break of the 20th and the 21st centuries has made it possible to manufacture mixed (digital and analog) circuits on a single chip. Due to such a progress the design and manufacturing of mixed circuits become very attractive, but expensive and time consuming. Most of the integrated circuit computer-aided design (IC CAD) software are digital-oriented systems incorporating simulation and testability techniques. These tools are not adequate to design the analog part of the IC. So the design of mixed signal systems is difficult and possible design errors may cause the design and manufacturing processes as high cost enterprise. In order to decrease the high cost of IC design and manufacturing process, a rapid prototyping is used to evaluate functionality and performance of novel circuits on hardware at an early design stage. To fully verify new concept of analog circuits we need to design, fabricate and measure prototype circuits. We have a few ways to solve this task: ASIC, programmable DSP, FPGA and lastly FPAA. The ASIC offers the best performance, but is not flexible because ASICs can provide limited parameterization. Moreover the design process is very long and costly. The programmable DSP is the most flexible and the easiest to program, but achieves these advantages at the cost of performance. FPGAs offer an attractive middle ground: the FPGAs offer flexibility and "reprogrammability" like the programmable DSP. Additionally FPGAs have performance that can rival that of the ASIC. Therefore nowadays, field programmable gate array (FPGA) devices are commonly used as fast prototyping digital systems [1–6]. Unfortunately, FPGAs are suitable for digital circuits and cannot be used in analog and mixed systems. The solution in this matter are the FPAA systems, which are reprogrammable while processing analog signals and may be used to face the challenges for overwhelming high cost manufacturing of the mixed signal circuits [7–16]. A limitation of these systems are low frequency and additional noise sources. The advantages of this method are simplicity of design, flexibility and short development time that would justify the use of this method.

This paper describes a rapid development system that was used to speed up implementation and testing of a number of algorithmic analog to digital converters. The system uses a limited set of well-specified analog functional hardware blocks and a fully software reconfigurable processing core based on a powerful FPAA. As an example 6-bit serial algorithmic analog to digital converter has been used to obtain rapid prototype of the specified converter using FPAA [17]. For our work a FPAA device AN221E04 based on switched capacitor technology was used [18]. The basic configurable analog block (CAB) is composed of an operational amplifier (OA) surrounded by capacitor banks, local routing resources, local switching, clocking resources, global connection points and input/output (I/O) pads. Evaluation board used to prototyping proposed converters is shown in Fig. 1.

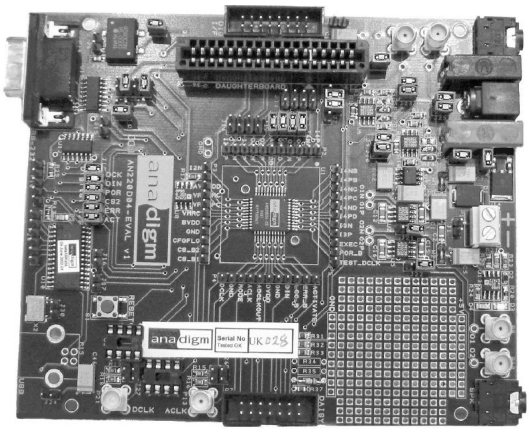

Fig. 1. Anadigm Vortex AN220D04 Evaluation Board whit the AN221E04 device

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2. Analog to digital converter based on iterative algorithm

An iterative, algorithmic analog to digital converter (ADC) performs a conversion shown in Fig. 2 [19]. It repeatedly adjusts the subsequent input voltage V_{INi} and recognizes its sign. The first V_{IN1} is the ADC input voltage V_{IN}. The procedure starts at the first stage ($i = 1$) to perform $N-1$ bit (a_{N-1}), which is the most significant bit (MSB). It is repeated until the desired number of N bits have been obtained. At the end of the procedure a_0 – the least significant bit (LSB) is determined. To perform the conversion in each cycle a sign of the input voltage V_{INi} is determined. If V_{INi} is lower than zero, the digital output a_{N-i} is set to "0", otherwise is set to "1". The V_{INi} voltage is doubled and summed with reference voltage $(-1)^{a_{N-i}}V_{REF}$ (i.e. V_{REF} for $a_{N-i} = 0$ and $-V_{REF}$ for $a_{N-i} = 1$) to perform the next step of conversion. The resulting voltage V_{Ri}, called residue, is then fed back to the input where it becomes the new input voltage V_{INi+1}. The subsequent residue voltages V_{Ri} are expressed as follows

$$V_{Ri} = V_{INi+1} = 2V_{INi} + (-1)^{a_{N-i}}V_{REF} \qquad (1)$$

for $i = 1, 2, \ldots, N-1$.

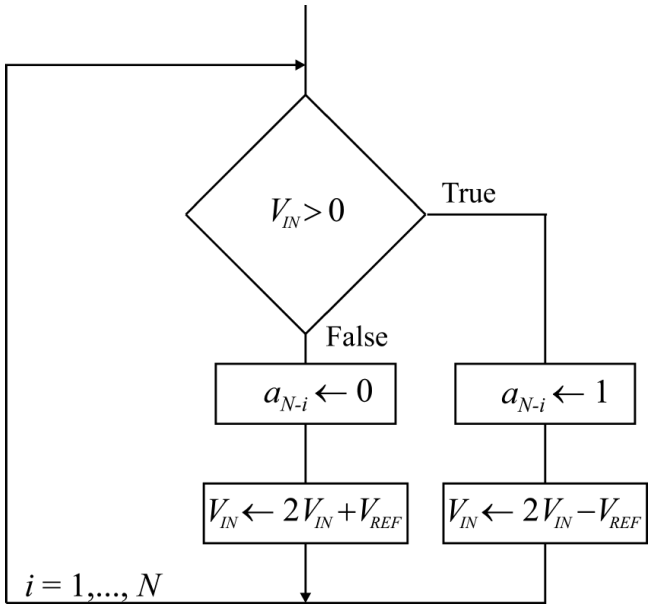

Fig. 2. Flow chart of an iterative algorithmic ADC

The basic circuit for performing a single bit conversion is shown in Fig.·3. It consists of a voltage comparator, a voltage controlled switch, a voltage gain-of-two-amplifier, a voltage summer and a delay cell. The comparator has been used as an one-bit analog to digital subconverter (1-bit ADC) to generate digital signal. It also controls the switch used in an one-bit digital to analog subconverter (1-bit DAC) to generate $-V_{REF}$ or V_{REF} voltage. The delay cell has been used to separate successive samples of the processed signal.

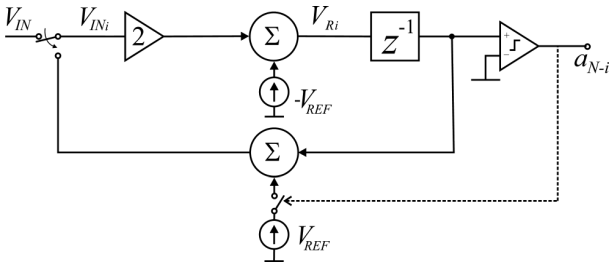

Fig. 3. Structure of an iterative algorithmic ADC

3. Iterative algorithm ADC structure

The block diagram for the iterative ADC performing conversion algorithm of Fig. 2 is shown in Fig. 4. The MSB (a_{N-1}) is generated in the first cycle by the 1-bit ADC. The analog value corresponding to this bit is generated by the 1-bit DAC and is equal $1^{aN-1}V_{REF}$ (i.e. V_{REF} for $a_{N-1} = 0$ and $-V_{REF}$ for $a_{N-1} = 1$). The 1-bit DAC output is summed with the output voltage V_{OUT1}. In the next clock cycle the resulting residue voltage is applied to the input to perform calculation for the next bit. All digital bits are performed in the same circuit in sequence. After the LSB (a_0) is calculated the input of converter is switched to the input analog signal again to perform digital value for the next sample.

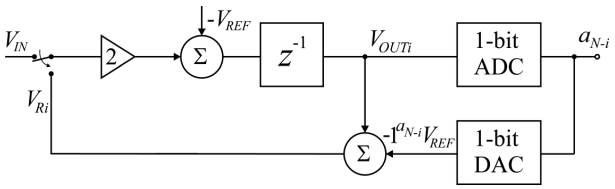

Fig. 4. Block diagram of an ADC based on iterative algorithm

Figure 5 shows a circuit realization of the iterative N-bit ADC using the FPAA AN221E04 device which is performing a conversion algorithm shown in Fig. 2. The structure is composed of a single stage, used N-times repeatedly, to determine N-bits digital signal corresponding to the analog input voltage V_{IN}.

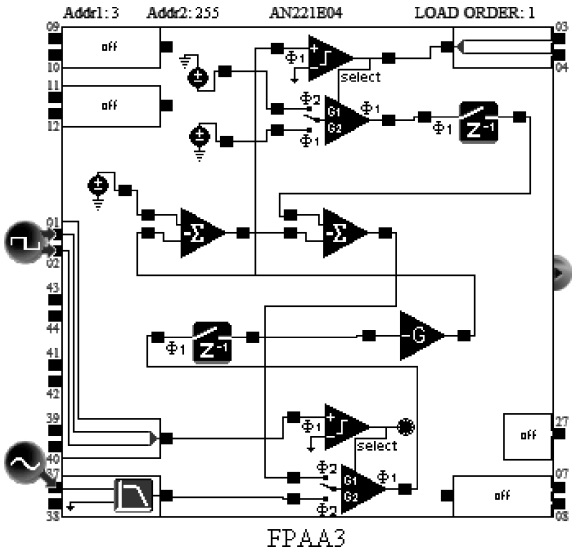

Fig. 5. Circuit realization of N-bit iterative algorithmic ADC

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Digital outputs and sinusoidal waveforms after reconstruction of digital outputs of the iterative algorithmic 6-bit ADC are shown in Figs. 6 and 7, respectively.

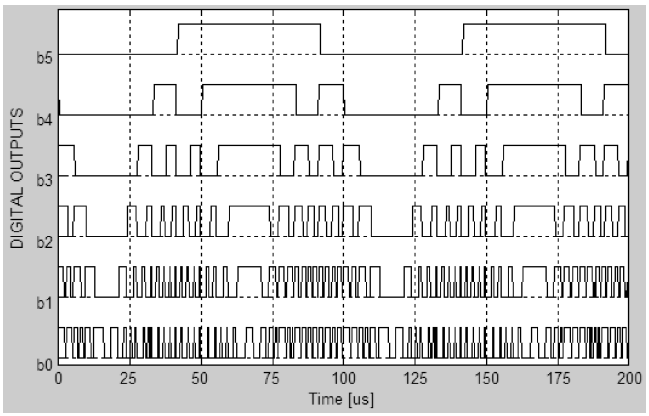

Fig. 6. Digital outputs of the iterative algorithmic 6-bit ADC

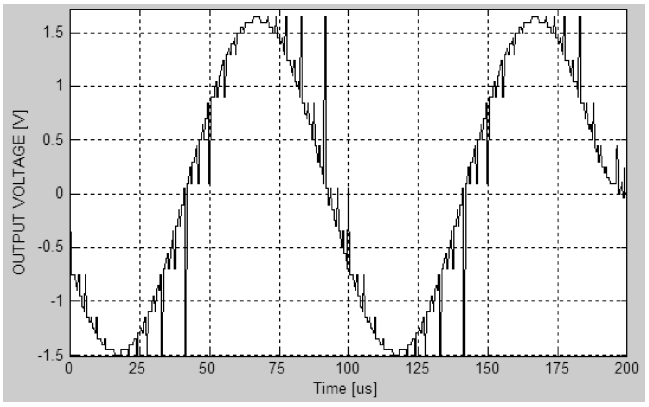

Fig. 7. Sinusoidal waveform after reconstruction digital outputs of the iterative algorithmic 6-bit ADC

4. Serial algorithmic ADC structure

A serial algorithmic ADC performs a conversion shown in Fig. 8. It repeatedly adjusts the subsequent input voltage V_{INi} and recognizes its sign. To perform the conversion in each cycle a sign of the input voltage V_{INi} is determined. If V_{INi} is lower than zero, the digital output a_i is set to "0", otherwise is set to "1". The V_{INi} voltage is doubled and summed with reference voltage $(-1)^{aN-i}V_{REF}$ to perform the next conversion. The resulting voltage V_{Ri} called residue is then passed to the input of the next stage where becomes input voltage V_{INi+1}. The subsequent residue voltages V_{Ri} are expressed by the equation (1). The procedure starts in the first stage $(i = 1)$ to perform $N-1$ bit $(a_{N-1} - MSB)$ and is repeated until the desired number of N bits have been obtained (a_0 – LSB is determined at the end).

Figure 9 shows the block diagram for the serial N-stage converter performing conversion algorithm shown in Fig. 8. The MSB (a_{N-1}) is generated by the first stage 1-bit ADC. The analog value corresponding to this bit is generated by the first stage 1-bit DAC and is equal $(-1)^{aN-1}V_{REF}$ (i.e. V_{REF} for $a_{N-1} = 0$ and $-V_{REF}$ for $a_{N-1} = 1$). The 1-bit DAC output is summed with the output of the gain-of-two amplifier. The resulting residue output voltage V_{R1} is then applied to the next stage. Structure of the first $N-1$ stages is identical. The N-th stage consists of the 1-bit ADC only and is used to perform the LSB (a_0).

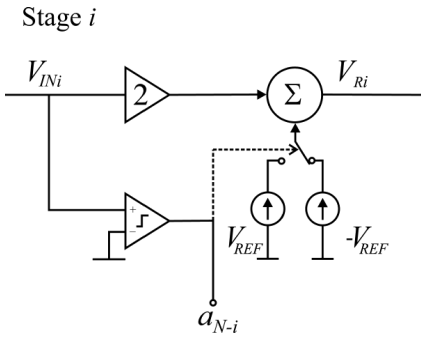

Fig. 8. Structure of i-th stage of the serial ADC

Figure 10 shows a circuit realization of the iterative 6-bit serial algorithmic ADC converter performing conversion algorithm shown in Fig. 8. The structure is composed of six cascaded stages to determine N-bits, a digital signal corresponding to the analog input voltage V_{IN}.

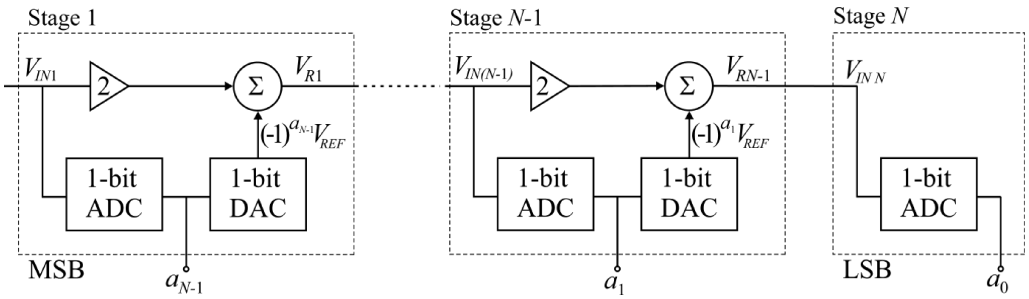

Fig. 9. Block diagram of a serial algorithmic ADC

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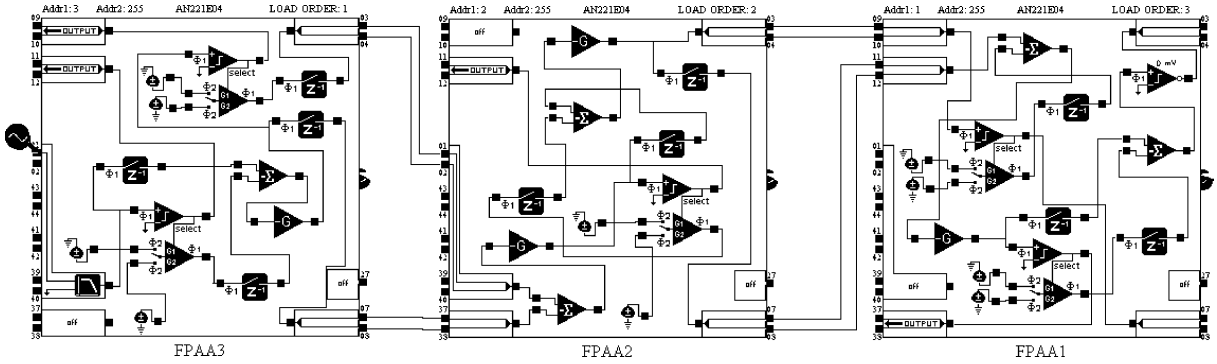

Fig. 10. Circuit realization of a 6-bit serial algorithmic ADC

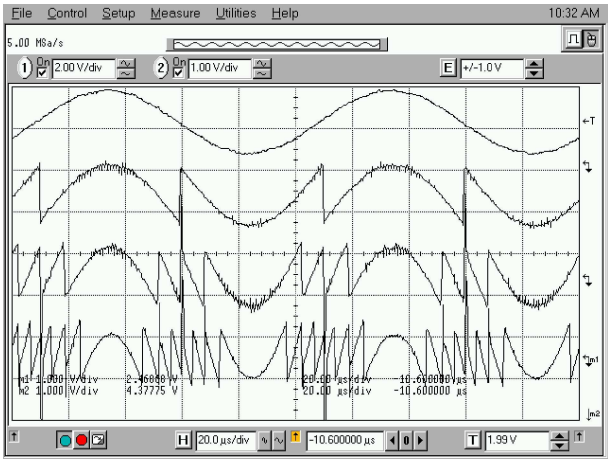

Fig. 11. Residue voltages of the serial algorithmic 6-bit ADC

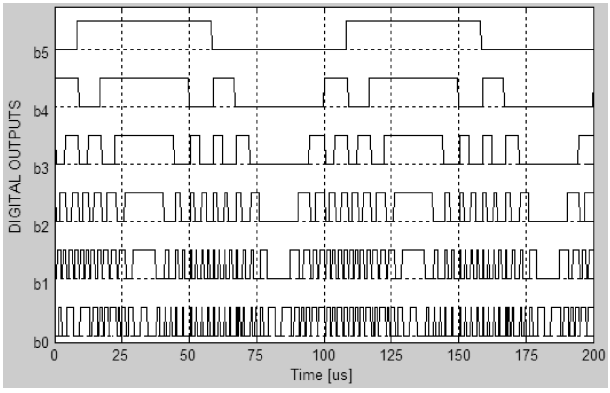

Fig. 12. Digital outputs of the serial algorithmic 6-bit ADC

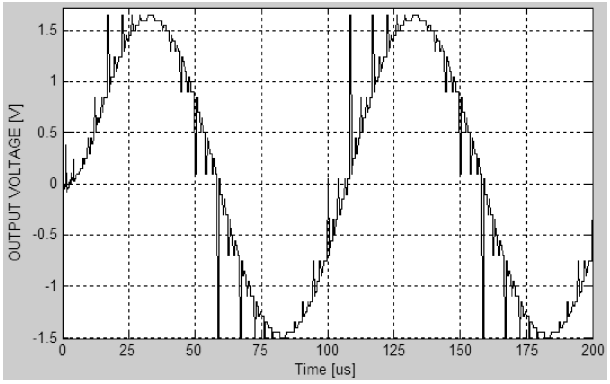

Fig. 13. Sinusoidal waveform after reconstruction digital outputs of the serial algorithmic 6-bit ADC

Residue voltages, digital output signals and their analog reconstructed sinusoidal waveform are shown in Figs. 11, 12 and 13, respectively. The discontinuity problem can be observed in Fig. 13, similarly as in Fig. 7.

5. Serial Gray algorithmic ADC

The binary serial ADC is commonly used to avoid discontinuities in the reconstructed analog sinusoidal waveform of the serial algorithmic converters shown in Figs. 4 and 9. The structure of the i-th stage of the Gray-serial ADC is shown in Fig. 14. The V_{INi} voltage is multiplied by $2(-1)^{aN-i}$ (i.e. $2V_{INi}$ for $a_{N-i}=0$ and $-2V_{INi}$ for $a_{N-i}=1$) and summed with reference voltage V_{REF} to generate the residue signal V_{Ri} that is passed to the next stage to generate the next bit. Now, the subsequent residue voltages are expressed as follows

$$V_{Ri} = V_{INi+1} = 2(-1)^{a_{N-i}} V_{INi} + V_{REF} \qquad (2)$$

for $i = 1, 2, \ldots, N-1$.

The basic i-th stage for performing a single bit conversion is shown in Fig. 14. It consists of a voltage comparator, a voltage controlled switch, a voltage gain-of-two-amplifier and a voltage summer. The comparator has been used as the 1-bit ADC to generate digital signal. It also controls the switch used in the 1-bit DAC to generate $-V_{REF}$ or V_{REF} voltage.

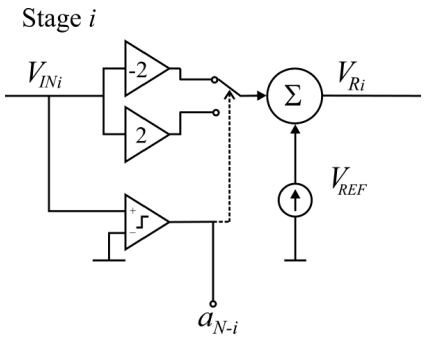

Fig. 14. Structure of i-th stage of the Gray-serial ADC

Figure 15 shows the block diagram for the Gray N-stage ADC performing conversion shown in Fig. 14. A circuit realization of 6-bit Gray ADC is shown in Fig. 16.

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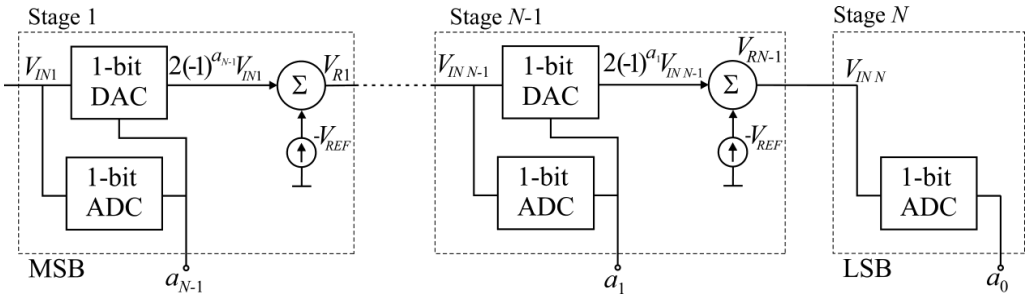

Fig. 15. Block diagram of a Gray algorithmic ADC

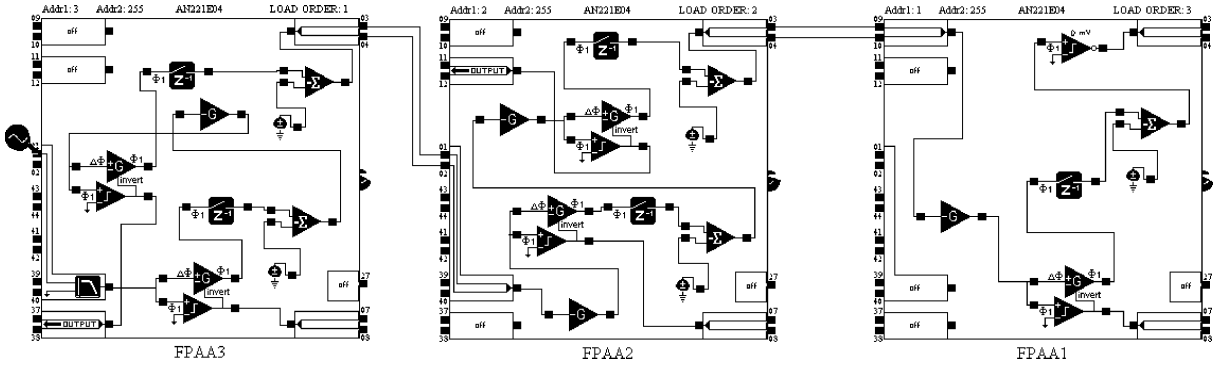

Fig. 16. Circuit realization of a 6-bit Gray algorithmic ADC

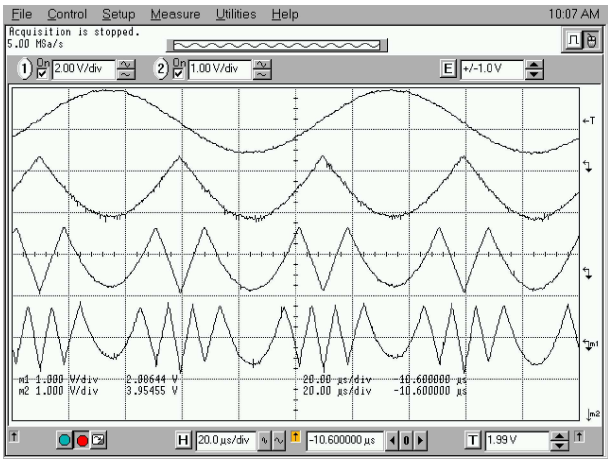

Fig. 17. Residue voltages of the Gray algorithmic 6-bit ADC

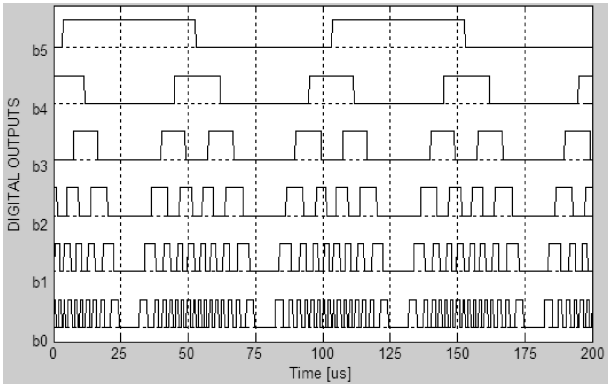

Fig. 18. Digital outputs of the Gray algorithmic 6-bit ADC

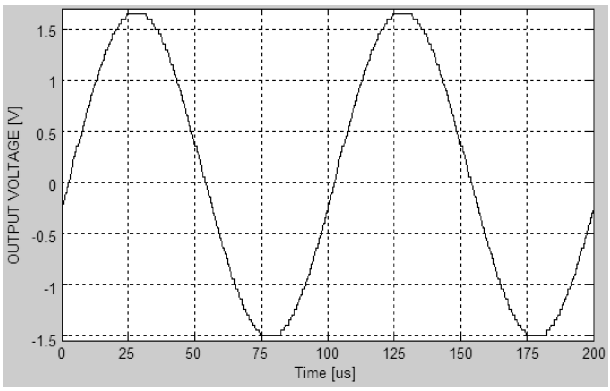

Fig. 19. Sinusoidal waveform after reconstruction digital outputs of the Gray algorithmic 6-bit ADC

A bit-per-stage-architecture based on a scheme shown in Fig. 14 is referred to as the serial-Gray, since the output coding is in the Gray code. The residue output waveforms for a sinusoidal input voltages which range is between $-V_{REF}$ or V_{REF} are shown in Fig. 17. Digital output signals and their analog reconstructed sinusoidal waveform are shown in Figs. 18 and 19, respectively.

6. Concluding remarks

A rapid prototyping method for designing mixed signal systems has been presented in the paper. The method is based on implementation of field programmable analog arrays AN221E04 to configure and reconfigure mixed signal systems. A serial bit-per-bit algorithmic analog to digital converter has been used as an example. The circuit characteristics have been measured and then the structure of the convert-

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er has been reconfigured to satisfy input specifications. The measured output and residue waveforms of the reconfigured converter confirm that FPAA reprogrammable devices such as AN221E04 may be useful for rapid and low cost prototyping of mixed signal systems.

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