

DOI 10.24425/aee.2020.133929

Large-signal input characteristics of selected DC–DC switching converters

Part I. Continuous conduction mode

WŁODZIMIERZ JANKE^{ORCID}, MACIEJ BĄCZEK^{ORCID},
JAROSŁAW KRAŚNIEWSKI^{ORCID}, MARCIN WALCZAK^{ORCID}

Department of Electronics and Computer Science

Koszalin University of Technology

Śniadeckich Street 2, 75-453 Koszalin, Poland

e-mails: {wlodzimierz.janke/maciej.baczek/jaroslaw.krasniewski/marcin.walczak}@tu.koszalin.pl

(Received: 27.04.2020, revised: 30.06.2020)

Abstract: Large-signal input characteristics of three DC–DC converter types: buck, boost and flyback working in the continuous conduction mode (CCM), obtained by simulations and measurements are investigated. The results of investigations are presented in the form of the analytical formulas and the exemplary results of the measurements and two forms of simulations: based on the full description of the converter components and on the averaged models. The parasitic resistances of the converter components are included in the simulations and their influence on the simulation results is discussed.

Key words: boost, buck, CCM, DC–DC converters, flyback, input characteristics

1. Introduction

Switching DC–DC converter modeling may be considered separately in two time scales: for short time segments Δt comparable with the switching period length T_S and for much longer segments containing many switching periods ($\Delta t \gg T_S$). It corresponds to the high or low frequency range. For the converter description in the low frequency range, the averaged models may be used, which neglect the fast changes of the currents and voltages during each switching period. We may also distinguish large-signal description (DC or time-dependent) and averaged small-signal characteristics, usually in the form of a set of transmittances. The first group of the above mentioned characteristics is considered in this series of two papers.



© 2020. The Author(s). This is an open-access article distributed under the terms of the Creative Commons Attribution-NonCommercial-NoDerivatives License (CC BY-NC-ND 4.0, <https://creativecommons.org/licenses/by-nc-nd/4.0/>), which permits use, distribution, and reproduction in any medium, provided that the Article is properly cited, the use is non-commercial, and no modifications or adaptations are made.

The description of the switch mode converters is considered widely in textbooks, as [1], and [2], and many papers, for example [3–10]. Typical description concerns usually the output voltage response to the changes of the input voltage, control signal or the load current. The knowledge of the large-signal input characteristics seems to be necessary in the precise simulation of interdependencies of real power sources and voltage converters or in cascaded connections of converters as in the distributed power systems [11]. It would be useful in particular, in the designing converters to be applied in the power factor correction in rectifying systems and to maximum power point tracking in photovoltaic systems [12–14]. The description of the input characteristics of switching converters is presented in some papers in the context of the input filter design [15–17] where only the small-signal input impedance of a converter is analyzed. The input characteristics are considered in the above papers for the assumed constant output voltage as a consequence of the proper control of the duty ratio (for the closed control loop). In such a situation the input conductance of a converter is negative. On the other hand it seems to be interesting to consider the influence of the duty ratio on the input characteristics of the converter without the control of the output voltage.

The main purpose of these paper series is the description of the large-signal input characteristics of three basic DC–DC converters: buck, boost and flyback, obtained by measurements, numerical simulations and analytical description. The open loop characteristics of converters are investigated. Two operation modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are considered. The results obtained for CCM are presented in the first part of the paper series and for DCM – in the second part. In the description of currents, voltages and a duty ratio of the switching signal, the small letters with capital subscripts denote the instantaneous values and the capital letters with capital subscripts denote DC terms of given quantities. The input and output voltages are denoted by v_G and v_O , respectively, and the load conductance – by G . In some equations, the load resistance $R = 1/G$ is used for convenience. Parasitic resistances of converter components are taken into account in the analysis and simulation. The Spice circuit simulator is used in the majority of simulations.

The schemes of the power stages of the converters are shown in Fig. 1 with the symbols of the real components used (for example, symbol L_F denotes inductor).

The waveforms of currents and voltages in the power stage of switching converters are very complex and the accuracy of their simulations is limited. It is caused mainly by the inaccurate description of converter components. In the popular approximation of a power converter description, the components are treated as ideal switches, inductors and capacitors. The better accuracy may be achieved if the parasitic series resistances is included in models of components but the phenomena in components and PCB are even more complex and the attempts to precise description of components may be found in some sources. The additional source of the inaccuracy of the averaged models is the procedure of averaging. On the other hand the simulation based on the averaged models is much simpler than full-wave simulation.

In Section 2, the time dependencies of the input current in the time segments comparable to the length of the switching period, observed by measurements and large signal PSpice simulations, are presented. The description of the averaged models of buck, boost and flyback converters operating in CCM is given in Section 3 and the DC input characteristics resulting from averaged models – in Section 4. The results of the measurements and calculations of the input characteristics for large time segments are shown in Section 5 in the form of DC characteristics (Section 5.1) and the time

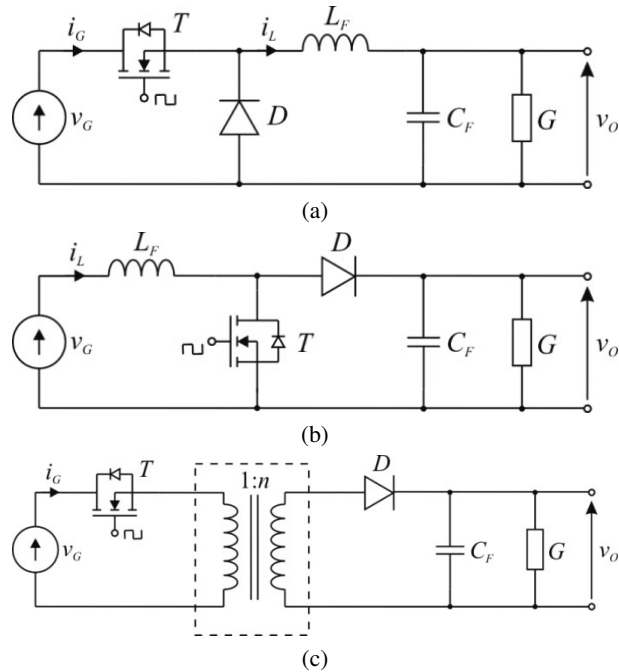


Fig. 1. The power stage schematics of a buck (a), boost (b) and flyback (c) converters

dependencies of the input currents (Section 5.2). A discussion and conclusions are presented in Section 6.

2. The waveforms of the input current of buck, boost and flyback in the short time segments

In the laboratory models of buck and boost converters, a NVD5867NLT4G MOS transistor and MBRS340 diode have been used, whereas in flyback the transistor is HEMT TPH3206 and diode MBRD1035. The parameters of the converters are: in the buck converter, $L = 90.8 \mu\text{H}$, $C = 108.8 \mu\text{F}$; in the boost, $L = 22.6 \mu\text{H}$, $C = 321 \mu\text{F}$; in the flyback, L (magnetizing inductance of transformer) is $150 \mu\text{H}$ and $C = 470 \mu\text{F}$, $n = 0.2$. Switching frequency of the buck is 100 kHz ; in the boost and flyback it is 200 kHz .

The examples of the input current waveforms for the power stage of the buck, boost and flyback converters obtained by measurements and simulations for the short time segments are shown in Fig. 2. The values of the input voltage, load conductance and duty ratio are: for buck, $v_G = 10 \text{ V}$, $G = 0.2 \text{ S}$, $d_A = 0.4$; for boost $v_G = 6 \text{ V}$, $G = 0.2 \text{ S}$, $d_A = 0.3$; for flyback $v_G = 20 \text{ V}$, $G = 1 \text{ S}$, $d_A = 0.5$. The presented results correspond to the steady state of converters, where the waveforms of currents and voltages in a given switching period are identical as the waveforms in the previous period.

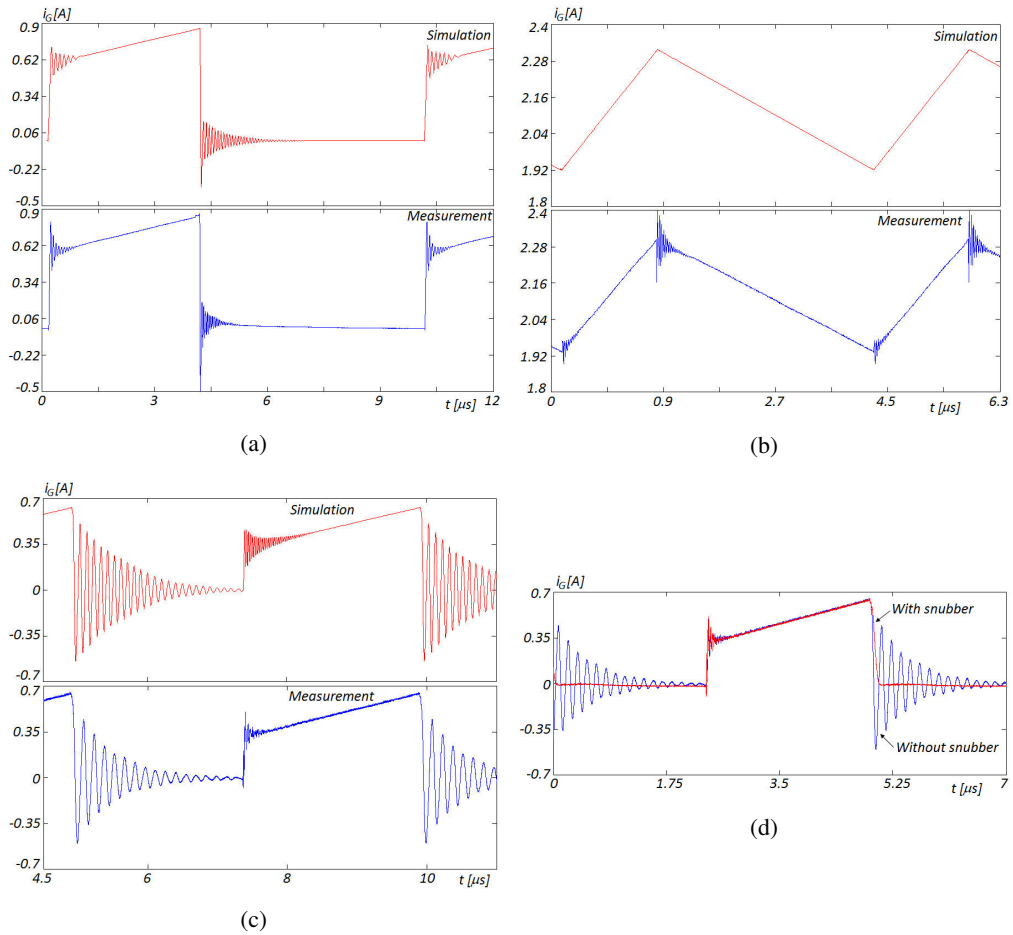


Fig. 2. Input current waveforms of converters obtained by measurements and large signal PSpice simulations: (a) buck; (b) boost; (c) flyback; d) comparison – flyback with and without snubber

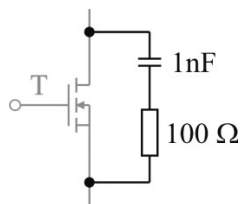


Fig. 3. The diagram of the snubber

The transistors and diodes in the direct large signal PSpice simulations are represented by their models accessible in the PSpice library. The inductors and capacitors in the simulations

are treated as a series connections of the ideal elements L and C with parasitic resistances R_L and R_C . The model of the transformer used in the simulation of flyback is shown in Fig. 4. Parasitic parameters of capacitors, inductors and the transformer, obtained by the independent measurements and used in PSpice simulations (notation in accordance with Figs. 5 and 6) are: R_C for buck, boost and flyback is 18.6 m Ω , 70 m Ω and 76 m Ω , respectively, R_L for buck and boost is 121.6 m Ω and 35 m Ω ; R_{L1} is 0.5 Ω , R_{L2} is 23 m Ω . Leakage inductances of the transformer are: $L_{R1} = 1.53$ μ H; $L_{R2} = 1.0$ nH.

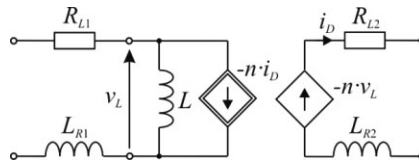


Fig. 4. Model of a transformer used in the large signal PSpice simulations [18]

The input current of the buck and flyback converters changes abruptly during the switching process, and temporary oscillations at switching instants occur. The fast switching and oscillations may be treated as the sources of electromagnetic interference signals (EMI). The relatively high amplitude of the parasitic oscillations in flyback are caused mainly by the resonances of transformer leakage inductances with the output capacitances of the transistor. A similar effect is observed in the buck converter, because of the parasitic inductance of the input path, and the good consistency of the measurements and simulations is achieved after introducing the parasitic input inductance 1 μ H to the model of the converter. These oscillations may be partially suppressed by the use of “snubbers” and the exemplary result of the use of a snubber in a flyback converter is shown in Fig. 2(d). The changes of the boost input current are more soft, because this converter does not contain a switch in the input loop. The measured oscillations in the boost converter are not observed in the large signal PSpice simulations, even after introducing the parasitic inductance in series with the transistor or diode to the model.

3. The large-signal averaged models of non-ideal converters

In the derivation of the large-signal averaged models of converters, the equivalent circuits of converters are used, as shown in Fig. 5. The transistors and diodes are described as switches with series parasitic resistances R_T and R_D respectively. The transformer in the flyback converter is represented by the pair of controlled sources, the magnetizing inductance L and series resistances R_{L1} and R_{L2} . The parasitic resistances of capacitors and inductors are also included in the averaged model derivation whereas other parasitic components such as diode and transistor internal capacitances and transformer leakage inductances are not included because they don't influence the averaged models.

The derivation of the averaged models may be performed in several ways: a) by state-space averaging, b) by the so called circuit averaging (or switch–pair averaging), and c) by the separation of variables. The last approach is used in the derivation of the large-signal averaged models of

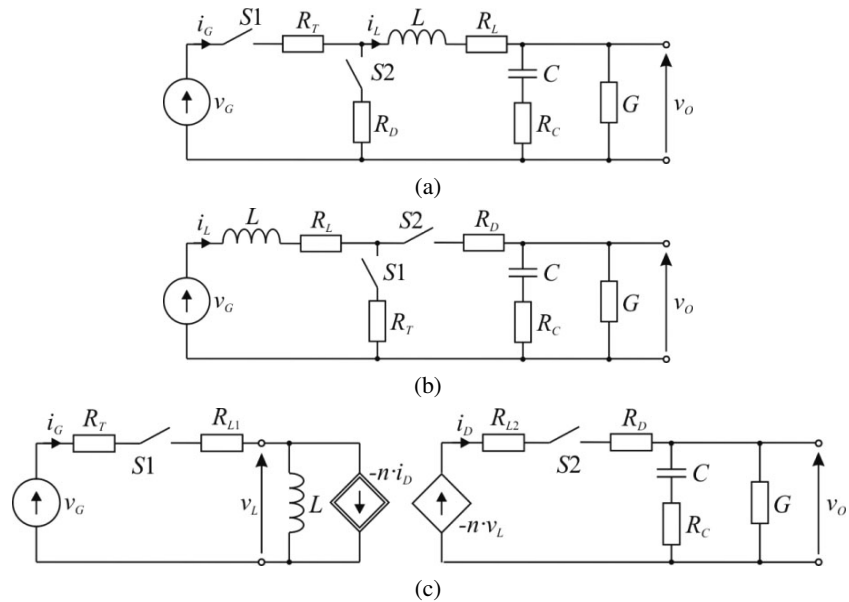


Fig. 5. Equivalent circuits of buck (a), boost (b) and flyback (c) converters used for averaged models derivation

buck, boost and flyback converters in papers [9] and [20]. The results for converters working in CCM are repeated here for convenience in the form shown in Figs. 6, 7, and 8.

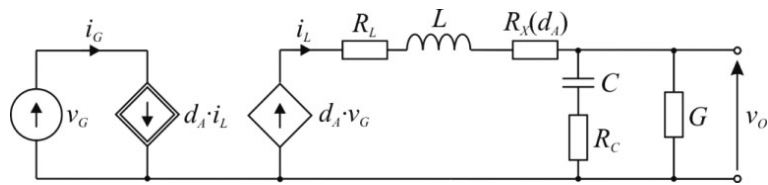


Fig. 6. A large-signal averaged model of a buck converter in CCM [9]

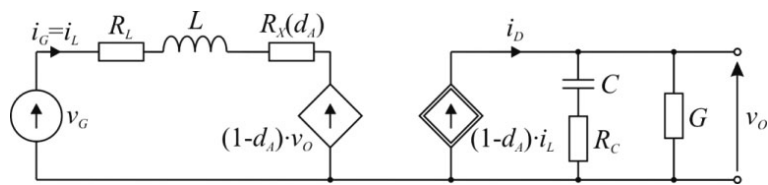


Fig. 7. A large-signal averaged model of a boost converter in CCM [9]

The description of the element R_X in Figs. 6 and 7 is [9]:

$$R_X = d_A \cdot R_T + (1 - d_A) \cdot R_D. \tag{1}$$

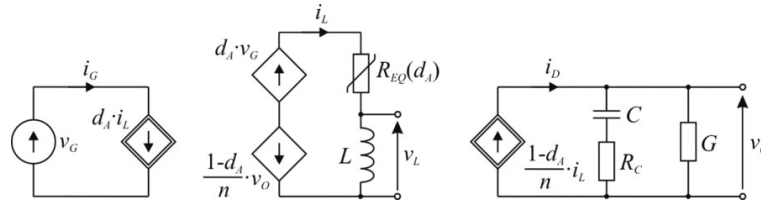


Fig. 8. A large-signal averaged model of a flyback converter in CCM [20]

The description of the element R_{EQ} is [20]:

$$R_{EQ} = d_A \cdot R_{TL} + (1 - d_A) \cdot \frac{R_{DL}}{n^2}, \quad (2)$$

where:

$$R_{TL} = R_T + R_{L1}, \quad (3)$$

$$R_{DL} = R_D + R_{L2}. \quad (4)$$

4. DC input characteristics

DC input characteristics of converters are derived from the DC equivalents of the models from Section 3, (for inductors shorted and capacitors opened) and for CCM are described by:

A) buck

$$I_G(\text{CCM}) = \frac{D_A^2 \cdot V_G}{1 + G \cdot R_Z} \cdot G, \quad (5)$$

B) boost

$$I_G(\text{CCM}) = \frac{G \cdot V_G}{(1 - D_A)^2 + G \cdot R_Z}, \quad (6)$$

where:

$$R_Z = D_A \cdot R_T + (1 - D_A) \cdot R_D + R_L, \quad (7)$$

C) flyback [19]

$$I_G(\text{CCM}) = \frac{G \cdot M_{Vi}^2 \cdot V_G}{1 + G \cdot R_{EQ} \cdot \frac{n^2}{(1 - D_A)^2}}, \quad (8)$$

where:

$$M_{Vi}(\text{CCM}) = \frac{n \cdot D_A}{1 - D_A}. \quad (9)$$

The dependencies of the DC input current on the input voltage are linear. The corresponding input conductances are nearly proportional to the load conductance and the deviation from the proportionality is the result of parasitic resistances.

4.1. Calculations and measurements of the input characteristics for DC or the large time segments

The converter behavior for large time segments $\Delta t \gg T_S$ may be described by the averaged models and calculations based on such models are verified by the full-wave simulations (with the full converter description) and by measurements. The examples of DC input characteristics are presented below in the form of the dependencies of the input conductance on the load conductance. The time-domain input characteristics are presented in the form of the input current response to the step change of the input voltage or duty ratio.

The results described in subsections 5.1 and 5.2 as the precise large signal PSpice simulations are obtained by averaging large-signal PSpice simulations, i.e. all of the samples related to a specific switching period were replaced by an averaged value. The value was calculated by performing a numerical integration (trapezoidal interpolation), over the switching cycle, and dividing it by the length of the switching period. Therefore the simulations may be considered as the results of numerical averaging. The trapezoidal interpolation is required when averaging simulation results because it is not possible to set a constant sample rate in PSpice simulations – the program automatically chooses the simulation step, making it denser in critical moments. Therefore adding the samples and dividing them by the number of samples in one period would give an invalid result. Similar numerical averaging is applied to samples obtained by measurements, except that the sample rate during the measurements was constant (e.g. for the buck converter it was equal to 20 MSPS). In the case of the measurements the trapezoidal interpolation was used because it's a good approximation of a numerical integration.

4.2. DC input characteristics

The measured and simulated dependencies of the DC input current on the input voltage of converters are linear according to the characteristics presented in Section 4, therefore the input conductances G_G may be found. The examples of the dependencies of the input conductance on the load conductance obtained by measurements and simulations are shown in Figs. 9(a), (b) and (c). Two kinds of simulations are presented – based on analytical Formulas (5), (6) and (8) and based on full-wave Spice simulations for steady state. The data presented in Fig. 8 are obtained for $D_A = 0.5$ and the input voltage is equal to: 10 V, 6 V and 20 V for buck, boost and flyback, respectively. The deviation from the linearity, caused by parasitic resistances is best visible in the case of the flyback converter.

4.3. Time-domain input characteristics

The examples of the time-domain input characteristics of the converters, in the form of the input current response to the step change of the input voltage or duty ratio, for time segments containing many switching periods are shown in Figs. 10, 11 and 12 for buck, boost and flyback, respectively. In the figure captions, the step change of a given quantity is described in the exemplary form – $v_G: 8-10$ V, whereas the constant quantity is marked in the figure. Curves 1 in Figs. 10–12 denote results of the detailed, large signal PSpice simulations, curves 2 – simulations based on the averaged models and 3 – measurements.

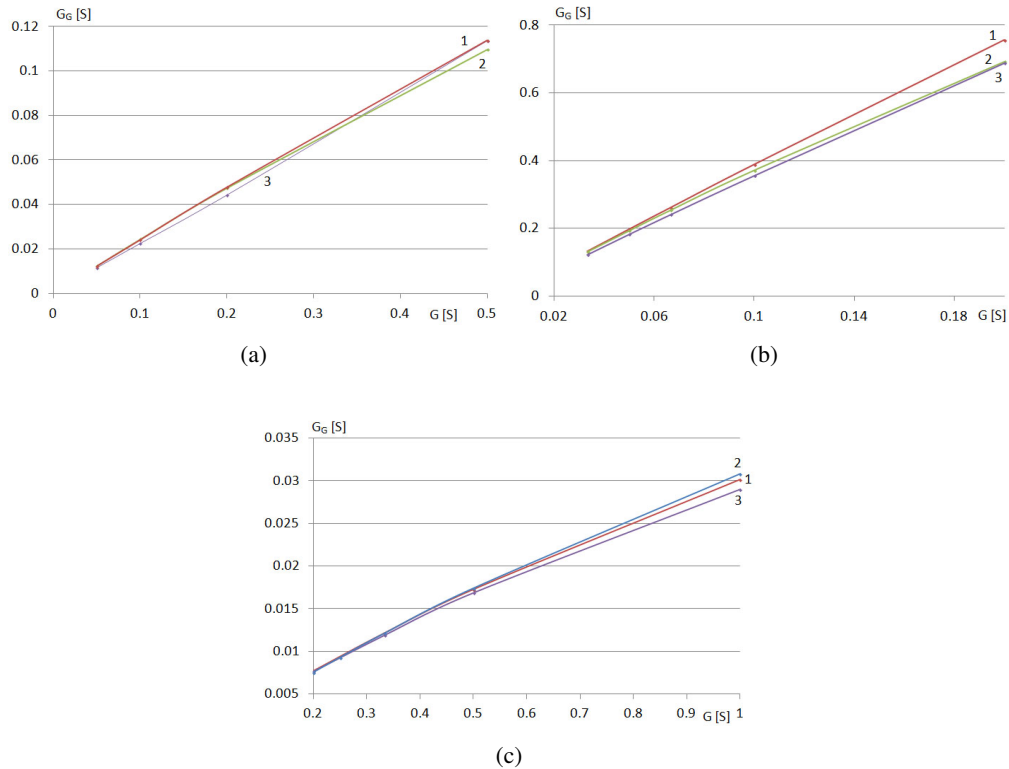


Fig. 9. Dependence of the DC input conductance G_G on the load conductance G of the buck (a), boost (b) and flyback (c) converters. Curve 1 – large signal PSpice simulations, 2 – calculations on Eqs. (5–8), 3 – measurements

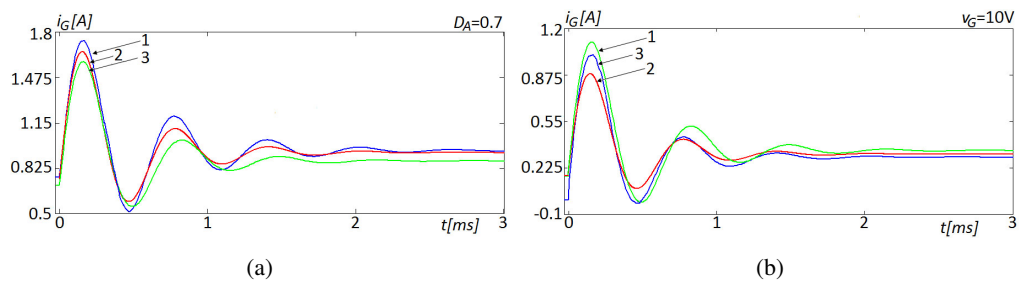


Fig. 10. The input current response in buck, to the step change: (a) v_G : 8 – 10 V; (b) d_A : 0.3 – 0.5

It is observed, that the waveforms of the input current obtained as the response to the step changes of the input voltage or the duty ratio have the form of damped oscillation. For the buck and boost converters it is possible to roughly estimate the frequency of these oscillations as a little

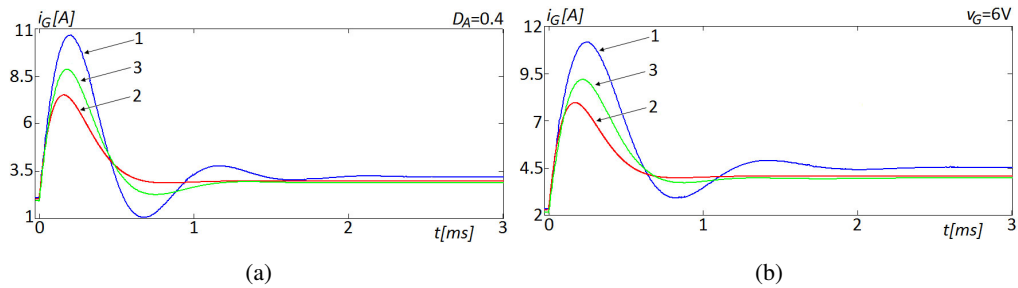


Fig. 11. The input current response in boost, to the step change: (a) v_G : 4 – 6 V; (b) d_A : 0.3 – 0.5

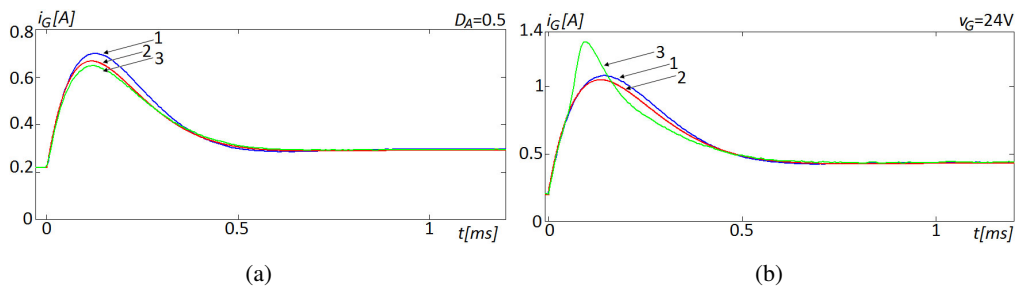


Fig. 12. The input current response in flyback, to the step change: (a) v_G : 18 – 24 V; (b) d_A : 0.45 – 0.55

higher than 1 kHz. It is the value similar to the resonant frequency of the LC circuit composed of inductors and capacitors used actually in these converters. The consistency of waveforms of the input current observed experimentally and obtained by the simulations based on the full large signal PSpice models as well as by the simulations based on the averaged models seems to be quite satisfactory.

Fig. 13 shows the very strong influence of the parasitic resistances of the flyback converter components on the results of calculations based on the averaged model. Calculations taking into account the parasitic resistances are consistent with the measurements and large signal PSpice simulations shown in Fig. 11(a) (note the different scales). It should be pointed out that the simulations based on averaged models are much faster than the precise large signal PSpice simulations. For example for flyback (averaged models 90 ms, full-wave 2132.63 s). On the other hand the simulations based on averaged models give the results of accepted accuracy.

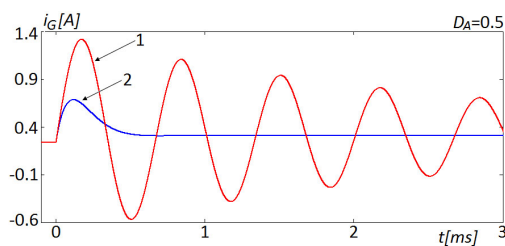


Fig. 13. Simulations of the input current response in flyback, to the input voltage step 18 to 24 V, based on the averaged model: curve 1 – without parasitic resistances; 2 – with parasitic resistances

5. Summary and conclusions

The large-signal input characteristics of the power stage of DC–DC converters: buck, boost and flyback working in continuous conduction mode (CCM) are presented. The characteristics are obtained by simulations and by measurements. In Section 2 – the fast changes of the input current in the time segments comparable with the switching period are shown. The parasitic oscillations at switching moments of different characters in different converters are visible. In the case of the flyback converter the suppression of the oscillations by the snubber is shown. Further results are obtained for large time segments and the measurement results are compared with two kinds of simulations: detailed large signal PSpice simulations and the simulations based on the averaged models. The parasitic resistances of the converter components are taken into account in the simulations. The response of the input current in the time domain to the step change of the input voltage or the duty ratio has the oscillatory form typical to the second order system. The waveform obtained experimentally are consistent with the results of simulations. The influence of the parasitic resistances on the results of simulations are revealed in Fig. 13 where the waveforms of the input current obtained by the simulations performed with and without parasitic resistances are compared. The results of the simulations performed without including the parasitic resistances are completely erroneous.

The input characteristics of converters in DCM are presented in the second part of the paper.

References

- [1] Erickson R.W., Maksimovic D., *Fundamentals of Power Electronics, 2-nd Edition*, Kluwer (2002).
- [2] Kazimierczuk M.K., *Pulse-Width Modulated DC–DC Power Converters*, J. Wiley (2008).
- [3] Middlebrook R.D., Čuk S., *A general unified approach to modeling switching-converter power stages*, Proc. IEEE Power Electronic Specialists Conference, pp. 18–34 (1976).
- [4] Middlebrook R.D., *Small-Signal Modeling of Pulse-Width Modulated Switched-Mode Power Converters*, Proc. IEEE, vol. 76, no. 4, pp. 343–354 (1988).
- [5] Vorperian V., *Simplified Analysis of PWM Converters using Model of PWM Switch, Part I: Continuous Conduction Mode*, IEEE Transactions on Aerospace and Electronic Systems, vol. 26, no. 3, pp. 490–496 (1990).
- [6] Vorperian V., *Simplified analysis of PWM converters using the model of the PWM switch, Part II: Discontinuous Conduction Mode*, IEEE Transactions on Aerospace and Electronic Systems, vol. 26, no. 3, pp. 497–505 (1990).
- [7] Maksimowic D., Stankovic A.M., Thottuvelil V.J., Verghese G.C., *Modeling and Simulation of Power Electronic Converters*, Proc. IEEE, vol. 89, no. 6, pp. 898–912 (2001).
- [8] Janke W., *Averaged Models of Pulse-Modulated DC–DC Converters, Part II. Models Based on the Separation of Variables*, Archives of Electrical Engineering, vol. 61, no. 4, pp. 633–654 (2012).
- [9] Janke W., *Equivalent circuits for averaged description of DC–DC switch-mode power converters based on separation of variables approach*, Bulletin of the Polish Academy of Sciences, vol. 61, no. 3 (2013).
- [10] Suntio T., *On Dynamic Modeling of PCM-Controlled Converters – Buck Converter as an Example*, IEEE Transactions on Power Electronics, vol. 33, no. 6, pp. 5502–5518 (2018).
- [11] Zhang X., *Impedance Control and Stability of DC–DC Converter Systems*, PhD Thesis, University of Sheffield (2016).

- [12] De Gusseme K., Van de Sype D.M., Van den Bossche A.P.M., Melkebeek J.A., *Variable-Duty-Cycle Control to Achieve High Input Power Factor for DCM Boost PFC Converter*, IEEE Transactions on Industrial Electronics, vol. 54, pp. 858–865 (2007).
- [13] Enrique J.M., Duran E., Sidrach-de-Cardona M., Andu´jar J.M., *Theoretical assessment of the maximum power point tracking efficiency of photovoltaic facilities with different converter topologies*, Elsevier Ltd, Solar Energy 81, pp. 31–38 (2007).
- [14] Shu Fan Lim, Khambadkone A.M., *A Simple Digital DCM Control Scheme for Boost PFC Operating in Both CCM and DCM*, IEEE Transactions on Industrial Electronics, vol. 47, pp. 1802–1812 (2011).
- [15] Kazimierzczuk M.K., Cravens R., Reatti A., *Closed-loop input impedance of PWM buck-derived DC–DC converters*, IEEE International Symposium on Circuits and Systems, ISCAS’94, vol. 6, pp. 61–64 (1994).
- [16] Kim D., Son D., Choi B., *Input Impedance Analysis of PWM DC-to-DC Converters*, IEEE 21st APEC, pp. 1339–1346 (2006).
- [17] Pidaparthy S.K., Choi B., *Input Impedances of DC–DC Converters: Unified Analysis and Application Example*, Journal of Power Electronics, vol. 16, no. 6, pp. 2045–2056 (2016).
- [18] Kewei Huang, Jie Li, Ningjun Fan, Yuebirr Li, Xiaolirr Hu, Luo Wu, *Modeling Analysis and Simulation of High-voltage Flyback DC–DC Converter*, IEEE International Symposium on Industrial Electronics, pp. 813–818 (2009).
- [19] Janke W., Bączek M., Kraśniewski J., *Input characteristics of a non-ideal DC–DC flyback converter*, Bulletin of the Polish Academy of Sciences: Technical Sciences, vol. 67, no. 5, pp. 841–849 (2019).
- [20] Janke W., Bączek M., Kraśniewski J., *Large-signal averaged models of the non-ideal flyback converter derived by the separation of variables*, Bulletin of the Polish Academy of Sciences: Technical Sciences, vol. 68, no. 1, pp. 81–88 (2020).