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# GENERATION OF THE REACTIVE CURRENT WITH THE ITERATIVE AGORITHM AID

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**Summary:** The iterative control of the power electronic compensator is presented. The method is based on the voltage measurement. The single phase DC/AC inverter with PWM control is considered. The inverter generates the reactive current shifted to voltage. The current amplitude is computed with the use the iterative algorithm based on Euler secant method. The required voltage amplitude is chosen as the objective function and the limits of the compensator current constitute the constraints. The simulation results for the circuit composed of the simple grid model and DC/AC inverter is presented. The DC/AC inverter with the series inductor realize the current source. The simulation are done with the use PLECS program. Sliding DFT seems to be adequate to compute the correct shift angle between voltage fundamental harmonic and compensator current. The simulation shows that the capacitor voltage connected at the DC side of inverter can be maintained by choosing of the power angle between the grid voltage and inverter voltage.

**Keywords:** reactive current, reactive power compensator, iterative control.

## 1. INTRODUCTION

Power flow studies are important in designing and in determining the best operation of existing systems. Distributed generation brings new challenges in this areas [1]. Electric utility companies use very elaborate programs for Power flow – studies to obtain information concerning the system design and operation. Very advanced arrangements are installed in order to control power flow in a electric grid [2]. It seems that local system weaknesses such as low voltages or over-voltages can be reduced by electronic controlled power compensators. Such arrangements can be controlled by the local node voltage. The proposed analysis and simulation corresponds to non-cooperative control of power compensators. The presented model of the DC/AC inverter contains the capacitor at the dc side as a voltage source. It means that the adequate location of the filter is the load nodes without the power source. The considered compensator is oriented only on the fundamental harmonic, higher harmonics are beyond the scope of this paper. The analysis is narrowed to the single-phase circuit, therefore the results are valid only for balanced three-phase circuits. Fundamental harmonics are recognized by sliding DFT. If harmonic contents in the voltage is small then DFT plays only auxiliary roll, as the main path of the control can be based on the RMS value. Power is not used in the presented algorithm, therefore it is convenient to use complex amplitudes as phasors, instead of RMS values. In the paper the real phasor value represent cosine time function. The complex amplitudes are denoted by capital letters $U$ and $I$ while vertical bars describe amplitudes $|U|$ and $|I|$.

## 2. ITERATIVE ALGORITHM

Let us consider the 2-port model of a single-phase circuit. Assume that considered nodes *ab* belong to the load type with no generator connected. The Thevenin representation of the considered 2-port is shown in Fig. 1.

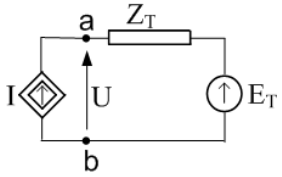


Fig. 1. Thevenin representation of the 2-port

Parameters $Z_T$ and $E_T$ are complex and unknown the system parameters.

$$Z_T = R + jX \tag{1}$$

$$E_T = E_c + jE_b \tag{2}$$

Voltage $U$ is the complex amplitude of the fundamental harmonic of the measured 2-port voltage. $I$ is the searched complex amplitude of the voltage - controlled current source. Current $I$ depends on voltage $U$ as follows

$$I = jbU \tag{3}$$

where $b$ is real number.
Using equations (1)-(3) for circuit in Fig. 1, we obtain

$$|U| = \frac{|E_T|}{\sqrt{(1+bX)^2 + (bR)^2}} \tag{4}$$

Voltage $|U|$ depends on control parameter $b$ and unknown system parameters $R$ and $X$. The voltage controlled current source represent active power filter (compensator) realized as DC/AC inverter. Let desirable voltage

$$|U| = U_d \tag{5}$$

and maximum current of the active filter

$$|I| = I_{\max} \tag{6}$$

The problem can be formulated as optimization problem. Find the $\min(\|U|-U_d|)$ as a function of control parameter $b$ such that $|I| < I_{\max}$.

The problem can be solved by the use of the iterative algorithm similar to Euler secant method. It can also be treated a particular case of Newton – Raphson method.

*Step 0.* Measure voltage $U_0$ for zero compensator current

$$I_0 = 0 \tag{7}$$

*Step 1.* Measure voltage $U_1$ for optional chosen nonzero compensator parameter $b_1$ and compensator current

$$I_1 = jb_1U_0 \tag{8}$$

*Step k.* Measure voltage $U_k$ for

$$b_k = \frac{|U_0|-U_d}{|U_0|-|U_{k-1}|}b_{k-1} \tag{9}$$

and compensator current

$$I_k = jb_kU_{k-1} \tag{10}$$

for each step $k > 0$ constrain $|I_k| < I_{\max}$ should be checked.

*Example.* The computations carried out for the circuit shown in Fig. 2 illustrates the presented algorithm.

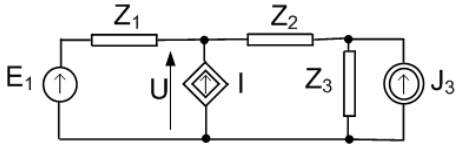


Fig. 2. Circuit with connected compensator

The circuit contains three impedances $Z_1 = (0.300 + j0.314)\Omega$, $Z_2 = (0.0300 + j0.0314)\Omega$, $Z_3 = (10.00 + j3.14)\Omega$, two independent sources $E_1 = (340 + j0.0)V$ or $E_1 = (330 + j0.0)V$, $J_3 = (0.0 + j20.0)A$ and one controlled current source denoting compensator. Compensator current *I* should be computed, while only voltage *U* is measured . It is assumed that the compensator should provide voltage $|U_d| = 325V$ and maximal compensator current is $|I_{max}| = 30A$. The computation results are placed in Table 1.

Table 1. Iteration results, $E = 340V$

| Step | *b* | *I,* A | $\|U\|$, V |
|---|---|---|---|
| 0 | 0.000 | 0.00 | 322.1 |
| 1 | 0.050 | 0.02+16.10i | 317.3 |
| 2 | -0.031 | 0.13-9.72i | 325.0 |

Table 2. Iteration results, $E = 330V$

| Step | *b* | *I,* A | $\|U\|$, V |
|---|---|---|---|
| 0 | 0.000 | 0.00 | 312.4 |
| 1 | 0.050 | 0.01+15.62i | 307.8 |
| 2 | -0.136 | 0.43-30.00i | 321.6 |
| 3 | -0.186 | -0.83-29.99i | 321.3 |

Current *I* placed in the table is computed from voltage complex amplitude *U* according (10). These complex values can be obtained from voltage time varying waveform as the fundamental harmonic. It seems that sliding DFT is adequate tool for this aim. The complex representation of the measured signal is convenient for further processing in order to obtain the signal for DC/IC inverter control. This procedure is described in the next section.

## 3. ACTIVE POWER FILTER

### 3.1. Sliding DFT

The algorithms presented in sections 2 and 4 need algebraic operations to be carried out on voltage amplitudes. Additionally in order to obtain time varying control signal the phases are needed. For these purposes the sliding DFT transformation is useful, even if voltage harmonics can be neglected. The paper concerns the periodical voltages. The windows for discrete Fourier transform should be equal the period. Additionally each window should be synchronized with the proper phase of grid voltage. The proposed iterative algorithm needs the proper time consumption for each iterative step. Hence, the sequenced windows are time delayed, but they have to be placed between the same phases. Phase Locked Loop (PLL) techniques [3] brings a good tool for this aim.

The sliding DFT (SDFT) algorithm performs an *M*-point DFT on time samples $x(m)$ within a sliding window [3]. The *n*th harmonic of *M*-point DFT is defined by

$$X(n) = \sum_{m=0}^{M-1} x(m)e^{-j2\pi mn/M} \tag{11}$$

The frequency–domain index $n$ is an integer in the range $0 \le n \le M-1$.

The principle used for SDFT is known as the DFT shifting theorem. It states that if DFT of windowed (finite-length) time-domain sequence $x(m)$, then the DFT of that sequence, shifted by one, is $X(n)e^{j2\pi n/M}$ . This process is expressed

$$S_n(m) = S_n(m-1)e^{j2\pi n/M} - x(m-M) + x(m) \tag{12}$$

where bin $S_n(m) = x(m)e^{-j2\pi mn/M}$ is the new spectral component seen in (11), $S_n(m-1)$ is the previous spectral component. The subscript *n* reminds, that the spectra are those associated with the *n*th DFT bin. SDFT needs to have unchanging window $M$ within the process. This restriction is important for considered application. If the processed voltage is periodical and the window is equal to the period then $|S_n(m)| = |S_n(m-M)|$ and according to (12) harmonic amplitudes remain unchanged, only phases are shifted by $2\pi n/M$ . This property can be used in order to test if the window is equal to the period. As the paper is concentrated on fundamental harmonics, therefore $n = 1$ and $|S_1(m)| = |S_1(m-M)|$ means that period is unchanged and matches to window.

### 3.2. Voltage source – current source

A shunt compensator operates as a current source controlled by a grid voltage waveform. This current is obtained from DC/AC voltage inverter with the additional series inductor as shown in Fig. 3. The *dc* side of the inverter is connected to capacitor *C* with voltage $U_{dc}$. We assume that capacitor is charged and its voltage

is maintained on a proper level higher than the peak value of the voltage $u_{ac}(t)$ at the *ac* inverter side .

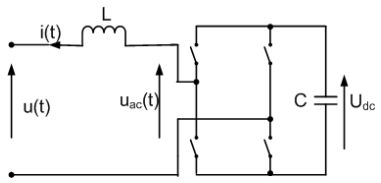


Fig. 3. Current source realization

Inverter should generate the voltage waveform $u_{ac}(t)$. This waveform results from the wanted compensator current obtained from the iterative algorithm. It is seen in Fig. 3, that voltage $u_{ac}(t)$ is equal to the sum of the grid voltage $u(t)$ and the voltage drop on the inductance *L*. This voltage drop follows from the current waveform obtained in the iterative process. As the result the complex value of the voltage fundamental harmonic at the *ac* converter side can be obtained as

$$U_{ac} = U + Z_L I \tag{13}$$

where $Z_L = R_L + jX$ , $X = \omega L$ and $\omega$ fundamental frequency. If simplification $R_L = 0$ is accepted than putting (10) in (13), we obtain

$$U_{ack} = U_{k-1}(1 - \omega L b_k) \tag{14}$$

From complex amplitude $U_{ack}$ the time function signal for DC/AC inverter control within *k*-th operation step can be obtained. The formula (14) contains series inductance $L$. The modified algorithm presented in section 4 enables one to omit inductance $L$.

### 3.3. Simulation results

The influence of the power angle on the capacitor voltage is recognized with the use of the PLECS model of the inverter shown in Fig. 4. The model consists of PWM inverter, dc voltage capacitor , sine wave blocs generating input signals, voltage source representing grid voltage , inductance connecting inverter with grid and additional capacitor reducing current ripple.

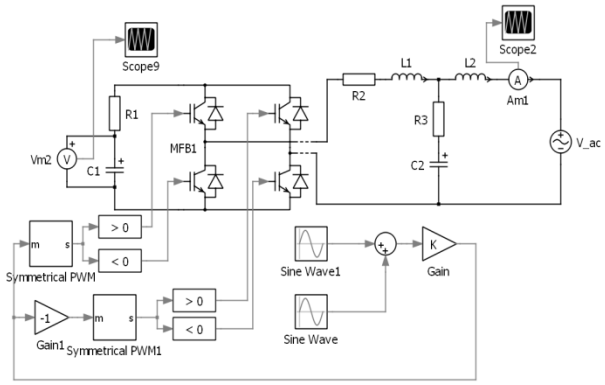


Fig. 4. PLECS model of the PWM inverter

The results presented below are obtained for the following model parameters.

Symmetrical PWM converter : Carrier frequency 5000Hz, Input and output limits [-1 1], Sine Wave: amplitude 634, frequency 314, phase 0.0 or -0.041,

Sine Wave1: not used,

Gain K=1/1014,

*DC* capacitor : $C_1 = 4000\mu F$ , $R_1 = 1\Omega$ .

Series inductor: $L_1 = 95mH$ , $R_2 = 1\Omega$ , $L_2 = 5mH$ .

Ripple filter: $C_2 = 1\mu F$ , $R_3 = 1\Omega$

Fig. 5 shows capacitor voltage (Scope 9) for two values of power angle determined in block Sine Wave. It can be seen that, for $\delta = 0$ the average capacitor voltage decreases, while for negative value $\delta = -0.041$ this voltage is maintained.

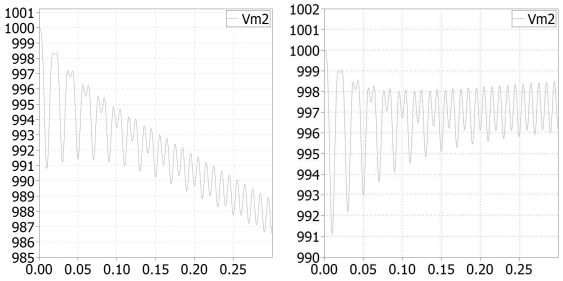


Fig. 5. Capacitor voltage for $\delta = 0$ and $\delta = -0.041$ rad

Fig. 6 shows grid voltage determined by voltage source $V_{ac}$ (left picture) and current (Scope 2) generated by the dc/ac inverter (right picture).

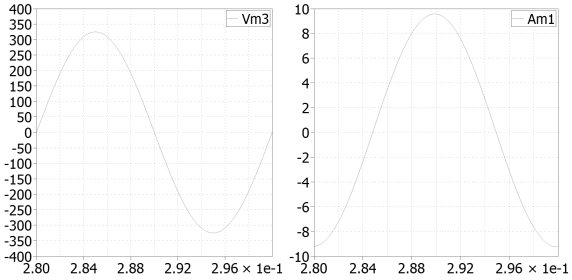


Fig. 6. Grid voltage and compensator current

## 4. VOLTAGE CONTROL FUNCTION

Shunt active filters improve grid voltage parameters by injection the properly chosen current. This current is formed in DC/AC inverter. The structure of such inverter is shown in Fig. 4. *dc* voltage is inverted on *ac* voltage. This voltage source connected in series with inductance forms the proper current. The time varying signal for PWM inverter is computed in the manner described below. For sinusoidal functions the following phasors will be used: grid voltage $U$ , compensator current $I$ , inductor inductance $Z_L$ , *ac* inverter voltage $U_{ac}$ . The *ac* inverter voltage is given (13). As $X >> R_L$, for simplification, we take $Z_L = jX$ .

The iterative algorithm presented in section 2 uses real control parameter *b*. Now, this parameter is changed for new real parameter defined as

$$w = 1 - bX \tag{15}$$

Using (15), equation (14) is substituted for the following relation

$$U_{ac} = wU \tag{16}$$

Parameter *w* can be obtained in the iterative process similar to this presented in section 2. The problem is formulated as

follows: find such $w$ that $\min(|U|-U_d)$ is reached with constrain $|I| < I_{\max}$.

*Step 0.* $w_0 = 1$.

*Step 1.* Optionally chosen $w_1 \neq 1$, such that

$$|I_1| = \frac{w_1 - 1}{X}|U_1| \leq I_{\max} \tag{17}$$

*Step 2.*

$$w_2 = 1 - \frac{|U_0| - U_d}{|U_0| - |U_1|}(1 - w_1) \tag{18}$$

*Step k.*

$$w_k = 1 - \frac{|U_0| - U_d}{|U_0| - |U_{k-1}|}(1 - w_{k-1}) \tag{19}$$

The set $w_k$ for $k = 0,1,2,...,K$ determines the set of voltage phasors

$$U_{ack} = w_k U_{k-1} \tag{20}$$

Obtained parameters $w_k$ are real. Power angle $\delta$ should be introduced in order to maintain the average capacitor voltage

$$U_{pck} = U_{ack} e^{j\delta_k} \tag{21}$$

Power angle $\delta_k$ should be obtained by additional control path from the average value of the capacitor voltage.

From complex amplitude $U_{pck}$, we obtain the time function signal for DC/AC inverter control within *k*-th operation step

$$u_{pk}(t) = \mathrm{Re}(U_{pck} e^{j\omega t}) \tag{22}$$

Angle $\delta_k$ in (21) can be treated as power angle known from power flow theory. It is seen from (21) and (22) , that for $\delta_k = 0$ voltages $U_{pck}$ and $U_{k-1}$ have the same phases, as $w_k$ is real. This conclusion is strict for $R_L = 0$. If voltages $U_{pck}$ and $U_{k-1}$ have the same phases, then no active power can be exchanged between grid to inverter. Only reactive power can be exchanged. In order to send active power from grid to inverter, angle $\delta$ should not be equal to 0. If $\delta < 0$, then positive active power is delivered to the *dc* inverter capacitor, and this capacitor voltage can be maintained. It is shown in the simulation presented in Fig.5. Owing to such active power flow the compensator behave as passive 2-port and does not need the additional energy source.

## 5. CONCLUSIONS

The iterative control needs few steps to reach its target. Each iterative step must be stretched on at least two windows, each a fundamental period long. One window means one measuring unit for DFT operation, even if the sliding DFT is applied each window must be synchronized with the fixed initial phase and have to be exactly one period long. Such requirements lead to the specific kind of control stretched over the necessary time interval. Synchronization can be maintained when phase locked loop is applied [4]. The grid voltage amplitudes observed in the iteration formulae can be substituted for RMS value.

Additional series conductance $L$ should be substantially bigger than grid inductance observed at the considered busses. This inductance should be properly chosen. The economical factors should be taken into account. The iterative algorithm presented in section 4 does not uses the inductance value, the exact knowledge of this value is not necessary.

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# GENEROWANIE PRĄDU BIERNEGO WSPOMAGANE ALGORYTMEM ITERACYJNYM


Przedstawiono koncepcję iteracyjnego sterowania układu wytwarzającego prąd bierny. Metoda opiera się na pomiarze napięcia sieci w węźle przyłączenia kompensatora. Rozpatrywany jest jednofazowy przekształtnik DC/AC ze sterowaniem PWM, realizujący sterowane źródło prądu sinusoidalnego przesuniętego względem pierwszej harmonicznej napięcia sieci. Amplituda wytwarzanego prądu jest obliczana z wykorzystaniem algorytmu iteracyjnego. Funkcją celu w tym algorytmie jest zadana wartość amplitudy podstawowej harmonicznej napięcia sieci. Zmienną poszukiwaną w procesie optymalizacji jest rzeczywisty współczynnik równy stosunkowi amplitudy generowanego sinusoidalnego prądu kompensatora do zmierzonej amplitudy podstawowej harmonicznej napięcia sieci. Pokazano możliwość wytworzenia sygnału sterującego przekształtnik AC/DC w kilku krokach metody iteracyjnej. Metodę tą można zakwalifikować do metod siecznych Eulera. Zaprezentowano wyniki symulacji komputerowych układu złożonego z uproszczonego modelu obwodowego sieci, przekształtnika DC/AC ze sterowaniem PWM oraz szeregowo włączoną cewką indukcyjną. Cewka indukcyjna umożliwia realizację źródła prądu i obliczenie sygnału sterującego przekształtnik. Symulacje wykonano z wykorzystaniem języka programowania PLECS. Pokazano możliwości podtrzymywania napięcia kondensatora włączonego po stronie DC przekształtnika za pomocą kąta mocy między napięciem sieci i napięciem przekształtnika.



**Słowa kluczowe:** prąd bierny, kompensator mocy biernej, sterowanie iteracyjne.