XLVIII Międzyuczelniana Konferencja Metrologów

MKM 2016

Akademia Górniczo-Hutnicza w Krakowie, 5-7 września 2016

HIGH-VOLTAGE DIVIDER WITH AUTOMATIC CALIBRATION - MODEL TESTS

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Abstract: This paper describes structure and method of operation of active high voltage divider with automatic calibration capable of measuring multi-harmonic signals. With the use of this structure identification of varying parameters of the measurement instrument is possible. Measured signal is used for automatic calibrations as the only excitation. To achieve such performance modification of two-sensor method was proposed. Simulation studies on proposed model were conducted that examined influence of Analog to Digital Converters (ADCs) quantization and amplifier parameters, and also ability of self-identification of structure's parameters. Relative errors of divider ratio estimation were calculated for different cases: the structure with an ideal amplifier, the structure with an amplifier with defined parameters and the structure with an amplifier with defined parameters with gain correction procedures.

Keywords: voltage divider, self calibration, two-sensor method, frequency characterization, frequency response.

1. INTRODUCTION

HIGH voltage measurement is very common and important task of electrical engineering. Transformers and capacitive dividers are most frequently used devices for high voltage measurement. Unfortunately, both of them have limited operational bounds. Moreover, they cannot be used in HVDC (High-Voltage Direct Current) systems, as they operate only with alternating current. Another type of high voltage transceivers are resistive dividers. They have a broad frequency band and are capable of converting DC voltage. However, they are expensive, hard to design and prone to environmental conditions like temperature and external electrical fields as it was shown in [1] and [2]. For these reasons their use in power grid is limited. Mentioned papers describe passive resistive dividers, based on Park divider. Another type of dividers are active dividers proposed and described in e. g. [7], [8] and [10]. In this paper we propose an active high voltage divider with automatic calibration procedure. It's operation principles are based on a modified two-sensor method [3] discussed and improved in [4] and [5]. The main idea of the proposal is construction of a low cost divider that is not prone to negative influence of environmental condition, aging of components or undefined load impedance. Described divider can be used, among other applications, in input circuitry of an energy meter or a power quality meter. In such an application it can provide very low uncertainty (at or below 0.1%) together with wide band, while keeping low cost due to lack of high precision components in a circuit.

1.1. The two-sensor method

The two-sensor method also being referred as blind method was proposed in 1936 by H. von Pfriem. The basic version of method was proposed for sensors of inertial character, which can be described by first order differential equation. A system realizing this method is presented in Figure 1.

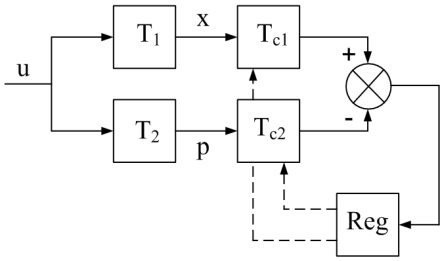

Fig. 1. The two-sensor method of auto-calibration. T_1,T_2 - time constants, u - input signal, p, x - output signals, T_{c1}, T_{c2} - adjustable dynamic parameters, Req - value of criterion used by the regulator.

It consists of 2 sensors characterized by time constants T_1 and T_2, which can simultaneously measure the input signal u. Output signals p and x of these sensors are supplied to inputs of serial correctors with adjustable dynamic parameters T_{c1} and T_{c2}. Based on the difference between output signals of correctors, the value of criterion used by the regulator Reg is brought down to zero by adjusting the dynamic properties of correctors. Once this criterion is fulfilled, the output signals of both correctors reproduce the measured signal reliably. The original method was able to identify dynamic characteristics of transducers only. The novelty of our application is that it allows to identify static characteristics as well. The presented idea of voltage divider allows to find coefficients of its mathematical model during its operation, using measured signal as the only excitation for identification procedures. Our application is also capable of measuring broadband signals.

2. THE STRUCTURE OF THE DIVIDER AND OPERATING PRINCIPLES

The main parameter of every voltage divider is divider ratio k. The value of measured high voltage U_A is calculated by multiplying low voltage U_2 by ratio $k = (Z_3+Z_4)/Z_4$, as it is shown in the right branch in Figure 2a. In standard voltage transducers k is considered as a real constant number. For voltage transformers it is usually only defined for 50Hz, while for resistive dividers a frequency response is given, but precise load impedance is required in order to keep it within declared uncertainty. In this paper k is considered as a complex number, defined separately for each analyzed frequency of measured signal (as a frequency response). It is also assumed that k fluctuates in time, taking into account aforementioned changes of divider parameters. The proposed divider can be used in both AC and DC systems, depending on an implementation. For AC version inductors or capacitors might be used as impedances in conjunction with resistors. In [6] several embodiments of high voltage divider with automatic calibration have been introduced. This paper takes under consideration an active divider, which contains an operational amplifier [7], [8]. Presented device was designed in a way it could adapt the two-sensor method. In this method measuring transducer consists of two parallel branches which measure the same value. The main assumption of the proposed structure is that one branch with Z_3 and Z_4 has constant structure and is used for the continuous measurement. The other branch with Z_1 and Z_2 changes its structure and performs a series of auxiliary measurements. These measurements allow to perform self-identification process of both dynamic and static properties.

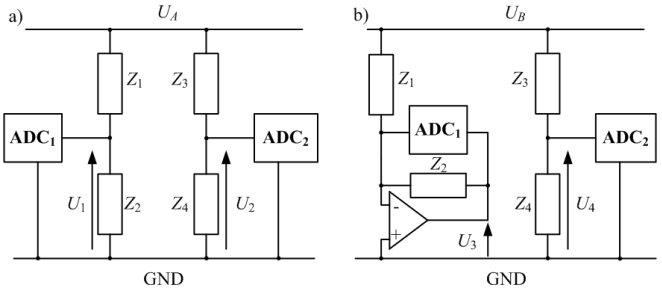

Fig. 2. Two stable configurations of the divider structure. Z_1; Z_2; Z_3; Z_4– impedances, U_1; U_2; U_3; U_4 – measured voltages, ADC_1; ADC_2 – analog to digital converters.

Figure 2 shows the simplified circuit of active adaptive divider in two stable configurations. In order to maintain transparency of the picture we do not show digital control and synchronization system. Constantly repeated operation cycle of adaptive divider is divided into three distinctive steps:

Step 1: Left and right branch of the adaptive divider circuit are made of unknown impedances (Fig.2a) – Z_1 and Z_2 for the left branch and Z_3 and Z_4 for the right branch. Voltages U_1 and U_2 on Z_2 and Z_4 impedances are acquired by ADCs. Parallel connected unknown input impedances of ADCs and impedances of divider itself are considered together as a single object in self-identification process. Voltage U_A is computed based on U_1 and U_2 measurement

$$U_A = \frac{Z_1 + Z_2}{Z_2} U_1 = \frac{Z_3 + Z_4}{Z_4} U_2. \tag{1}$$

Step 2: Left branch of the divider changes its structure (Fig. 2b). Impedances Z_1 and Z_2 along with an amplifier create an active attenuator circuit. Impedance Z_1 is connected in between high voltage and virtual ground. This way the high current is flowing trough impedance Z_1, as well as trough impedance Z_2. Impedance Z_2 has no influence on current flowing through Z_1. Measuring voltage U_3 current flowing trough Z_1 and Z_2 can be estimated. Divider ratio k is estimated as a complex number

$$k = \frac{Z_3 + Z_4}{Z_4} = \frac{U_1}{U_2 + U_1 \dfrac{U_4}{U_3}}. \tag{2}$$

Voltages U_A and U_B are calculated using updated k

$$U_A = kU_2, \tag{3}$$

$$U_B = kU_4, \tag{4}$$

Equation (2) is true only for an ideal operational amplifier. Finite gain of an amplifier forces us to calculate real amplifier's transfer function. The influence of amplifier transfer function is calculated in the correction (third) step.

Step 3: Additional impedance Z_5 is connected to the circuit as it is shown in Figure 3a, afterward like in Figure 3b.

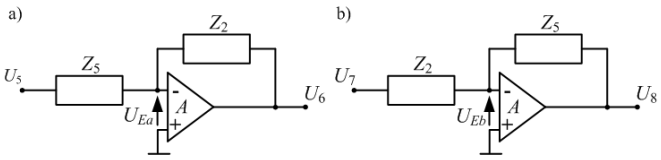

Fig. 3. A structure for estimating amplifier's transfer function influence. A – amplifier gain, U_{Ea}; U_{Eb} – input voltages, Z_5 – additional impedance, U_5; U_6; U_7; U_8 – voltages.

Equations describing the circuit in Figure 3 are given by (5).

$$a)\ \begin{cases} U_{Ea} = \dfrac{-U_6}{A} \\ \dfrac{U_5 - U_{Ea}}{Z_5} = \dfrac{U_{Ea} - U_6}{Z_2} \end{cases} \quad b)\ \begin{cases} U_{Eb} = -\dfrac{U_8}{A} \\ \dfrac{U_7 - U_{Eb}}{Z_2} = \dfrac{U_{Eb} - U_8}{Z_5} \end{cases} \tag{5}$$

Using (5) the gain of amplifier A is calculated

$$A = \frac{U_6 U_7 - 2U_6 U_8 + U_8 U_5}{U_6 U_8 - U_5 U_7}. \tag{6}$$

Evaluation of A is prone to accuracy of voltages $U_5 \div U_8$ measurement like (2) due to bad condition number of the denominator.

Modified divider constant is given by

$$k = \frac{U_1}{U_2\left(1 + \dfrac{1}{A}\right) + U_1 \dfrac{U_4}{U_3}}. \tag{7}$$

3. SIMULATION RESULTS

In order to verify proposed structure of adaptive active divider a number of simulations were performed. All simulations were conducted in Matlab environment. Results are presented for models of various complexity. To examine an accuracy of a divider constant estimation, relative error δ_k (8) was introduced. Amplitude and phase differences in a reference divider constant and an evaluated divider constant, considered as complex numbers, were accounted together with a quality called total vector error (TVE), as for Synchrophasor IEEE Standard C38.118.1 [9].

$$\delta_k = \left| \frac{k - k_{ref}}{k_{ref}} \right| \tag{8}$$

where k_{ref} is a reference divider constant, k is an evaluated constant and $|\cdot|$ stands for modulus. All simulations were conducted for multi-harmonic signal $u_A = U_{max1}\cos(2\pi f_0 t + \phi_{10}) + U_{max5}\cos(2\pi 5 f_0 t + \phi_{50}) + U_{max7}\cos(2\pi 7 f_0 t + \phi_{70})$, where basic frequency f_0 = 50Hz. Maximum voltage values: U_{max1} = 1kV, U_{max5} = 5.5V and U_{max7} = 4.2V were chosen according to results of actual measurements in power system. Phase of harmonic components are: $\phi_{10} = \phi_{50} = \phi_{70} = 0$ rad. Signal was sampled with a frequency of Fs = 50kHz, and the number of samples $N = F\text{s}/f_0$ = 1000. The ADCs' ranges was ±10V.

Impedance Z_1 = 99kΩ, and Z_2= 1kΩ. This is considered as operating point. Z_2 is fluctuated around this operating point with respect to module and phase. k_{ref} is referenced to distorted Z_2. Impedances Z_3 = 99kΩ and Z_4 = 1kΩ are fixed.

3.1. The effect of quantization with ideal amplifier

In configuration for Step 2, for an ideal amplifier k is given by equation (2).

Influence of ADCs resolution of 18 and 24 bits on δ_k was checked. Figure 4 shows estimation errors δ_k for nominal frequency in the case of 24 bit resolution.

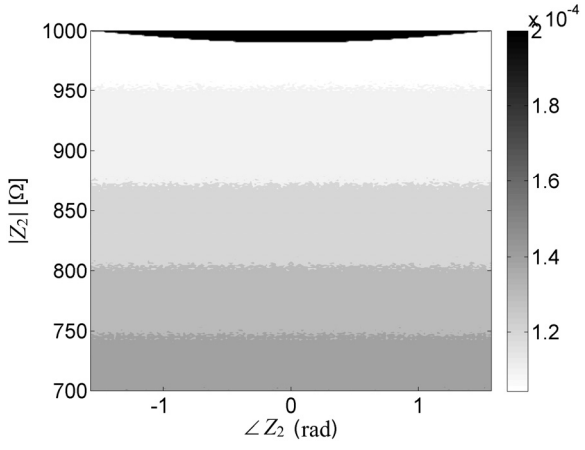

Fig. 4. Estimation error δ_k in the case of 24 bit quantization.

The increase of errors for impedance $|Z_2|$ close to 1000Ω is caused by saturation of ADCs. The change of phase of impedance Z_2 has no influence on estimation. Maximum value of estimation error δ_k for $|Z_2| \in \langle 700;950 \rangle$ and $\angle Z_2 \in \langle -\pi/2;\pi/2 \rangle$ for 18 bit and 24 bit resolution was calculated. Error δ_k for 18 bit resolution equals 1.516e-4 and for 24 bit resolutions equals 2.224e-6. As expected, errors δ_k for 24 bit quantization are smaller than for 18 bit quantization due to a smaller quantization noise.

3.2. The influence of a real amplifier's gain and its correction

Table 1 shows maximum value of estimation error δ_k for each harmonic for $|Z_2| \in \langle 700;950 \rangle$ and $\angle Z_2 \in \langle -\pi/2;\pi/2 \rangle$ for various gains of amplifier modeled as a first order inertial object. Gain values were chosen based on the real operational amplifiers OP07 and OP37 working in closed-loop for cutoff frequency f_c = 1000 Hz. Gains of these amplifiers equals respectively $4\cdot10^5$ and $1.8\cdot10^6$. Calculations for gain 10^8 were also performed to verify how the proposed structure would work with very high, but finite gain.

The results in the first part of Table II called "Without correction" refer to situation described in Step 1 and Step 2. The second part of the Table II called "With correction" refers to situation with additional Step 3.

For nominal frequency for algorithm without correction, for both resolutions, errors decrease with the growth of gain of the amplifier. Divider ratio for higher harmonic is estimated with bigger error than in case of nominal frequency. Use of the amplifier gain correction results in a significant decrease of a divider ratio estimation error for each harmonic. The Table 1 presents the worst case results of several simulation experiments. In authors' opinion, bad numerical condition of the denominator in (2) may cause the misaligned result for the 24-bit resolution and gain $1.8\ 10^6$.

Table 1. Estimation error δ_k for 18 and 24 bit quantization for different gains of amplifier.

Without correction						
Bits	**18**			**24**		
Amp.	$4\cdot10^5$	$1.8\cdot10^6$	10^8	$4\cdot10^5$	$1.8\cdot10^6$	10^8
1st har.	4.9e-4	2.3e-4	1.5e-4	3.8e-4	8.4e-4	3.7e-4
5 th har.	0.086	0.086	0.086	0.002	0.001	0.001
7 th har.	0.070	0.070	0.070	0.002	0.001	0.001
With correction						
Bits	**18**			**24**		
Amp.	$4\cdot10^5$	$1.8\cdot10^6$	10^8	$4\cdot10^5$	$1.8\cdot10^6$	10^8
1st har.	1.5e-4	1.4e-4	1.4e-4	2.4e-6	2.7e-6	2.1e-6
5 th har.	0.079	0.078	0.078	9.5e-4	9.7e-4	9.2e-4
7 th har.	0.072	0.071	0.070	0.001	0.001	9.6e-4

4. CONCLUTIONS

The presented theory and simulation validate the concept of an active high-voltage divider with automatic calibration. The proposed divider has the unique ability of identifying its parameters while being constantly connected to the Grid, which eliminates the necessity of periodic manual calibrations, but considerable modification of legal regulations and standards are required in order to make it possible.

In simulations calculated error δ_k arises mainly due to insufficient resolution of ADCs. For nominal frequency for 18 bit ADC maximum error in examined range equals 1.5e-4 and for 24 bit ADC maximum error drops to 2.4e-6. Such results were achieved due to amplifier gain correction procedures. For higher harmonics maximum errors are several orders higher but still reasonable. Simulation results show that the use of the correction procedure allows to achieve errors of the same order of magnitude as for an ideal

amplifier. This removes a significant obstacle for a hardware implementation. Conducted research encourage us for the further work and development of experimental model of studied structure. Experiments will allow us to verify model studies and propose improvements to the divider structure, being another step towards industrial implementation.

5. REFERENCES

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AKTYWNY DZIELNIK WYSOKIEGO NAPIĘCIA Z AUTOKALIBRACJĄ - BADANIA MODELOWE

Niniejszy artykuł opisuje budowę i zasadę działania aktywnego dzielnika napięciowego z autokalibracją. Układ ten jest w stanie zidentyfikować swoje parametry. Sygnał mierzony jest jedynym potrzebnym w tym celu wymuszeniem. Zasada działania układu bazuje na modyfikacji metody dwuczujnikowej. Przeprowadzone zostały symulacyjne badania modelowe proponowanego układu. Zbadany został wpływ wykorzystywanych w układzie przetworników AC, wpływ kwantyzacji, oraz możliwość autoidentyfikacji parametrów dzielnika. Obliczone zostały błędy względne estymacji przekładni dzielnika (stałej dzielnika) dla różnych przypadków: układu z idealnym wzmacniaczem operacyjnym, układu z wzmacniaczem o zdefiniowanych parametrach i układu ze wzmacniaczem o zdefiniowanych parametrach wraz z zaimplementowaną procedurą identyfikacji jego wzmocnienia i korekcją negatywnego wpływu ograniczonej wartości wzmocnienia.

Słowa kluczowe: dzielnik napięcia, autokalibracja, metoda dwuczujnikowa, charakterystyki częstotliwościowe, odpowiedź częstotliwościowa.