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Using the real-time simulator for prototyping power electronics inverter

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Abstract: This paper deals with real-time (RT) simulators applied in power electronic applications and implemented in a real inverter. The process of preparing and starting up an active rectifier prototype (with an active filter function), using the real-time OPAL RT simulator is given. The control system of the converter and the results of simulation using the Matlab/Simulink suite are discussed.

Key words: numerical simulation, rectifiers, active filters, Real time systems

1. Introduction

The advancements of high computing power digital control systems have made it possible to construct increasingly complex topologies of power electronics systems [1, 2]. The complexity of the control systems for modern topologies have resulted in various advancements made to simulation tools. Computer programs for analyzing systems in limited time windows (e.g. Matlab/Spice) make it possible to become initially acquainted with the principle of operation of a device and allow a regulation system diagram to be prepared [1–5]. The usability of these programs in the process of prototype start-up is limited. Real-time simulators (RTS) are very useful during prototyping [6–10]. Such simulators are equipped with a set of analog and digital outputs and inputs. The analog outputs of the simulator are connected to the measurement channels of a real control system (prototype). The digital outputs controlling e.g. the converter transistors are connected to the digital inputs of the simulator. In such a configuration, the power circuit (converter with passive elements and supply network or motor) is modeled in the simulator. This kind of simulation is called Hardware in the Loop (HIL) [8, 9, 11, 12].

HIL simulations are very useful at the initial stage of developing a prototype of a control system for power electronics converters operating with a power supply network of high short-circuit power. The HIL simulation makes it possible to verify control algorithms in conditions very close to reality with a reduced risk of damage of any elements due to incorrect control implementation. During testing in real conditions (without HIL), algorithmic errors may cause damage of power electronics systems [4, 6, 7, 9, 12]. Moreover, these errors are usually difficult to detect because of the distorted operation of debugging probes and the destruction of the power electronics elements.

An incorrect transistor control sequence causes high and fast-changing current to flow, resulting in interference in the operation of debugging probes or even damage to power electronics elements. The HIL simulation is resistant to these hazards because no high-value currents ever flow in the system, no high voltages appear (no problem with interferences), and there is no risk of damaging any of the converter power circuit elements. Fig. 1 presents successive stages of development of an operating power electronics converter.

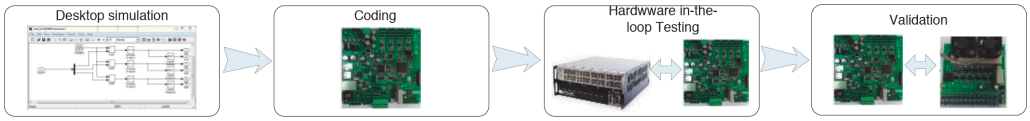


Fig. 1. Stages of work on constructing a power electronics

At the beginning of the control system development, simulations are performed in tools like Spice or Matlab. Simulations [1–5] of this type make it possible to get acquainted with a new topology, to develop a control system, and to check the system performance in dynamic states. After finishing the simulations and getting familiar with the properties of the tested converter, one may proceed to the implementation of the protection and regulation system in the target controller based on a digital chip (DSP/FPGA). Then the correctness of the operation of the prepared controller is verified with the use of a real-time simulator (RTS), which substitutes the real grid and switching elements of the converter (IGBT/MOSFET) together with passive elements. The converter transistors are controlled by the controller on the basis of voltage and current measurements calculated by the RTS. The entire control channel is verified in near-real conditions: A/D converters, a regulation system, modulator. This makes it possible to detect most errors made during coding without placing the system at risk of damage. After completion of the HIL simulations, one may safely proceed to testing the system in real conditions (with a connection to the power supply network).

The paper will present the process of constructing a converter using a real-time simulator OpalRT OP5600 with the example of a three-phase active rectifier.

2. Principle of operation of the rectifier

The control system of the voltage-raising three-phase active rectifier with grid line current shaping is realized in a rotating *dq* frame. In this reference system, sinusoidal signals of the synchronous frequency are represented as constant values, which enables the use of well-known

PI controllers. Fig. 2 presents a diagram of connection of the rectifier to the grid. Because L ≫ R, the diagram omits the resistance of the chokes and the power supply network.

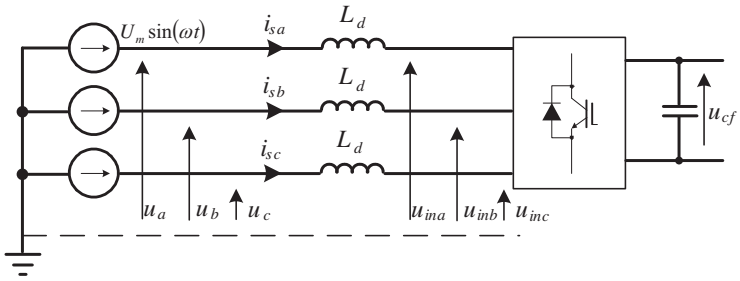


Fig. 2. Diagram of connection of the rectifier to the power supply network

The following designations have been adopted in Fig. 2: i_{sn} represents the phase currents, u_n is the phase voltage of grid, u_{inn} is the converter input voltage (where $n = a, b, c$). The phase currents, in accordance with Fig. 2, are described by the equation:

$$u_n - u_{inn} = L\frac{\mathrm{d}\, i_{sn}}{\mathrm{d}t}\,. \tag{1}$$

After transformation (1) to the rotating dq frame, the following equation is obtained:

$$\overline{u}_{sdq} - \overline{u}_{indq} = \Delta\overline{u}_{dq} = L_d\frac{\mathrm{d}\,\bar{i}_{sdq}}{\mathrm{d}t} + j\omega L_d\bar{i}_{sdq}\,. \tag{2}$$

By decomposing (2) into components d and q, the following is obtained:

$$u_{ind} = u_{sd} - \Delta u_d = u_{sd} - \left(L_d\frac{\mathrm{d}\, i_{sd}}{\mathrm{d}t} - \omega L_d i_{sq}\right), \tag{3}$$

$$u_{inq} = u_{sq} - \Delta u_q = u_{sq} - \left(L_d\frac{\mathrm{d}\, i_{sq}}{\mathrm{d}t} - \omega L_d i_{sd}\right). \tag{4}$$

Equations (4) and (5) describe the waveforms of the input voltages of the converter. By substituting the demanded line current values in the equations, it is possible to determine the voltage waveforms forcing the flow of the required current. The components $L_d(\mathrm{d}\, i_{sdq}/\mathrm{d}t)$ represent the dynamic states of the converter. By assuming that there are only proportional elements in the regulation system, the following relationships are obtained on the basis of equations (4) and (5):

$$u_{ind} = u_{sd} - (K_R\Delta i_{sd} - K_d\Delta i_{sq}) = u_{sd} - [K_R(i_{sdr} - i_{sd}) - K_d(i_{sqr} - i_{sq})], \tag{5}$$

$$u_{inq} = u_{sq} - (K_R\Delta i_{sq} - Kq\Delta i_{dq}) = u_{sq} - [K_R(i_{sqr} - i_{sq}) - K_q(i_{sdr} - i_{sd})]. \tag{6}$$

3. Rectifier simulation in Matlab/Simulink software principle of operation of the rectifier

Fig. 3 presents a block diagram of the regulation system together with the power circuit. The following designations have been adopted in this figure: *TP* represents elements, which delay the switch (dead time), *PI* is the proportional-integral regulator, *KS* is the sign comparator, *SI* is the current separator, *SU* is the voltage separator, *SAW* is the symmetrical triangular waveform generator, *Kr*, *Kd*, *Kq* are the proportional elements, *ST* represents contactors, *Rr* is the resistor, limiting the loading current of the capacitor *CF*, Σ is the adder.

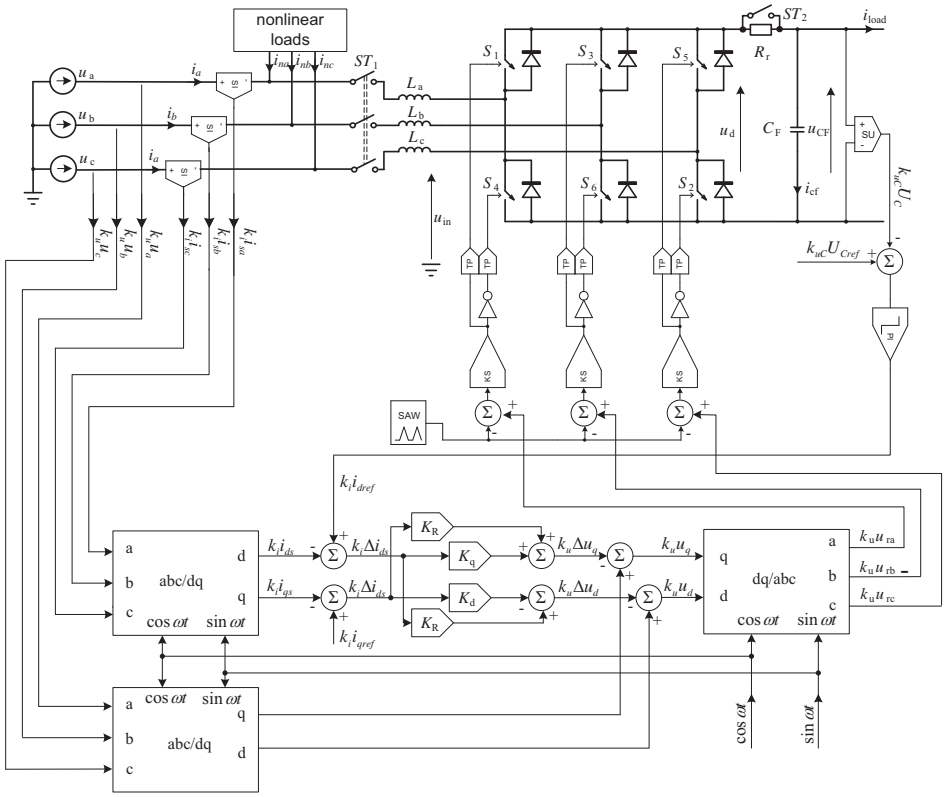


Fig. 3. Block diagram of the regulation system together with the power circuit

The reference signals of the set currents $k_i i_{dref}$ (active current) and $k_i i_{qref}$ (reactive current) have been marked in Fig. 3. The reference value of the active current is determined by the voltage regulator on the basis of the error between the demanded voltage on the capacitor (CF) and the actual value of this voltage. The reactive current may be set by the master control system in order to perform the function of a reactive power compensator for the primary harmonic. In the case when there is no need to introduce reactive power into the grid, the reference value $k_i i_{qref}$ is set to zero.

Since the control system aims to keep the sinusoidal current waveforms in the grid in phase with the voltage, it can also be used as an active filter (when the reactive power compensation is not being performed). In such a case a nonlinear receiver is connected between the current separators (SI) and the mains chokes (L_a, L_b, L_c).

The correctness of the control concept (Fig. 3), the dynamic states of operation of the converter (step switching on the load in the DC circuit), and the ability of the system to perform the function of an active filter have been verified in the simulation (Matlab/Simulink software).

In the simulation it has been assumed that the system is being supplied from a three-phase network of line-to-line voltage equal to 127 V, the maximum converter current is equal to 15 A, and the set voltage of capacitor is equal to 420 V. Fig. 4 presents the waveforms of currents and voltages characterizing the operation of the rectifier.

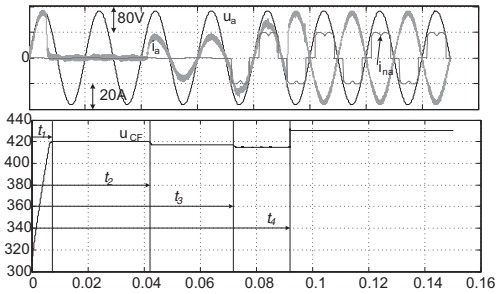


Fig. 4. Waveforms of power supply line phase voltage (u_a), power supply line current (i_a), nonlinear receiver current (i_{na}), and DC link voltage (u_{CF}). Results of simulation in Matlab/Simulink software; t_1 – charging capacitor CF, t_2 – idle state, t_3 – load connected to DC-link, t_4 – load connected to DC-link and nonlinear load working, t_5 – nonlinear load working and transferring energy from DC-link to the grid

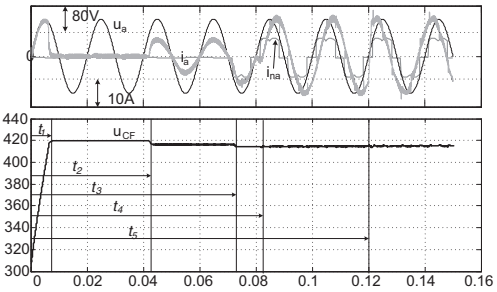


Fig. 5. Oscilloscope traces depicting the possibility of introducing reactive power into the power supply line by the converter t_1 – charging capacitor CF, t_2 – idle state, t_3 – load connected to DC-link, t_4 – load connected to DC-link, nonlinear load working and generating the inductive reactive power, t_5 – load connected to DC-link, nonlinear load working and generating the capacitive reactive power

Fig. 4 presents the waveforms of grid phase voltage (u_a), grid current (i_a), nonlinear receiver currents (i_{na}), and DC- link voltage (u_{CF}). Four characteristic spans of the system operation have also been marked: t_1: capacitor charging from the value equal to the line-to-line voltage amplitude to the set voltage (420 V), t_2: after this time the DC receiver connected to the capacitor is switched on, t_3: the nonlinear receiver is switched on (in this case, a three-phase diode rectifier with resistive load), t_4: the capacitor voltage rises above the set voltage. Fig. 4 does not show the initial charging of the capacitor from the voltage equal to zero to the amplitude of the grid voltage, because charging is then performed by the diode rectifier (the antiparallel diodes of the bridge transistors). Switching of the transistors does not affect the shape of the power supply line current at that time, the value of the current at that time is limited by the resistor (R_r). In the time span t_1 the current is already sinusoidal and in phase with the voltage, the value of the current is limited by the limit (15 A) set by the voltage regulator (of PI structure). After the capacitor is charged to the set level, the line current decreases to the value resulting from the leakage of

the capacitor and the power losses of the converter. After the time t_2 the receiver is connected to the capacitor (in the case of the simulation it is a 75 Ω resistor). After the resistor is connected, the power supply line current is sinusoidal and in phase with the voltage, the capacitor voltage decreases by approx. 1.5 V. This results from the adopted structure of the regulation system. After the time t_3 the nonlinear receiver is switched on (the DC receiver connected to the capacitor remains switched on). After switching on the nonlinear receiver, the capacitor voltage decreases by approx. 2.5 V. This change is small, it does not exceed 0.6% of the set voltage. Despite the appearance of nonlinear currents, the system has maintained the sinusoidal currents in the power supply line in phase with the voltage. In the last analyzed time-span the capacitor voltage has increased above the set value (a braking motor, another energy source, e.g. PV, etc.). This results in the sign of the regulator voltage error being changed to negative, and as a consequence, the energy from the capacitor starts to be transferred to the power supply line. As follows from the presented analysis, the system described has been operating correctly in all cases and has fulfilled the function of a rectifier and an active filter, making it possible to transfer the energy from the capacitor to the grid (four-quadrant operation).

If the nonlinear receiver introduces reactive power into the grid line, the converter will compensate for it. In the presented example (Fig. 3), the nonlinear receiver is the three-phase diode rectifier loaded with the resistor. This type of nonlinear receiver used in the example is loading the mains with reactive power. As it results from the waveforms in Fig. 4, after switching on the diode rectifier the grid current remains sinusoidal and in phase with the voltage, i.e. the analyzed converter has correctly compensated the reactive power. The described system can fulfil an additional function of introducing additional reactive power into the grid. This is performed on demand of the master control system. Simulation traces depicting such operation are presented in Fig. 5. The same functions as presented in Fig. 4 are realized in the time spans t_1, t_2, t_3. After the time t_4 the converter introduces inductive reactive power into the mains. In the last period from the time t_5 capacitive reactive power is being introduced into the grid. Generating the additional reactive power by the converter does not disturb other functions of the system, i.e. stabilizing the capacitor voltage and filtering the higher harmonics introduced by the nonlinear receiver.

4. Coding of the control system

A system for controlling a real active rectifier, based on an FPGA chip, has been prepared on the basis of the diagram given in Fig. 3 and the simulation performed in Matlab/Simulink software. A picture of the controller is presented in Fig. 6. Presented rectifier is part of the high speed flywheel energy storage system. In final solution the FPGA chip has controlled rectifier and flywheel inverter. To meet this requirement, the FPGA has been chosen instead of DSP.

The digital control and regulation circuit has been based on the FPGA matrix EP3C16E144 from Cyclone III family manufactured by Altera/Intel. The eight-channel bipolar 12-bit A/D converter MAX1308 has been used for the measurement data acquisition. The applied converter allows fast conversion of analog data (conversion time of all channels $To = 1.98$ μs) and data transfer to the FPGA chip with bus throughput of 456 ksps. In addition, the controller has been equipped with: four galvanically separated general-purpose binary inputs, triple inputs according to the standard RS-422/RS-485 allowing the connection of e.g. a BLDC motor positioning system

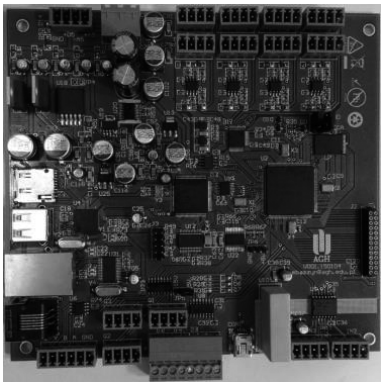


Fig. 6. A picture of the controller used for implementing the control system from Fig. 2

or an encoder, six binary outputs of voltage 15 V or 5 V, nineteen binary outputs aimed for transistor control. The controller board also comprises a microSD card socket, USB-OTG, and RJ45 socket allowing the system to be connected to the Internet.

A description of the control system structure has been prepared in the VHDL language (Very High Speed Integrated Circuits Hardware Description Language), using the Quartus II suite (version 13.1 Web Edition). All computational operations are based on a fixed-point notation. In the system it has been assumed that voltages and currents are described using sixteen-bit vectors, where the currents are represented in Q10 format, and the voltages – in Q5 format. The calibration block is responsible for adapting the data from A/D converters to the selected format. Such approach makes it possible to easily change the parameters during the transition from the HIL simulator to the real system. The algorithm for synchronization with the grid is operating on the basis of the principle of ABC-DQ conversion and is described in detail in [13]. As it results from the description of the control system, in order to determine the control it is necessary to know the phase voltages (Equations (6) and (7)). However, in many cases it is not possible to perform measurements of phase voltages, therefore line-to-line voltages are used for synchronization in the described solution. After a correct synchronization, the system introduces a phase shift of $\pi/6$ into the synchronized waveform, so that it corresponds to the phase voltages.

5. HIL simulation

Simulation techniques became a very important tool in the development and analysis of complex dynamic systems in recent years. Due to a significant increase in the computational capabilities of modern computers, engineers are able to easily perform analyses of the performance of the designed control systems in a short time. Thanks to the use of computer simulation, the correctness of a control algorithm can be verified without possessing a physical controller. Such an approach allows a significant reduction of the product development time, as well as substantial savings on costly physical prototypes.

The OP5600 simulator by OPAL-RT has been used during the work presented in this paper. The simulator is built on the basis of two six-core processors Intel Xeon Six-Core 3.33 GHz 12 M Cache 6.4 GT/s and the FPGA chip Xilinx Spartan 3 used for signal processing, it has

16 analog input channels, and 64 each of digital outputs and inputs. The analog outputs board OP5330 allows voltage signals in the range of $+/-15$ V to be generated with a sampling rate of 1 MS/s (simultaneous sampling of all channels) and a resolution of 16 bits. The digital outputs board OP5354 makes it possible to control 32 galvanically isolated channels, with simultaneous sampling up to 40 MS/s, with a high logic state voltage range of 5–30 V. The digital inputs board OP5353 comprises 32 optically isolated channels, sampled simultaneously at a rate up to 10 MS/s. The acceptable range of input voltages is 4–100 V.

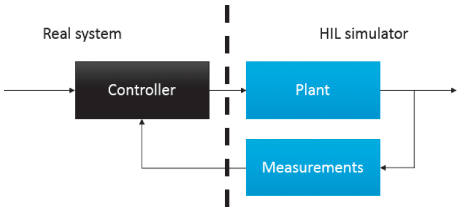


Fig. 7. HIL simulator concept

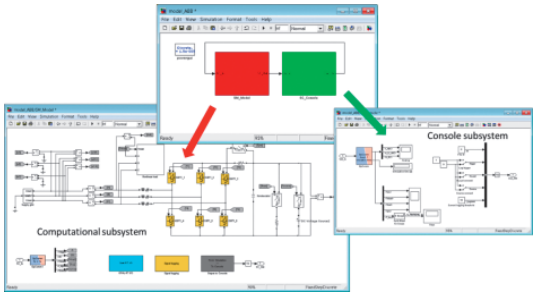


Fig. 8. Structure of the model with division into the computing subsystem and the console subsystem

The simulation model has been prepared in Matlab/Simulink software, using OPAL-RT and SimPowerSystemstoolboxes. It has been divided into the computing subsystem – comprising the SimPowerSystems model as well as I/O interfaces and saving the signals to a file, being calculated in the simulator, and the console model which is executed in the user computer and allows a non-line preview of the model state, as well as setting some input values (triggering the waveform logging, control signals for breakers and switches). After model preparation using the RT-LAB environment, the code and executable files have been generated. The structure of the model is presented in Fig. 8.

In the case of the real-time simulation a very important parameter to consider is the time step of simulation. The shorter the time step, the more precise the simulation results; the longer the time step, the more time for computation and the higher possible complexity of the model. The choice of adequate time step must be a result of careful analysis, and must take into account the computational complexity of the model and the switching frequency (the higher the switching frequency, the shorter the time step). The time step of simulation for the presented model has been established at 15 μs. In the case of inadequate choice of the time step system may become unstable, give inadequate results, and some of the transistor control signals may be missed as well (in the case of the modulation duty cycle near to 0 or 100%). An example of such situation is presented in Fig. 9. Fig. 9 presents the waveform of the phase voltage u_a, the phase current i_a, the PWM waveform generated by the controller (PWM_1), and the PWM waveform read by the OPAL simulator (PWM_2). The computation step set in the simulator was too large, which resulted in the control pulses not being correctly read. In the vicinity of the voltage crossing the amplitude value, the duration time of the transistor triggering pulse was shorter than the computation step, therefore the simulator did not identify that pulse, and as a result, it wrongly calculated the grid current.

Despite the performed testing of the control system using the tools of the Quartus II suite, numerical errors could be observed during initial starts of the controller with the OpalRT simulator, resulting in the flow of currents at the level of 1.5 kA and settling of the capacitor voltage at the level of 4.5 kV. After correcting the control program and removing the errors, tests of the control system have been performed. First, the basic assumptions set for the converter have been verified: stabilization of the capacitor voltage, the sinusoidal grid current in phase with the voltage (the system did not compensate the reactive power). Oscilloscope traces confirming the fulfillment of the set requirements (waveforms recorded with step switching on the DC receiver connected to the capacitor) are presented in Fig. 10.

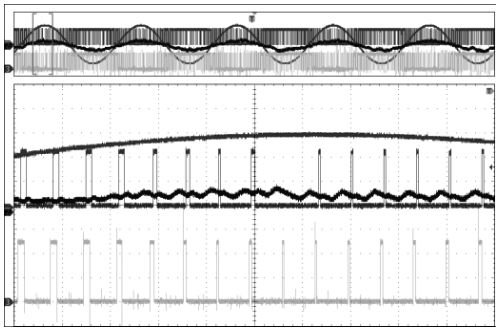


Fig. 9. Example of inadequately chosen computation step

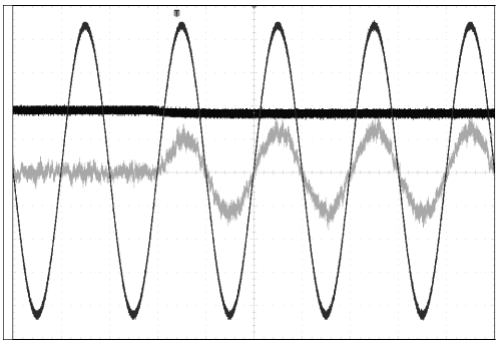


Fig. 10. Waveforms of the phase voltage u_a, power supply line current i_a, capacitor voltage u_{cf} at step switching on the DC receiver

After the receiver was connected, the capacitor voltage decreased by 0.5%, the grid current was sinusoidal and in phase with the voltage. Next, the operation of the converter as an active filter and a reactive power compensator has been verified (Fig. 10). A three-phase diode rectifier was connected with the DC receiver switched on.

In the case of a capacitor voltage increase above the set value, the tested system should return the energy from the capacitor to the grid. Oscilloscope traces recorded in such situation are presented in Fig. 11.

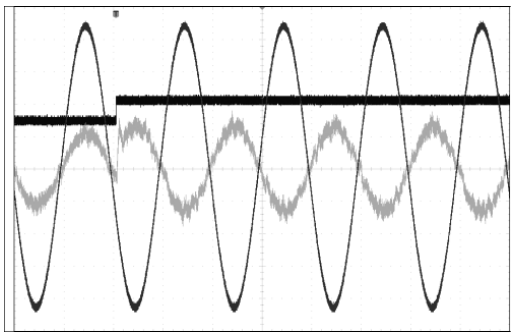
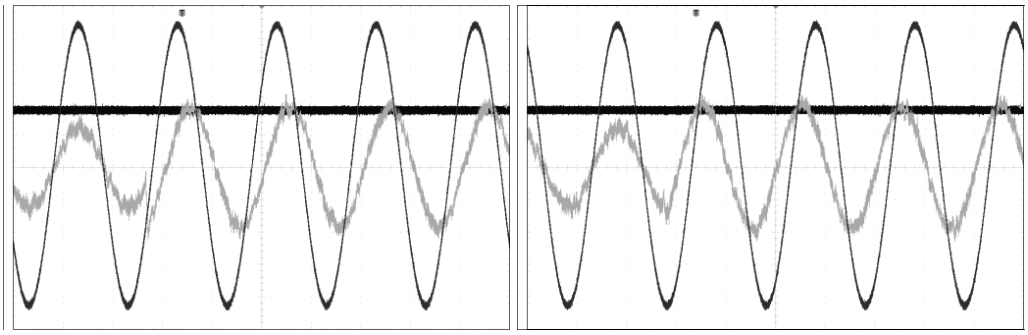


Fig. 11. Waveforms of the phase voltage u_a, grid current i_a, DC-link voltage at a step increase of the capacitor voltage forced by an external event (e.g. motor braking)

It follows from the presented oscilloscope traces that the system was performing correctly. After the set voltage of the DC-link was exceeded, the phase of the grid current has changed, and the inverter started to return energy to the mains.

Fig. 12 presents oscilloscope traces depicting the possibility of introducing a primary harmonic of reactive current of inductive character (Fig. 12a) and capacitive character (Fig. 12b) into the power supply line. The system receives the command to start to supply the reactive power of specified value from the master supervision system (e.g. from a local transmission system operator).



(a) (b)

Fig. 12. Waveforms of the phase voltage u_a, power supply line current i_a, capacitor voltage, phase shift φ between the voltage and current of the power supply line at introducing: (a) inductive; (b) capacitive

Fig. 13 presents the oscilloscope trace recorded during termination of returning energy to the power supply line at switched on DC- link receiver and filtering of higher harmonics of the nonlinear receiver.

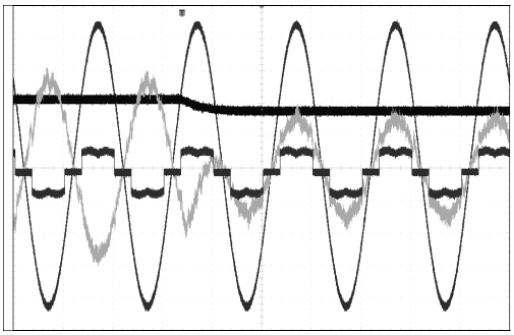


Fig. 13. Waveforms of the phase voltage u_a, power supply line current i_a, nonlinear receiver current i_{na}, capacitor voltage during termination of returning energy to the power supply line

6. Experimental setup

After completion of work with the HIL simulator, the verified algorithm was transferred into a real converter with a power circuit in accordance with the diagram from Fig. 3 and based on IGBT modules SK25GD126ET manufactured by Semicron (maximum switching frequency

equal 50 kHz). In the presented rectifier, switching frequency was equal 12 kHz. The frequency assumed was much below the capabilities of the used transistors because it was adapted to easier transition to a more powerful system using IPM modules. A system identical to the one used for realization of the HIL simulation (Fig. 6) has been applied as the control system. Since the analog outputs of the OPAL-RT simulator accepted values in the range of ± 15 V, whereas the real measurement channels gave signals at the level of ± 10 V, it was necessary to change the gains in the analog channels and the corresponding gains in the digital channel. These changes, together with verification of their correctness, required approx. 3 hours of work. Upon starting the experimental system, and confirming that the control system was operating correctly, the protection blocks were deactivated.

Since perfect sinusoidal waveforms of grid voltages had been assumed in Matlab/Simulink and HIL simulation, it was necessary to correct the settings of the regulators so that the grid current would be sinusoidal with deformed voltages. Use of deformed voltages in the HIL simulation would result in increasing the complexity of computations performed by the simulator, thus increasing the computation step.

Fig. 14 presents an oscilloscope trace recorded during precharge of the DC link capacitor.

After switching on the system, the transistors are blocked, the contactor ST2 (Fig. 2) remains open, and the capacitor charging current flows through the diodes of the transistor bridge. The value of the charging current is limited by the resistor R_r (time span t_1 in Fig. 4). After charging the capacitor to the amplitude value of the line-to-line voltage, the contactor ST2 short-circuits, the resistor R_r, and the transistors start pulsing, causing the capacitor voltage to increase to the set value (time span t_2 in Fig. 4). The value of the current within this time span is limited by the regulation system (the maximum value of the voltage regulator from Fig. 2).

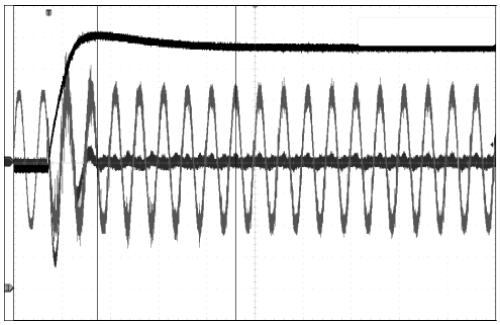


Fig. 14. Waveforms of the voltage and current of the power supply line during capacitor charging

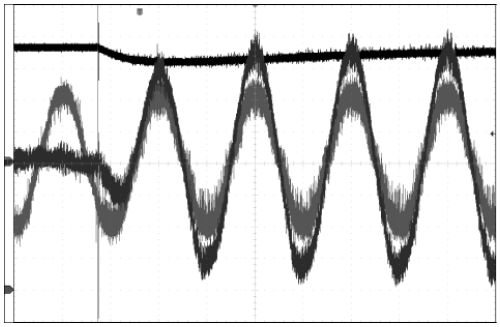


Fig. 15. Waveforms of the phase voltage u_a, power supply line current i_a, capacitor voltage u_{cf} at step switching on the DC receiver

Waveforms of the phase voltage u_a, grid current i_a, capacitor voltage u_{cf} at step switching on the DC receiver are presented in Fig. 15.

After the receiver was connected, the capacitor voltage decreased by 4.3%, and the grid current remained sinusoidal and in phase with the voltage. Oscilloscope traces depicting the operation of the rectifier as an active filter are presented in Fig. 16. A three-phase diode rectifier has been connected to the grid.

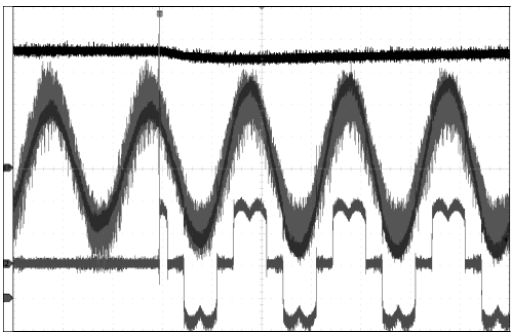
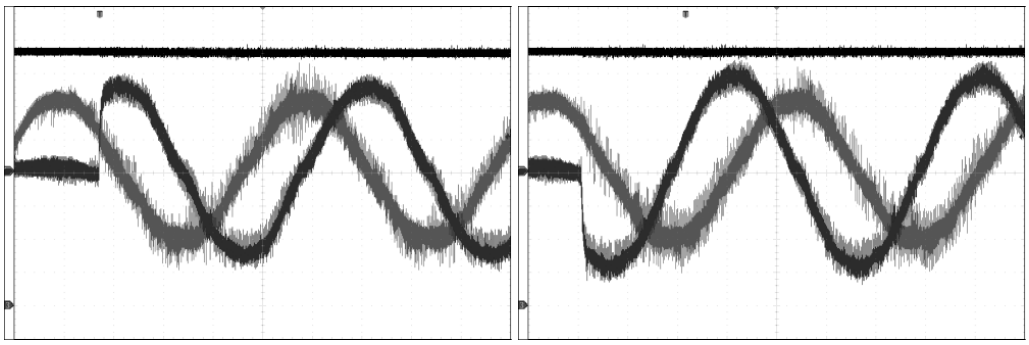


Fig. 16. Waveforms of the phase voltage u_a, power supply line current i_a, nonlinear receiver current i_{na}, capacitor voltage at switching on the diode rectifier

Fig. 17 presents oscilloscope traces depicting the system operation at introducing a primary harmonic of reactive current of inductive (Fig. 17a) and capacitive character (Fig. 17b) into the power supply line.



(a) (b)

Fig. 17. Waveforms of the phase voltage u_a, power supply line current i_a, capacitor voltage, phase shift φ between the voltage and current of the power supply line at introducing: (a) inductive; (b) capacitive reactive power into the mains

Fig. 18 presents oscilloscope traces recorded during returning the DC link energy to the grid.

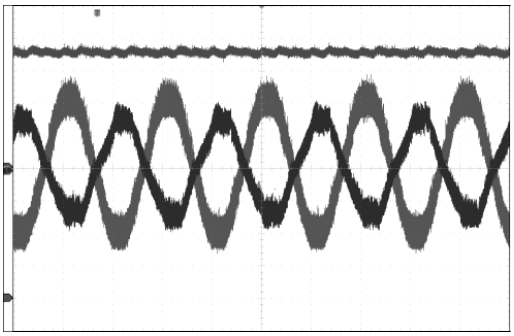


Fig. 18. Waveforms of the phase voltage u_a, power supply line current i_a, during returning energy to the power supply line

7. Summary

Because the ideal model of the grid has been used in the Matlab and HIL simulations (impedance is equal to zero, ideal sinusoidal voltage), it is difficult to make the quantitative comparison of these results with real measurements. In addition, in the HIL simulation the switching frequency was several times lower than in the test bed, therefore the results are not comparable. But comparing functionality (current shape, reactive power compensation, active filtration), the results obtained from the test bed match the results obtained in Matlab/Simulink and HIL simulation. This confirms the usability of these tools in prototyping of power electronics systems, especially in the case where the prototyped devices cooperate with a grid. The test of the control system with the OPAL-RT simulator made it possible to safely verify the correctness of system operation in both static and dynamic states (initial choice of regulator parameters). Errors which would cause damage to semiconductor elements and would be difficult to diagnose in operation of a real system with a grid, even a low-power one, have been detected and removed during operation with the HIL simulator. By progressing through the simulation stages described in the paper, the control system of the prototype has never reported exceeding the permissible value of the grid currents or the DC link capacitor voltage. Starting up the laboratory test bed required only a few hours of work in order to scale the measurement channels.

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