

DC-DC boost-flyback converter functioning as input stage for one phase low power grid-connected inverter

ADAM KAWA, ADAM PENCZEK, STANISŁAW PIROG

Department of Power Electronics and Energy Control Systems

AGH University of Science and Technology

e-mail: {penczek/adamkawa/pirog}@agh.edu.pl

(Received: 02.04.2014, revised: 08.06.2014)

Abstract. The paper treats about main problems of one phase DC-AC microinverters that allow single solar cell to be joined with the grid. One of the issues is to achieve high voltage gain with high efficiency in DC circuit, which is necessary for proper operation of inverter. The operating principles, results of practical implementation and investigations on boost-flyback converter, which meets mentioned demands, are presented. (high step-up DC-DC boost-flyback converter for single phase grid microinverter).

Key word: DC-DC high-step-up converter, boost converters, microinverters, renewable energy

1. Introduction

In recent years, as part of solutions related to “smart grids”, low power inverters have gained ever increasing popularity, enabling to utilize energy from single photovoltaic panels (power up to 300 W, MPP voltage range 25-50 V). This solution has numerous advantages, the most important of which is the possibility of optimum utilization of each PV panel (MPPT algorithm implementation [6] for single panels, which enables, among others, elimination of the effect of shading of serial connected cells), high level of scalability (installations can be made constructed out of ‘blocks’ functioning independently of each other). The requirements for the inverters of this type include mainly the overall dimension and price minimizing, high efficiency (over 90%), the execution of algorithms for maximum power point tracking with simultaneous fulfilling safety requirements (protection against island operation) as well as the electrical energy quality standards. Moreover, the connectability of any number of independently operating devices to a common grid is desirable.

Generally, the DC-AC converters can be divided into two groups: insulated [8, 10, 11] (most frequently with the use of a 50 Hz transformer or a high frequency transformer) and non-insulated [2, 9]. In view of the need to minimize costs and overall dimensions, in the case of microinverters it is advisable to use non-insulated systems. Their disadvantage is the

presence of earth currents flowing through parasitic capacities of PV panels and the need to obtain a high voltage gain at the DC voltage side.

Figure 1 shows the scheme of a typical, non-insulated grid converter supporting photovoltaic panels.

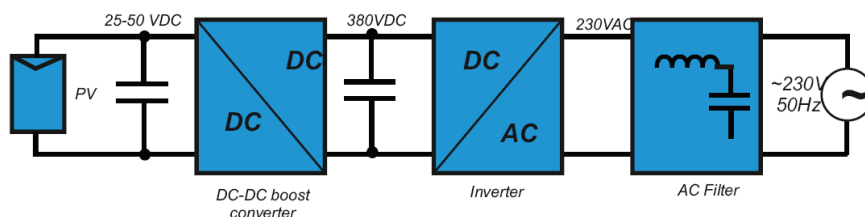


Fig. 1. Block diagram of a system for acquiring energy from PV

It is composed of several elements: DC-DC converter; capacitor assembly, enabling buffering of the energy related to the changing value of the momentary power in a one phase grid (100 Hz component) and the elimination of the switching frequency current components, DC-AC inverter and AC filter (most frequently of LC or LCL type). One of the basic issues in transformerless converters is to achieve a considerable voltage value increase from the input level of 25-50 V to the level required for the correct mains inverter operation. Assuming the use of a full bridge inverter, for the rated voltage in European grids (230 V) it is around 380 V (in the United States, the issue is not so significant due to the lower one phase grid voltage of 120 V). It means that the DC-DC converter must operate with the gain of $K = 7.7-15.2$, which is not easy to obtain without a considerable efficiency loss. This paper analyzes the properties of a typical DC-DC converter increasing voltage in operating conditions with a high duty cycle D . Existing solutions were analyzed, enabling to improve the operating conditions of the voltage increasing system [1-7, 12, 13, 15]. Next, one of the typologies was singled out, being a combination of a boost converter and a flyback converter, operating with a two coupled winding choke [3, 4]. Subsequent points describe the converter operating principle and present results of simulation tests and actual model tests, with parameters fulfilling the assumptions presented at the beginning of the paper ($U_{in} = 30$ V, $U_{out} = 380$ V, $P_{out} = 300$ W).

2. DC-DC boost converter – limitations

Due to the structure simplicity, in numerous converters a preferred solution is the use of a conventional DC-DC boost converter (Fig. 2).

According to [4], actual DC-DC boost converter gain value including the influence of parasitic elements is described by the following formula:

$$K = \frac{U_{in}}{U_{out}} = \frac{R_o}{\frac{r_{Lp} + D \cdot r_{ds_on}}{1 - D} + r_{diode} + D \cdot \left(\frac{r_c R_o}{r_c + R_o} \right) + R_o (1 - D) \left(1 + \frac{U_D}{U_{out}} \right)}, \quad (1)$$

where: U_D – voltage drop on a diode during conduction; D – PWM duty cycle; r_{Lp} – choke serial resistance; r_{dson} – MOSFET transistor conduction resistance; r_c – capacitor serial resistance; R_o – load resistance; r_{diode} – diode equivalent resistance can be calculated on the basis of the catalog specifications (U_F/I_F).

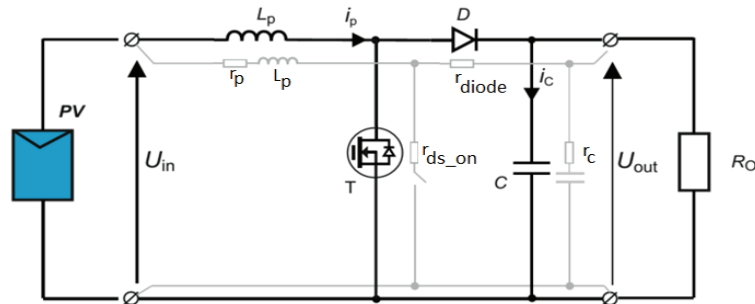


Fig. 2. Boost converter circuit including parasitic elements

After substituting actual elements parameters to the formula (1), the output characteristics of the DC-DC boost converter was obtained for two cases, $U_{in} = 25\text{ V}$ and 50 V . It was assumed that the maximum output power is 300 W (for $U_{out} = 380\text{ V} \rightarrow R_o = 481\ \Omega$).

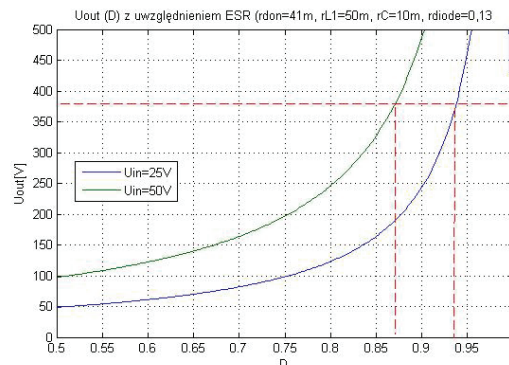


Fig. 3. DC-DC boost converter voltage characteristics including the influence of parasitic elements ($r_{donMOSFET} = 41\text{ m}\Omega$, $r_{Lp} = 50\text{ m}\Omega$, $r_c = 10\text{ m}\Omega$, $r_{diode} = 50\text{ m}\Omega$)

The DC-DC boost converter allows for obtaining a very high efficiency, but with the gain coefficient of around 2 ($D = 0.5$). However, as it results from the characteristics shown in Figure 3, in order to fulfill the design assumptions for the microinverter ($U_{out} = 380\text{ V}$), the device should operate with the duty cycle D of $0.87 \div 0.94$. The operation with such high duty cycles involves efficiency deterioration, the main reason of which are the MOSFET transistor switching losses (high voltage on element, diode reverse current flowing during the transistor commutation process). It is confirmed by the test results of an actual system with the following parameters: $U_{in} = 35\text{ V}$, $L_p = 1400\ \mu\text{H}$, $r_{Lp} = 60\text{ m}\Omega$, IPW60R041 MOSFET transistor ($R_{dson} = 41\text{ m}\Omega$), FFH30S60S diode ($I_N = 30\text{ A}$, $t_{rr} < 40\text{ ns}$), shown in Figures 4a and 4b.

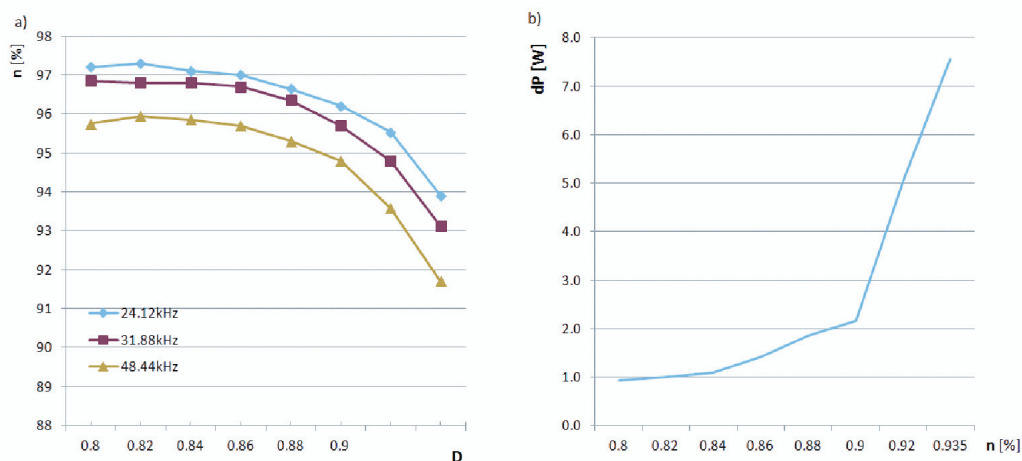


Fig. 4. a) DC-DC converter efficiency characteristics measured for 3 different switching frequencies; b) switching losses in duty cycle function

As can be read from Figure 4a, at high (above 0.82) D coefficient values, the efficiency rapidly decreases (due to the significant increase in the share of switching losses – characteristics in Figure 4b).

3. Alternative solutions

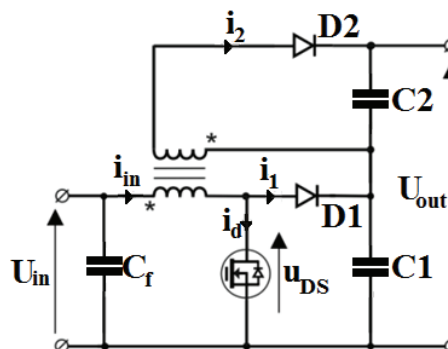
In order to improve the operating parameters of the DC-DC system, multilevel systems can be used [5] or boost converters can be connected serially [2], with one converter operating at low frequency and the other operating at high frequency. However, a disadvantage of this solution is the cost of elements and problems with the system stability in the case of a closed control system operation. Another solution may be the use of a flyback converter. In this case, the effect of efficiency decrease also occurs at high voltage gain values [14]. Additionally, the semiconductor element is exposed to high overvoltages, the source of which is the transformer leakage inductance.

The references describe numerous solutions allowing for obtaining high direct voltage gain. The references [1] and [2] classify and describe in detail the most important ones, dividing them into four categories:

- systems with coupled inductances;
- systems with switched capacitances;
- systems with coupled inductance and switched capacitances.

After analyzing various solutions, considering the requirements set by the microinverter application (structure simplicity, low cost), the boost-flyback (BF) DC-DC converter system described in [3] and [4] was chosen for tests. Figure 5 shows the system diagram. The system is a combination of a boost converter and a flyback converter, which use a common mutually coupled winding choke.

Fig. 5. Boost-flyback converter diagram



The BF converter output voltage is the sum of voltages from flyback converter (3) and boost converter (2):

$$\frac{U_{C1}}{U_{in}} = \frac{1}{1-D}, \quad (2)$$

$$\frac{U_{C2}}{U_{in}} = n \frac{D}{1-D}, \quad (3)$$

$$K_u = \frac{U_{out}}{U_{in}} = \frac{U_{C1} + U_{C2}}{U_{in}} = \frac{1}{1-D} + \frac{nD}{1-D} = \frac{1+nD}{1-D}, \quad (4)$$

$$U_{out} = \frac{1+nD}{1-D} \cdot U_{in}, \quad (5)$$

where: n – coupled inductance turns ratio.

The derived formula for the system output voltage (5) concerns the continuous magnetic flux mode operation, i.e. the situation in which the energy stored in the choke at no point in time decreases to zero. As it results from the relationship (5), in comparison with a standard boost converter, the boost-flyback converter at the same duty cycle allows for obtaining higher voltage gain value, which additionally can be fixed by means of an appropriate selection of turns ratio in coupled choke. Moreover, in the boost-flyback converter, unlike in the flyback topology, no voltage spikes occur on the transistor. It is so because the energy stored in the choke primary winding leakage inductance is transferred to the output capacitor C_1 . Hence, there is no need to use overvoltage protection elements.

4. DC-DC boost-flyback converter – operating principle

The boost-flyback converter is described in detail in [3] and [4]. The system operation concept (Fig. 7) can be presented by analyzing successive operation intervals shown in Figure 6.

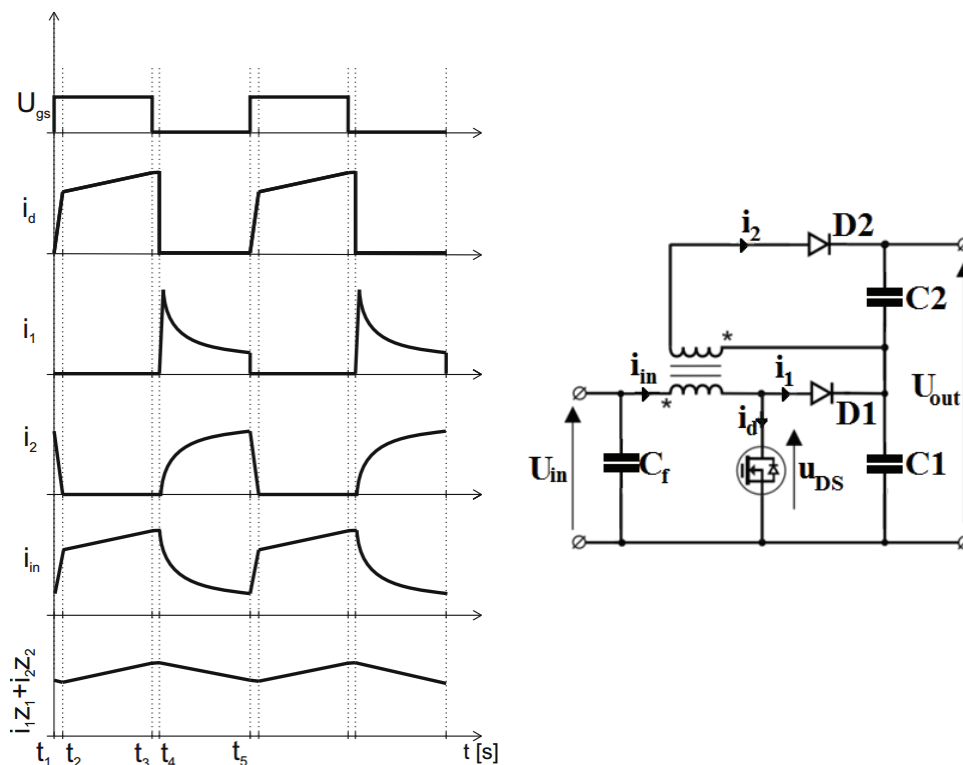


Fig. 6. Current and voltage waveforms in BF converter

- t_1-t_2 – time interval immediately after switching on the power transistor; at the beginning diode D_2 is biased in the conduction direction because the energy from the secondary winding leakage inductance is carried away; i_2 still has a non-zero value. The moment the whole leakage inductance energy is carried away to load, diode D_2 becomes reverse biased.
- t_2-t_3 – during this time period diodes D_1 and D_2 are reverse biased. The current is building up in the choke primary winding, hence the energy is accumulated, while the output capacitors C_1 and C_2 supply the load.
- t_3-t_4 – during this time period the power transistor is switched off and its output capacitance C_{oss} is charged with the use of the choke primary winding current.
- t_4-t_5 – this time interval begins when the voltage on the MOSFET transistor reaches the value sufficient for diodes D_1 and D_2 to be biased in the conduction direction. Before instant t_4 current flowed through the choke primary winding leakage inductance, and due to the lack of other significant inductances in the loop, the current i_1 increases with a very high derivative at the beginning of the interval. The situation is different at secondary winding side. Since t_4 , the secondary winding current i_2 increases from the zero value. Because of the presence of the leakage inductance and parasitic resistances in the loop, the current i_2 increases exponentially in time function. It is assumed that the output capacities

C_1 and C_2 are sufficiently high so that during the one period of converter operation the voltage on them does not change. This means that during the diodes conduction, the flux as well as the choke magnetomotive force (MMF) ($\theta = z_1 i_1 + z_2 i_2$) is decreasing linearly (omitting winding serial resistance). These observations lead to a conclusion that during the interval t_3-t_4 , the primary winding current waveform in shape reflects the exponential waveform of current i_2 . Since the converter input current is the sum of currents i_1 and i_d , it is characterized by a high ripple, not resulting directly from the choke primary winding inductance value.

Reference [4] analyzes in detail the BF converter operation including parasitic elements (Fig. 7). On the basis of this analysis, a formula for the converter voltage gain (6) was derived.

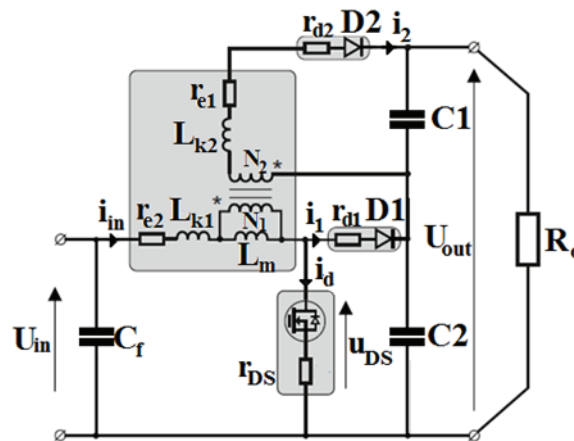


Fig. 7. BF converter diagram including parasitic elements

$$K_{uESR} = K_u \frac{1 - \frac{(1-D) U_{D1} + U_{D2}}{1+nD} \frac{U_I}{U_I}}{1 + \frac{1}{1-D} \frac{1}{R_o} (r_{e1} + r_{e2} + r_{D1} + r_{D2}) + \frac{1}{(1+D)^2} \frac{1}{R_o} (1+n)^2 D (r_{e1} + r_{DS})} \quad (6)$$

$$K_u = \frac{1+nD}{1-D},$$

where: U_{Dx} – voltage drop on a diode during conduction; D – PWM duty cycle; r_{e1}, r_{e2} – choke winding serial resistances; r_{ds} – MOSFET transistor conduction resistance; R_o – load resistance; r_{D1}, r_{D2} – D_1 and D_2 diodes equivalent resistance (calculated on the basis of the catalog specifications). On the basis of the relationships (6) and (5), Figures 8-10 feature voltage gain characteristics for boost converters and boost-flyback converters. The following parameters were taken: $r_{e1} = 50 \text{ m}\Omega$; $r_{e2} = n \cdot r_{e1}$; $r_{D1} = r_{D2} = 130 \text{ m}\Omega$; $R_L = 481 \text{ }\Omega$; $U_{D1} = U_{D2} = 1,95 \text{ V}$; $U_{in} = 6 \text{ V}$.

Figure 8 shows a compilation of gain characteristics for boost converters and boost-flyback converters ($n = 2$). Their comparison shows undoubtedly that the BF system voltage gain is higher at the same coefficient D .

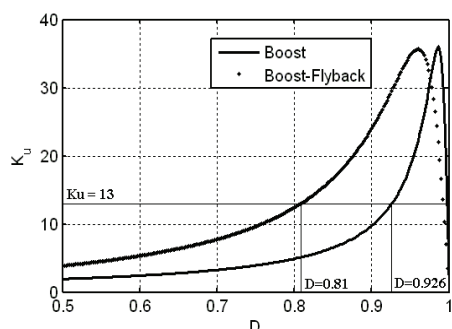


Fig. 8. Boost and BF converter ($n = 2$) voltage gain comparison

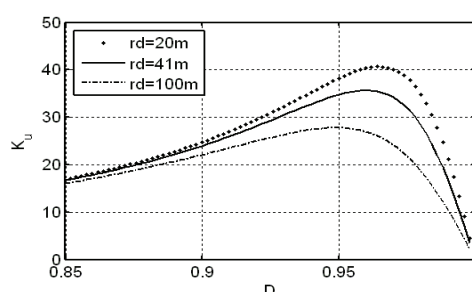
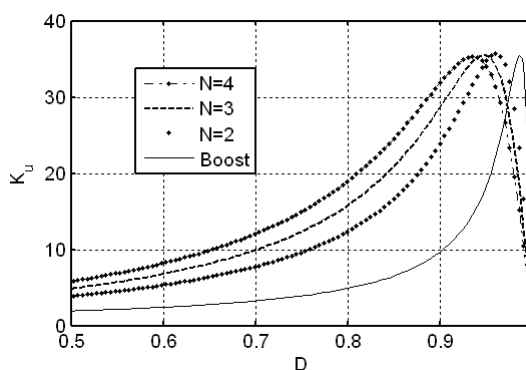


Fig. 9. BF converter voltage gain in duty cycle function for various transistor resistances

Figure 9 shows the influence of MOSFET transistor resistance on DC voltage gain characteristics. It is clearly visible that this parameter has a considerable influence on voltage gain only at coefficients $D > 0.9$. When designing the boost-flyback converter, two key parameters should be determined, i.e. the coupled choke turns ratio and the primary winding inductance. Apart from the converter voltage gain $K_u(D)$, the value of the choke turns ratio n also affects the whole system efficiency. The selection of a high turns ratio allows for limiting the MOSFET transistor operating voltage, which in turn enables the use of a low channel resistance element. In such case, it is possible to use diode D_1 with a low allowable reverse voltage. In a specific situation, it would be a Schottky diode. Apart from a low forward voltage, the Schottky diode is characterized by a very low reverse recovery charge value, which in the boost converter (as in BF) definitely deteriorates the power transistor switching conditions, thus decreasing the efficiency. High coupled choke turns ratio involves the need to use a diode with a considerable allowable reverse voltage as D_2 . The turns ratio should be optimized (for specific application requirements and available elements) in order to obtain the best possible efficiency of the whole boost-flyback converter. Figure 10 shows the BF converter gain characteristics in relation to the duty cycle for various turns ratios (obtained on the basis of the relationship (6)). For comparison, the same chart features also the boost converter characteristics.

In order to determine the required magnetising inductance (in the reduction: of the primary winding inductance), a formula should be used which determines the value of inductance for operation at the border of the choke magnetic flux continuity.

Fig. 10. BF converter voltage gain at various turns ratios and Boost gain ($R_{ds_on} = 41 \text{ m}\Omega$)



On the basis of [4], the critical inductance value is as follows:

$$L_k = \frac{1}{2} \frac{(1-D)^2}{(1+nD)^2} R_o D T_s. \quad (7)$$

5. Test setup

In order to verify the analytical deliberations and simulation tests results, a test setup was constructed, which allowed for conducting the laboratory tests of the boost-flyback converter (Fig. 11, 12).

The DC-DC boost-flyback converter system was designed for operation with the input voltage within the range of 25-50 V. The designed DC-DC converter rated power is 300 W at the output voltage of 380 V. The following power semiconductor elements were selected: IPW60R041 MOSFET transistor ($R_{ds_on} = 41 \text{ m}\Omega$), DSEP30-12A diodes. ($I_N = 30 \text{ A}$; $t_{rr} < 40 \text{ ns}$; $U_F = 1200 \text{ V}$)).

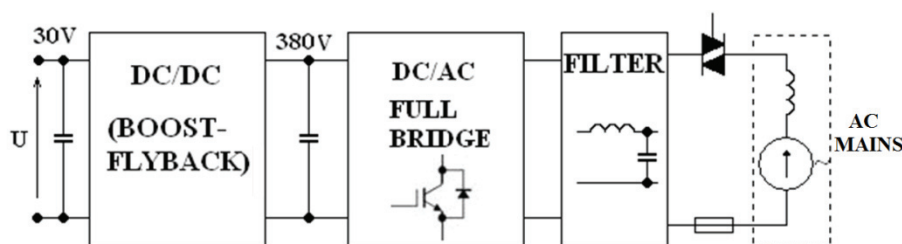


Fig. 11. Block diagram of the DC/AC converter allowing for obtaining energy from a single photovoltaic panel

In order to conduct tests in conditions similar to actual conditions, a possibility was provided to load the system with the use of a single phase voltage inverter (4 H bridge with LC filter). However, majority of the laboratory tests were conducted with the use of a the resis-

tance load. Additionally, on the input to the DC-DC converter, a capacitor filtering the converter current (containing a considerable AC component) was placed. Figure 12 shows a photo of the test bed.

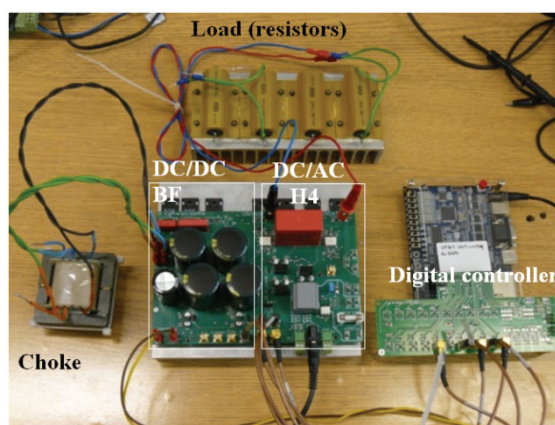


Fig. 12. Photo of the test setup

6. Coupled winding choke design and execution

In the flyback converter, it is necessary to provide a good magnetic coupling between the primary and secondary windings. Failure to meet this requirement results in voltage spikes on the transistor, the elimination of which with the use of additional snubber circuit requires dissipation of the energy – the poorer the winding coupling is, the higher loss energy must be dissipated. For this reason, various transformer winding methods are used for system topologies of this type, e.g. consisting in placing the primary winding in a layer between the divided secondary winding. For the system with the boost-flyback topology this requirement is not so critical. At certain leakage inductances, only the voltage on the capacitor C_2 will decrease, which may not be desirable but does not radically decrease the efficiency. The energy stored in the primary winding leakage inductance does not have to be lost in ancillary systems (such as is the case in flyback systems), because it is naturally released to the capacitor C_1 .

The designing of the coupled choke for the boost-flyback system consists in determining the required primary winding inductance and saturation current, and, on the basis of this value, calculating the required number of winding turns and magnetic gap length. The number of turns of the secondary winding was calculated on the basis of the required turns ratio value. In order to obtain the designed value of the voltage on the capacitor C_2 , the resulting number of turns of the secondary winding was increased by around 10%, to compensate for the voltage loss on resistances and leakage inductances. The choke for the test system was equipped with three windings (Fig. 13), one primary winding located between two secondary ones. This configuration allows for obtaining four secondary winding connection options which differ by the equivalent resistance and leakage inductance:

Option 1. The secondary winding in the deepest layer (L2) has the lowest resistance and the highest coupling coefficient in relation to the primary winding (L1).

Option 2. The secondary winding in the top layer (L3) has a higher serial resistance and a lower coupling coefficient in relation to the primary winding.

Option 3. The parallel connection of the secondary windings enables to obtain the lowest serial resistance and the highest coupling coefficient.

Option 4. The serial connection of the windings enables to obtain a turns ratio n of 1 : 2.

Fig. 13. Choke windings connection diagram for various options and choke cross section with indicated winding arrangement

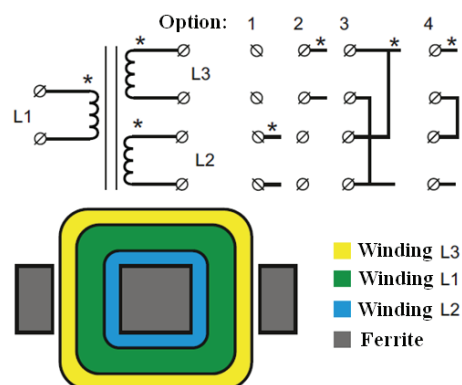


Table 1 presents the measured choke winding parameters, while Table 2 lists the measured magnetic coupling coefficients for each of the secondary winding connection options.

Table 1. Choke winding parameters

Winding	Resistance [m Ω]	Self-inductance [μ H]
L1	50	610
L2	130	749
L3	165	762

Table 2. Secondary winding parameters at various connections

Option	Coupling coefficient k	Turns ratio n
(L1 – L2)	0.992	1: 1.13
(L1 – L3)	0.983	1: 1.13
(L1 – L2 L3)	0.993	1: 1.13
(L1 – L2 + L3)	0.990	1: 2.26

7. Laboratory tests

The waveforms from the DC-DC converter system operation with resistance load ($R_L = 474 \Omega$) are shown in Figure 14.

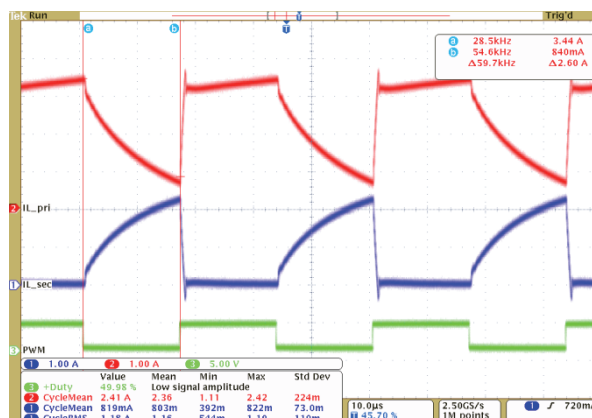


Fig. 14. Waveforms from DC-DC BF system operation with resistance load: 1 – diode D2 current(1 A/div), 2 – input current (1 A/div), 3 – PWM signal (1 A/div)

Figure 15 shows waveforms from the inverter operation (with RL load), supplied from the DC-DC BF converter.

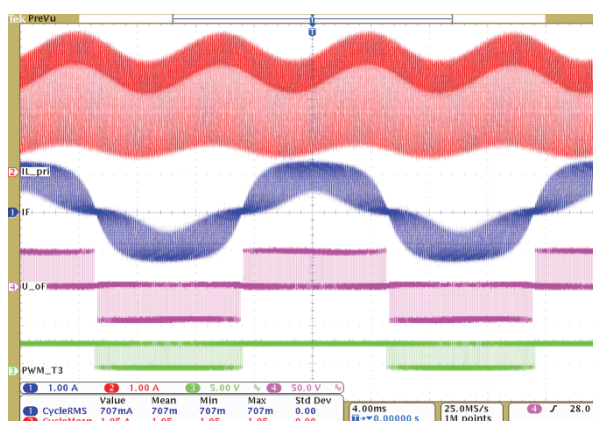


Fig. 15. Waveforms from DC-DC and DC-AC systems operation with resistive load: 1 – inverter output current (1 A/div), 2 – DC-DC converter input current (1 A/div), 3 – PWM signal for one of inverter transistors, 4 – inverter output voltage (50 V/div)

As results from the measurements, the converter input current (Figure 14, waveform No. 2) has a high AC component of high frequency, which is a disadvantage of this solution. In order to restrict the input current ripple, the additional filtration at the input to the DC-DC system should be used.

As part of the laboratory works, the boost-flyback output voltage vs duty factor D characteristic curves were measured, loaded with the resistance $R_L = 474 \Omega$. The value of the input voltage was fixed at 30 V. The output voltage was determined as the sum of the voltages measured on both output capacitors C_1 and C_2 (Fig. 17). The output voltage characteristics in duty cycle function various choke winding connection options are shown in Figure 16.

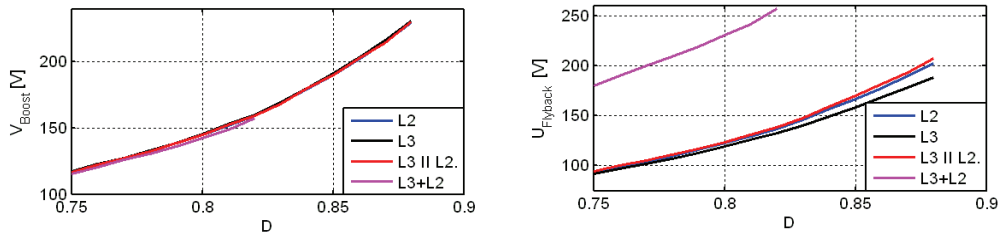


Fig. 16. Control voltage characteristics $U(D)$ for boost module (U_{C1}) and flyback module (U_{C2}) in DC-DC boost-flyback converter

It should be noted that the winding connection option (hence the choke parasitic parameters value) has significant influence on the flyback converter voltage (U_{C2}), while it has very little influence on the value of the boost converter output voltage (U_{C1}). The influence of the choke parasitic elements becomes more important as the duty cycle increases.

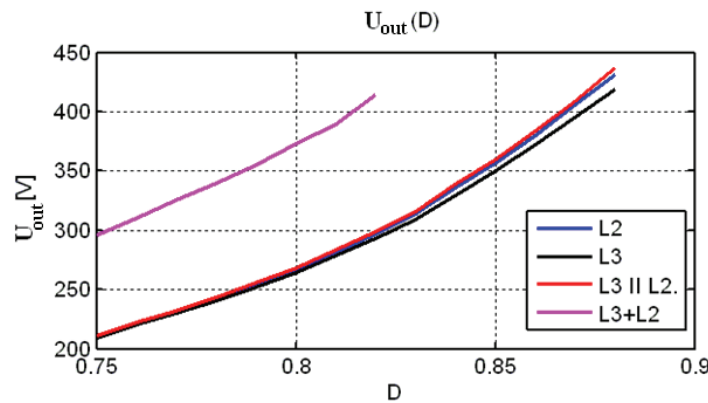


Fig. 17. Total converter output voltage $U_{out} = U_{C1} + U_{C2}$ in duty cycle function for various choke connection options

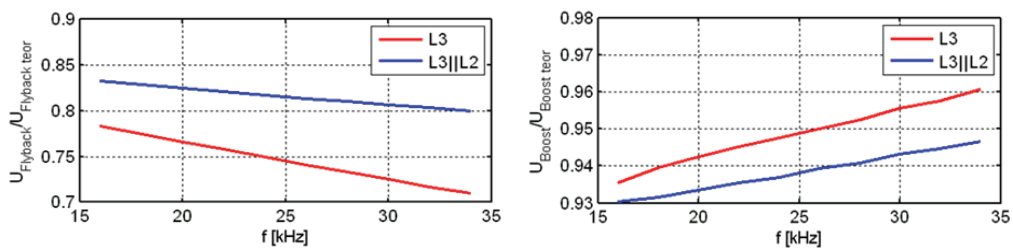


Fig. 18. Voltage $U_{Flyback}(U_{C2})$ and $U_{Boost}(U_{C1})$ in relation to theoretical values depending on the operating frequency

In order to show the influence of the leakage inductance on the output voltage, measurements were taken at constant set duty cycle $D = 0.87$, constant load resistance $R_L = 474 \Omega$ and

changed pulse frequency. The characteristics were measured for two extreme choke secondary winding connection options, i.e. for winding L3 only (with the lowest coupling in relation to L1) and for the parallel connection of windings L2 and L3 (best coupling). In the characteristics shown in Figure 18, the measured voltages are related to the theoretical values calculated for ideal elements, i.e. according to formulas (2) and (3).

For the flyback converter, the voltage (U_{C2}) increases as the frequency increases. Moreover, in the case of the configuration with a poorer winding magnetic coupling, the voltage deviation from the theoretical value is higher. The boost converter voltage increases as the frequency increases, but this variation falls within a considerably lower range than in the case of voltage U_{C2} . Since the elements serial resistances in approximation do not change their influence on the voltages $U_{\text{Flyback}}(U_{C2})$ and $U_{\text{Boost}}(U_{C1})$ at frequency change (total lack of the frequency parameter in formula (6)), it should be concluded that the winding leakage inductance is responsible for this property. From the analysis of the characteristics shown in Figures 17 and 18, it follows that the winding leakage inductances have considerable influence on the converter output voltage, and their omission in formula (6) is a large approximation; the larger, the higher is the assumed switching frequency.

8. Summary

The paper presents the DC-DC boost-flyback converter enabling the adjustment of the photovoltaic panel output voltage (25÷50 V) to the level required by the voltage inverter (380 V). The use of this typology allows for obtaining high voltage gain coefficients at relatively low coefficient D (in relation to the boost converter). In comparison with other solutions, alternative to the conventional boost converter, the system is composed of a small number of elements. Moreover, it can operate with a choke of low inductance value (despite the operating mode, the input current contains a high variable component). With appropriate selection of turns ratio ($n \geq 2$), it is possible to limit the MOSFET transistor operating voltage value (this means the possibility to use a low channel resistance element) and boost converter diode operating voltage (which in turn enables the usage of the Schottky diode, characterized by a low transient charge and low voltage in the conduction state). As a result, the losses in the boost converter circuit decrease. A disadvantage of the boost-flyback system is a high AC component occurring in the input current. In order to avoid the phenomenon of the photovoltaic panel accelerated ageing related to the high AC component, it is necessary to use additional input filters.

References

- [1] Meneses D., Blaabjerg F., García O., Jose A.C., *Review and Comparison of Step-Up Transformerless Topologies for Photovoltaic AC-Module Application*. IEEE Transactions on Power Electronics 28(6): 2649-2663 (2013).
- [2] Li W., He X., *Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications*. IEEE Trans. Ind. Electron. 58(4): 1239-1250 (2011).

- [3] Tseng K.C., Liang T.J., *Novel high-efficiency step-up converter*. Proc. Inst. Elect. Eng. Elect. Power Appl. 151(2): 182-190 (2004).
- [4] Liang T.J., Tseng K.C., *Analysis of integrated boost-flyback step-up converter*. Proc. Inst. Elect. Eng. Elect. Power Appl. 152(2): 217-225 (2005).
- [5] Pirog S., Baszynski M., Czekonski J. et al., *Multicell DC/DC Converter with DSP/CPLD Control. Practical Results*. Power Electronics and Motion Control Conference, EPE-PEMC 2006, 12th International (2006).
- [6] Stala R., Koska K., Stawiarski L., *Realization of Modified Ripple-based Mppt in a Single-phase Single-stage Grid-connected Photovoltaic System*. Industrial Electronics (ISIE), IEEE International Symposium (2011).
- [7] Stala R., *The Switch-Mode Flying-Capacitor DC-DC Converters With Improved Natural Balancing Industrial Electronics*. IEEE Transactions on Industrial Electronics 57(4): 1369-1382.
- [8] Rodriguez G., Andres L., Balda J.C., *A Comparison of Isolated DC-DC Converters For Microinverter Applications*. Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE (2013).
- [9] Pirog, S., Baszynski M., *Modelling a Single Phase Multicell DC/AC Inverter Using FPGA*. Przegląd Elektrotechniczny 84(2): 84-87 (2008).
- [10] Stawiarski L., Szarek M., Mondzik A., Penczek A., *Single-phase Grid-connected Photovoltaic System With Variable Control Structure*. Przegląd Elektrotechniczny 89(2a): 34-39 (2013).
- [11] Stawiarski L., Szarek M., Mondzik A. et al., *Single-phase Grid-connected Photovoltaic System*. Przegląd Elektrotechniczny 88(2): 218-222 (2012).
- [12] Janke W., *Averaged Models of Pulse-modulated DC-DC Power Converters. Part I. Discussion of Standard Methods*. AEE 61(4), (2012).
- [13] Janke W., *Averaged Models of Pulse-modulated DC-DC Power Converters. Part II. Discussion of Standard Methods*. AEE 61(4), (2012).
- [14] Halder T., Kalyani N., *Comprehensive Power Loss Model of the Main Switch of the Flyback Converter*. International Conference on Power, Energy and Control (ICPEC) (2013).
- [15] Dawidziuk J., *A Dual Inductor fed Boost Converter With an Auxiliary Transformer and Voltage Doubler*. Bulletin of the Polish Academy of Sciences. Technical Sciences 61(4): 787-791 (2013).