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Problems related to the correct determination of switching power losses in high-speed SiC MOSFET power modules

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Abstract. High-speed switching capabilities of SiC MOSFET power modules allow building high power converters working with elevated switching frequencies offering high efficiencies and high power densities. As the switching processes get increasingly rapid, the parasitic capacitances and inductances appearing in SiC MOSFET power modules affect switching transients more and more significantly. Even relatively small parasitic capacitances can cause a significant capacitive current flow through the SiC MOSFET power module. As the capacitive current component in the drain current during the turn-off process is significant, a commonly used method of determining the switching power losses based on the product of instantaneous values of drain-source voltage and drain current may lead to a severe error. Another problem is that charged parasitic capacitances discharge through the MOSFET resistive channel during the turn-on process. As this happens in the internal structure, that current is not visible on the MOSFET terminals. Fast switching processes are challenging to measure accurately due to the imperfections of measurement probes, like their output signals delay mismatch. This paper describes various problems connected with the correct determination of switching power losses in high-speed SiC MOSFET power modules and proposes solutions to these problems. A method of achieving a correct time alignment of waveforms collected by voltage and current probes has been shown and verified experimentally. In order to estimate SiC MOSFET channel current during the fast turn-off process, a method based on the estimation of nonlinear parasitic capacitances current has also been proposed and verified experimentally.

Key words: SiC MOSFET; power modules; channel current; switching losses; time alignment.

1. INTRODUCTION

Nowadays, silicon carbide (SiC) MOSFETs are commonly used in a wide range of power electronics converters where high switching frequency, high efficiency, and high power density are required [1–7]. They proved to be reliable successors of silicon-based transistors in many applications, and currently, they are being used in large-scale projects like electric cars traction inverters [8, 9], electric buses traction inverters [10, 11], high power battery chargers [12–14], or new generation power electronics converters sets for locomotives [15]. As the converters operate at elevated switching frequencies, proper estimations of switching power losses are essential during the design and prototyping process. Today, the most common method of determining switching power losses in SiC MOSFETs is a calculation based on switching energies determined during double-pulse tests. These energies are determined based on an integral of the instantaneous power measured across the transistor during the switching process [16]. However, because SiC MOSFETs are much faster than their Si equivalents, this method may lead to high errors [17]. Such an error is usually related to nonlinear parasitic capacitances appearing in MOSFETs combined with fast switching. Fast switching processes are associated with very steep slopes of voltage and current waveforms, not to mention high-frequency oscillations. SiC MOSFETs have very low parasitic capacitances compared with same rated Si transistors due to much smaller chip sizes [5, 18–21]. However, taking into account very fast switching, currents flowing through parasitic capacitances of SiC MOSFETs can be significant [22]. During the turn-off process, as these currents do not flow through the SiC MOSFET channel, they do not participate in the heat generation associated with the current conduction through the MOSFET resistive channel [23, 24]. At the same time, power losses connected with current flowing through parasitic capacitances in SiC MOSFETs are negligible compared with channel power losses during switching processes [25]. The problem is that during the turn-on process, charged parasitic capacitances discharge through the MOSFET resistive channel and that current is not visible on the MOSFET terminals. Thus the turn-on switching energy is higher than observed. On the other hand, measuring the MOSFET drain current with a probe during the turn-off process provides a waveform of combined channel current and parasitic capacitances currents. In order to determine switching power losses correctly, it is crucial to separate MOSFET channel current component and parasitic capacitances current components and use only the channel current component to determine instantaneous power losses in a tran-

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sistor. Considering fast switching processes in SiC MOSFETs and the fact that oscilloscope probes often exhibit different output signal delays, proper time alignment of the waveforms obtained with the oscilloscope probes during commutation tests is necessary and also crucial for proper switching power losses determination [26].

This paper describes various problems connected with the correct determination of switching power losses in high-speed SiC MOSFET power modules, which could have been neglected in the case of the slow-switching Si semiconductors, and proposes solutions to these problems. In order to estimate SiC MOSFET channel current, a method based on the estimation of nonlinear parasitic capacitances current has been proposed. In this article, the origin of power losses in a MOSFET transistor has been explained. A design of a dedicated testbench for switching power losses determination in high-speed SiC MOSFET power modules has been shown. A method of achieving a correct time alignment of waveforms collected by voltage and current probes has been shown. The prepared testbench has been tested, and the obtained SiC MOSFET power modules switching energies have been compared with data provided by manufacturers. The issue of parasitic capacitances in SiC MOSFETs and their impact on the switching energies determination process has been raised. A method of separating the SiC MOSFET channel current component from the measured drain current waveform during the turn-off process has also been presented and discussed. Experimental results of the turn-off switching energies obtained with the proposed method of determining switching energies have been compared with the results obtained using the commonly used method considering the integral of the instantaneous values of the measured drain-source voltage and the measured drain current during switching processes.

2. POWER LOSSES IN MOSFET TRANSISTORS

Power losses in MOSFET transistors are related to the resistive nature of the MOSFETs channels during current conduction. For an idealized MOSFET transistor (without parasitic capacitances and inductances), the instantaneous power losses in a MOSFET transistor can be expressed as the product of instantaneous values of the drain-source voltage and the drain current, as shown in equation (1).

$$p_{LOSS}(t) = v_{DS}(t) i_D(t), \tag{1}$$

where:

- $p_{LOSS}(t)$ represents the instantaneous power losses in the transistor,
- $v_{DS}(t)$ represents the instantaneous drain-source voltage,
- $i_D(t)$ represents the instantaneous drain current.

Considering the MOSFET transistor operation in a power electronics converter, power losses are divided into power losses related to current conduction through a resistive channel and a drift zone in a steady state when the transistor is turned on, and switching power losses connected with the transistor switching transients. This paper focuses on switching power losses in high-speed SiC MOSFET power modules and many challenges in determining them correctly. These challenges are associated with the fact that actual MOSFET transistors in power modules exhibit a significant amount of parasitic capacitances in internal structures and parasitic inductances of connections inside their packages, which significantly affect switching processes.

Transistor switching power losses can be determined based on waveforms of the transistor drain-source voltage and the drain current collected during a double-pulse test. The double-pulse test is a well-known and widely acknowledged method of determining switching power losses in transistors [27–30]. A simplified schematic of the double-pulse test testbench has been shown in Fig. 1. In such a configuration, it is possible to observe the turn-on and turn-off behavior of the device under test (DUT) at nominal current-voltage conditions.

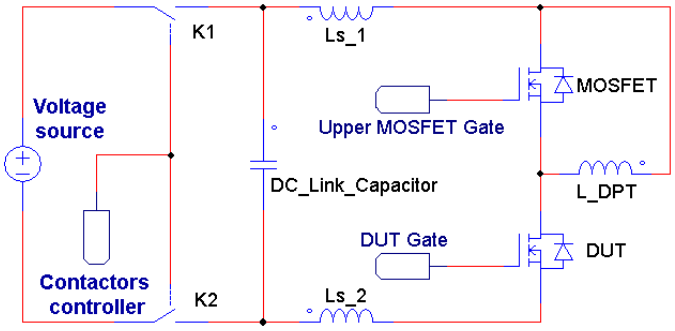

Fig. 1. Simplified schematic of the double-pulse test testbench

3. DOUBLE-PULSE TEST TESTBENCH FOR SIC MOSFET POWER MODULES

Preparation of the double-pulse test circuit for SiC MOSFET power modules to perform commutation tests with currents of hundreds or even thousands of amps is a challenge. A sophisticated design minimizing parasitic inductances in a power loop is required. Without minimizing parasitic inductances in the power loop, the switching speed of the transistors in the circuit may be limited [22, 30]. It is also associated with overvoltages that appear between drain and source of the MOSFET switch, caused by parasitic inductances in the power loop and fast switching processes. For poorly designed power loops with high parasitic inductances, the overvoltages may exceed the breakdown voltage of the SiC MOSFET power module, resulting in an avalanche breakdown and possible permanent damage of the transistor [31–33]. In inadequately designed circuits, to lower overvoltages, a switching process must be slowed down, often by increasing the external gate driver output resistor value. It results in a less steep slope of the transistor falling current during the turn-off process, lowering the voltage induced at parasitic inductances in the power loop, according to equation (2).

$$v_{L_S}(t) = L_S \frac{\mathrm{d}i_D(t)}{\mathrm{d}t}, \tag{2}$$

where:

- $v_{L_S}(t)$ represents the instantaneous voltage induced across the parasitic inductances in the power loop,
- L_S represents the parasitic inductances in the power loop.

Slowing down switching processes increases switching power losses in a MOSFET and is not the best solution. Parasitic inductance in the power loop also affects the resulting switching energies obtained in the double-pulse test. It will positively affect the turn-on process – lowering turn-on switching energy, but at the same time, turn-off switching energy can rise to very high levels, increasing and dominating the sum of turn-on and turn-off energies [30, 34].

A dedicated testbench has been prepared to perform a double-pulse test on selected SiC MOSFET power modules. The Advanced Conversion 700D590 power ring film capacitor has been used as a DC-link capacitor. In order to test various SiC MOSFET power modules assembled in different packages, dedicated busbars have been designed and manufactured to connect DC-link capacitor with SiC MOSFET power modules, keeping parasitic inductances minimized. The one dedicated to Mitsubishi Electric FMF300BX-24A SiC MOSFET power module (1200 V, 300 A) has been shown in Fig. 2.

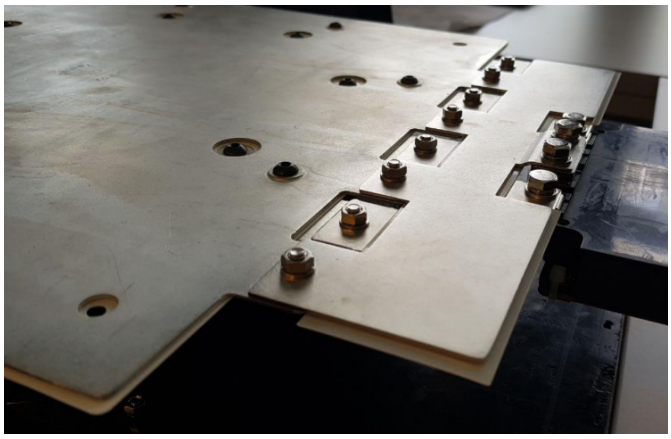

Fig. 2. Busbar connecting low-inductance DC-link capacitor with a SiC MOSFET power module

In order to obtain comparable results of double-pulse tests with different SiC MOSFET power modules, as a gate driver, a modified SiC gate driver unit from MEDCOM company has been used, with 30 amps current capability and 20 ns rise/fall times. A connection between gate driver and SiC MOSFET power modules gate connection terminals has been made using as short as possible high bandwidth coaxial cable to minimize parasitic inductance in the gate loop, as depicted in Fig. 3.

Accurate measurements of voltages and currents for fast switching SiC MOSFETs are challenging. New generation SiC MOSFET power modules are capable of switching load currents in times of the order of tens nanoseconds and are mostly used in high power converters, working with high voltages and high currents. Steep slopes of voltages and currents cause high electromagnetic interferences (EMI) radiation. A high level of EMI may lead to high interferences while performing measurements with oscilloscope probes. In order to minimize interfer-

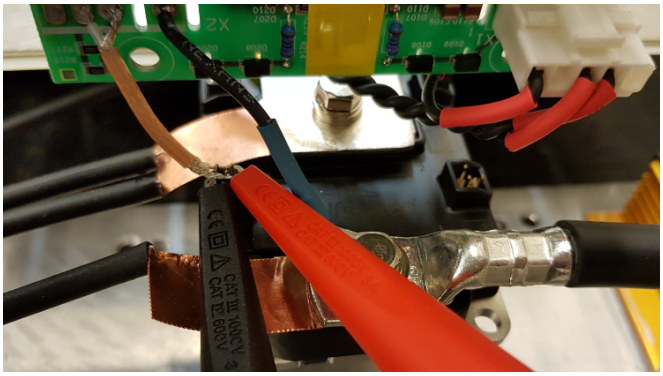

Fig. 3. Coaxial connection of gate driver output with Wolfspeed CAB400M12XM3 SiC MOSFET power module

ences in captured waveforms, a usage of differential probes is preferred. In the prepared testbench, four Tektronix THDP0200 probes have been used to measure voltages on both upper and lower SiC MOSFET in a power module, the gate-source voltage of the lower SiC MOSFET (which is a device under test), and DC-link capacitor voltage (SiC MOSFET power module supply voltage).

Current measurements of fast switching SiC power modules are challenging and involve a trade-off. There are three commonly used methods of measuring fast switching transistors currents [35]:

- a high-bandwidth coaxial shunt resistor,
- a wide-band current transformer,
- a Rogowski coil current probe.

Coaxial shunt resistors offer high bandwidth (up to 2 GHz for Powertek A-5-05) and are suitable for pulse tests with relatively low test currents. However, in the case of SiC MOSFET power modules with test currents often exceeding one thousand amps, using a coaxial shunt resistor can highly limit the versatility of the prepared testbench because of the power dissipation limits in coaxial shunt resistors. Another problem with coaxial shunt resistors is the proper connection with laminated busbars. It is easy to increase the parasitic inductance in the power loop using them. Moreover, coaxial shunts also do not provide galvanic isolation, and their output signal is susceptible to noise due to the low output signal voltage level.

Wide-band current transformers offer high bandwidth (e.g., Pearson 2877 features 200 MHz bandwidth) and galvanic isolation, but their shape and construction make achieving a low parasitic inductance in the switching loop difficult. This disadvantage is caused by the fact that using a current transformer in a power loop forces a dedicated busbar design, limiting the possibility of optimizing the power loop in terms of minimalization of the parasitic inductance. When installed in the circuit, the current transformer increases the resulting parasitic inductance in the power loop meaningfully.

Thus, the most common solution is the Rogowski coil, which features the lowest bandwidth of the three considered types of current probes. However, they provide galvanic isolation, are easy to install in the dedicated circuit, and do not significantly increase the parasitic inductance in the power loop.

Modern, flexible Rogowski coil current probes feature bandwidth up to 50 MHz, which is sufficient for most SiC MOSFET power modules current measurements [36]. For a testbench dedicated to SiC MOSFET power modules, the priority is to keep parasitic inductances in the power loop as low as possible. In order to achieve that, the drain current of the device under test has been measured with a 30 MHz CWT Ultra Mini Rogowski coil current probe. The best-in-class models with the 30 MHz bandwidth or higher and the minimum rise times below 20 ns are suitable for most SiC MOSFET power modules current measurements.

The manufacturer of the used flexible Rogowski coil current probe guarantees full-scale accuracy of $\pm$ 0.2%, however, only if the current conductor is positioned in the center of the Rogowski coil loop. Variations with conductor position inside the coil loop lower the accuracy to $\pm$ 2%. It is a common feature of flexible Rogowski coil current probes, and it should be considered when performing measurements. In order to ensure repeatability and accuracy of current measurements, dedicated 3D-printed plastic coil formers have been manufactured to keep the conductor central in the Rogowski coil loop.

4. PROPER TIME ALIGNMENT OF WAVEFORMS

Experiments show that new generation SiC MOSFET power modules are capable of switching load currents in times of the order of tens of nanoseconds (Fig. 4). Voltage and current probes often exhibit significantly different time delays of their output signals entering an oscilloscope. For SiC MOSFET power modules, not considering these delays most often leads to significant errors in determining switching power losses [26]. To obtain accurate switching power losses, time alignment of voltage and current waveforms is crucial. The literature describes several methods of ensuring correct time alignment of used probes [35]. However, most of them are applicable only for relatively small transistors and low currents of tens of amps or require dedicated calibration tools. In order to achieve proper time alignment, a method based on a voltage drop over parasitic inductance in a power loop during the turn-on process of a SiC MOSFET has been used [37]. A Keysight E5061B vector network analyzer with a prepared SiC MOSFET power module package fixture has been used to extract the parasitic inductance in the power loop. The whole testbench (the DC-link capacitor connected with dedicated busbars) has been measured, resulting in a 16.2 nH of parasitic inductance in the power loop (for a lumped-parameter model, shown in Fig. 5). It should be noted that in the actual circuit, the parasitic inductance is a distributed parameter along also distributed capacitances (including busbars). The effective parasitic inductance in the actual circuit may be lower than the one obtained from the lumped-parameters model [38]. However, the lumped-parameters model is a good reference and a good starting point in further calculations.

With the purpose of achieving proper time alignment of the collected waveforms by voltage and current probes, a voltage drop over effective parasitic inductance has been calculated on the basis of the current waveform. The calculated voltage drop

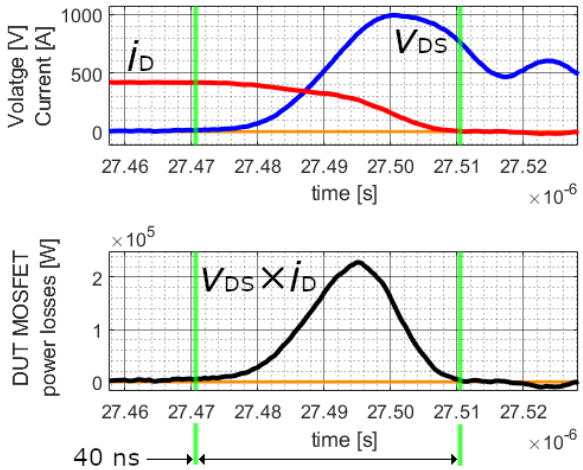

Fig. 4. CAB400M12XM3 turn-off process waveforms of drain-source voltage, drain current, and power losses

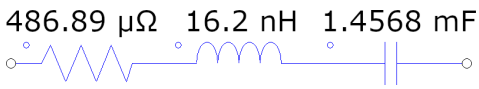

Fig. 5. Lumped-parameters model of the DC-link capacitor connected with dedicated busbars

has been subtracted from the measured voltage across the DC-link capacitor (SiC MOSFET power module supply voltage) before the start of the turn-on process. The outcome waveform Δv_{L_S} has been used as a reference for the time alignment process. In order to achieve proper time alignment, it is necessary to perform a deskew operation (time delay compensation by time-shifting of the waveform) on the obtained waveforms. Precise time alignment is achieved when the obtained waveform of the SiC MOSFET power module supply voltage with the subtracted voltage drop over parasitic inductance matches the actual voltage waveform captured by the voltage probe during the turn-on process, as depicted in Fig. 6.

A good confirmation of the proper time alignment while performing the double-pulse test is also the drain-source voltage

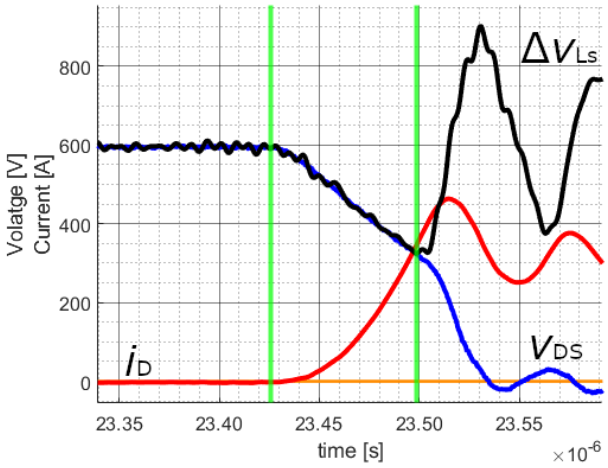

Fig. 6. Proper time alignment of voltage and current waveforms

waveform of the upper transistor in the SiC MOSFET power module (v_{DSTT} in Fig. 7), while the lower switch (DUT) turns on. A proper time alignment results in the matching waveform of the upper transistor drain-source voltage with the previously calculated waveform Δv_{L_S} when voltage oscillations occur, as depicted in Fig. 7.

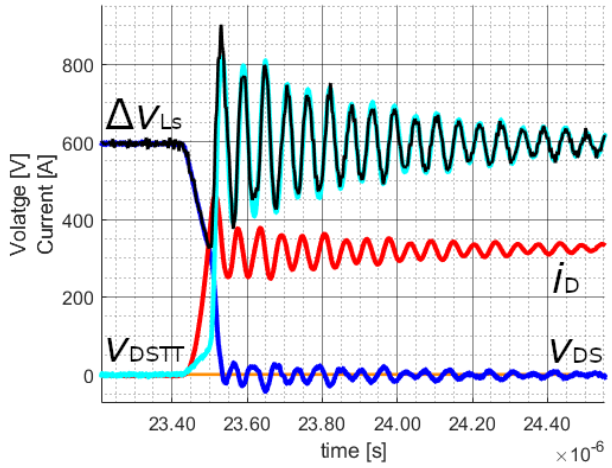

Fig. 7. Comparison of the calculated voltage drop over parasitic inductance waveform (with DC offset) with voltage oscillations measured across upper MOSFET terminals in SiC MOSFET power module under test

5. EXPERIMENTAL VERIFICATION OF THE RELIABILITY OF THE PREPARED TESTBENCH

In order to confirm that the results obtained on the prepared testbench are reliable, a series of double-pulse tests have been performed using SiC MOSFET power modules shown in Fig. 8:

- Mitsubishi Electric FMF300BX-24A (1200 V, 300 A),
- Cree CAS300M12BM2 (1200 V, 300 A),
- Wolfspeed CAB400M12XM3 (1200 V, 400 A).

In addition to the testbench, the gate driver unit has also been adjusted according to the conditions described in the particular power module datasheet to ensure comparable driving conditions. All tests have been performed with the same external gate resistors resistances and gate-source voltages, as described in datasheets.

Fig. 8. Selected SiC MOSFET power modules. From left: Mitsubishi Electric FMF300BX-24A, Wolfspeed CAB400M12XM3, Cree CAS300M12BM2

The resulting switching energies determined using the commonly used method based on the integral of the instantaneous power measured across the transistor during the switching process have been compared with switching energies data provided by manufacturers. Considering obtained results for FMF300BX-24A (Fig. 9) and CAS300M12BM2 (Fig. 10) SiC MOSFET power modules, switching energies are similar to the data provided by the manufacturers. Small differences in the turn-on (E_{ON}) and the turn-off (E_{OFF}) energies may be associated with the variations in power modules parameters resulting from tolerances in production processes or different parasitic inductances in the power loops of testbenches. Another factor responsible for the decrease of the total switching power losses is the gate driver current capability. It is well known that a gate driver with relatively high output resistance increases the effective gate loop resistance, resulting in slower switching processes and higher switching power losses. Unfortunately, the datasheets do not provide any information about used gate drivers in tests performed by the manufacturers.

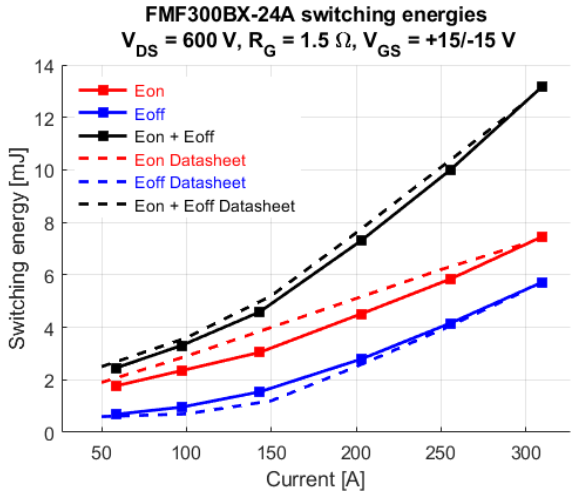

Fig. 9. Mitsubishi Electric FMF300BX-24A SiC MOSFET power module switching energies comparison

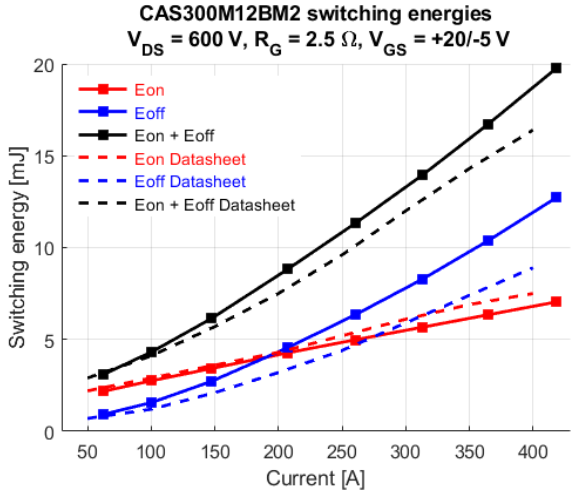

Fig. 10. Cree CAS300M12BM2 SiC MOSFET power module switching energies comparison

In the case of CAB400M12XM3 (Fig. 11) SiC MOSFET power module switching with no additional external gate resistor ($R_{G\_EXT} = 0\ \Omega$), obtained turn-on energy is noticeably

lower than in the datasheet. Taking into account previously described factors that may affect obtained switching energies, in that case, the difference may also be caused by limited bandwidth and not fast enough rise time of used Rogowski coil output signal. A faster current probe might be needed to adequately capture the steeply rising slope of the drain current during the turn-on process in that case. All in all, the trends of the obtained results are similar to the datasheet. Thus, it is assumed that conducted measurements are correct.

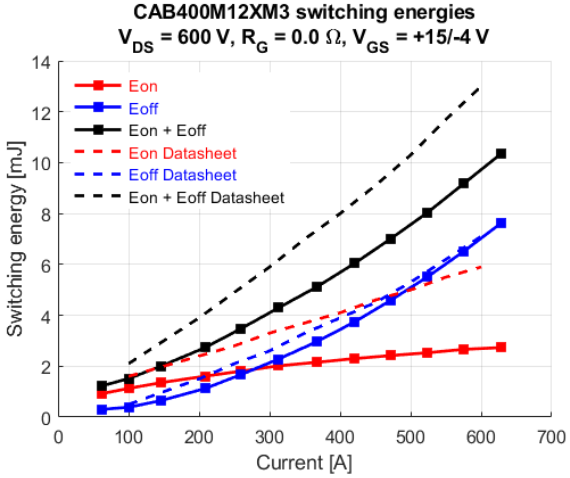

Fig. 11. Wolfspeed CAB400M12XM3 SiC MOSFET power module switching energies comparison

6. THE ISSUE OF PARASITIC CAPACITANCES IN SIC MOSFETS AND THEIR IMPACT ON THE PROPER SWITCHING ENERGIES DETERMINATION PROCESS

6.1. Turn-off process

The transitions from the on-state to the off-state in SiC MOSFETs are so fast that even though their parasitic capacitances are much lower than in their Si equivalents, the high steepness of the drain-source voltage waveform causes a significant capacitive current flow. The problem is that while performing a commutation test like the double-pulse test, the measured drain current includes, in addition to the MOSFET channel current, also a current component that is flowing through nonlinear parasitic capacitances during the charging process. In order to determine the turn-off losses correctly, the parasitic capacitances current component should be removed from the drain current. The current flowing through parasitic capacitances does not flow through the MOSFET channel or drift zone and barely participates in heat generation. Even though the charging process of nonlinear parasitic capacitances is not lossless, the amount of energy dissipated as heat due to current flow through parasitic capacitances is negligible compared to the MOSFET channel losses [25]. All in all, the key to the accurate determination of the switching power losses is the estimation of the instantaneous channel current.

6.2. Turn-on process

Considering the turn-on process of the SiC MOSFET, a drain current measured with a probe during the double-pulse test does not provide complete information about what happens inside the MOSFET. The reason for that is that during the turn-on process, a charged parasitic output capacitance of the MOSFET (a sum of parasitic capacitances between gate-drain and drain-source terminals C_{OSS}) is being discharged through the MOSFET channel [23, 24]. It is not possible to measure that current component with a probe outside the power module. However, as it is a current component flowing through the MOSFET channel, it affects the actual turn-on switching energy. A good estimation of additional energy that should be added to the obtained turn-on switching energy from the double-pulse test is the energy stored in the nonlinear parasitic output capacitance of the MOSFET. That energy can be derived from the characteristic of parasitic output capacitance as a function of drain-source voltage, using equation (3), and equation (4).

$$Q_{OSS} = \int_0^{v_{DS}} C(v_{DS})\,\mathrm{d}v_{DS}\,, \tag{3}$$

where:

- Q_{OSS} represents the charge stored in the parasitic output capacitance of the MOSFET,
- $C(v_{DS})$ represents the value of nonlinear parasitic capacitance in the MOSFET transistor dependent on the drain-source voltage.

$$E_{OSS} = Q_{OSS}V_{DS}\,, \tag{4}$$

where E_{OSS} represents the energy stored in the parasitic output capacitance of the MOSFET at given voltage V_{DS}.

Without considering this effect, the turn-on switching energy determined based on the commonly used equation (1) may be significantly underestimated. It might be exceptionally problematic in power electronics converters, where transistors are working with elevated switching frequencies, as this effect may be a dominant component of switching power losses during converter operation with low load, lowering its efficiency substantially.

7. ESTIMATION OF THE SIC MOSFET CHANNEL CURRENT DURING THE TURN-OFF PROCESS

Yue Xie et al. proposed a method of estimating SiC MOSFET channel current based on the nonlinear transfer characteristic of the device under test [39]. However, in SiC MOSFETs, the gate threshold voltage level changes significantly based on the previous bias of the gate (especially when the negative gate bias is applied), affecting the shape of the transient characteristics [40]. The transfer characteristic also changes significantly with the value of drain-source voltage, a drain-induced barrier lowering (DIBL) effect appearing in SiC MOSFETs due to relatively short channels and even time of the SiC MOSFET transistor being in the on-state or the off-state [41]. Since SiC MOSFET chips sizes are much smaller than their Si equivalents, internal gate resistances have grown significantly. As a result, the gate-source voltage measured during the switching processes at the SiC MOSFET power modules connection points is

far different from the gate-source voltage in the internal structure [27]. Thus it is difficult to estimate the actual instantaneous value of the gate-source voltage precisely. In some cases, the proposed method of estimating SiC MOSFET channel current based on the transfer characteristic may be misleading, resulting in meaningful errors.

With the intention of overcoming these issues, a different approach has been proposed in this paper. As the measured drain current waveform during switching processes consists of the MOSFET channel current component and MOSFET parasitic capacitances current component, separation of the drain current components is possible. Separation of the capacitive current component and subtracting it from the measured drain current waveform results in a waveform representing the MOSFET channel current component. In order to estimate the instantaneous value of capacitive current during the turn-off process, nonlinear capacitance curves provided by manufacturers of SiC MOSFET power modules have been implemented in MATLAB as spline functions. The obtained voltage waveforms from the double-pulse test have been used to calculate currents flowing through the nonlinear parasitic capacitances during the turn-off process based on equation (5).

$$i_C(t) = C(v_C(t))\frac{\mathrm{d}v_C(t)}{\mathrm{d}t}, \tag{5}$$

where:

- $i_C(t)$ represents the instantaneous current flowing through the capacitance.
- $C(v_C(t))$ represents the instantaneous value of nonlinear parasitic capacitance in the MOSFET transistor dependent on the instantaneous voltage across that capacitance.
- $v_C(t)$ represents the instantaneous voltage across the capacitance.

8. EXPERIMENTAL RESULTS OF SIC MOSFET POWER MODULE CHANNEL CURRENT ESTIMATIONS AND SWITCHING ENERGIES OBTAINED USING THE PROPOSED METHODS

Experimental results show that for the fast turn-off processes of Wolfspeed CAB400M12XM3 SiC MOSFET power module switching load current of 415 amps with no additional external gate resistor ($R_{G\_EXT} = 0\ \Omega$), the peak capacitive current component amplitude $i_{C_{OSS}}$ may be as high as 75 amps, as depicted in Fig. 12. That high value of the capacitive current component in the drain current shows that determination of the instantaneous turn-off switching power losses based on the commonly used method (expressed by the equation (1)) may lead to severe overestimation of the SiC MOSFET power module turn-off energy (E_{OFF}). As $i_{C_{OSS}}$ is dependent only on v_{DS}, in the case of the turn-off process at lower load currents, the relation of $i_{C_{OSS}}$ to i_D grows significantly, resulting in an even higher overestimation of the turn-off switching energy, as shown in the Table 1. It can be seen that for SiC MOSFET power module Wolfspeed CAB400M12XM3, error may vary from approximately 8% at 400 amps to over 683% at 50 amps.

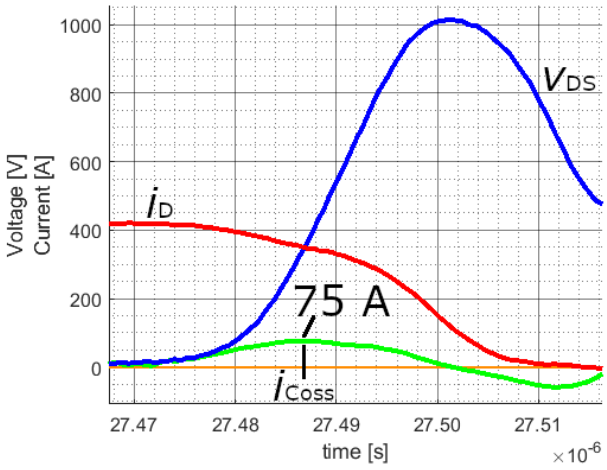

Fig. 12. Capacitive current component $i_{C_{OSS}}$ of the drain current during the fast turn-off process of Wolfspeed CAB400M12XM3 SiC MOSFET power module, switching with no additional external gate resistor ($R_{G\_EXT} = 0\ \Omega$)

Selected experimental results of SiC MOSFET power module channel current estimation (i_{CH}) based on the proposed method has been shown in Fig. 13 (for Mitsubishi Electric FMF300BX-24A), Fig. 14 (for Cree CAS300M12BM2), and Fig. 15 (for Wolfspeed CAB400M12XM3). Similar trends for all modules have been observed.

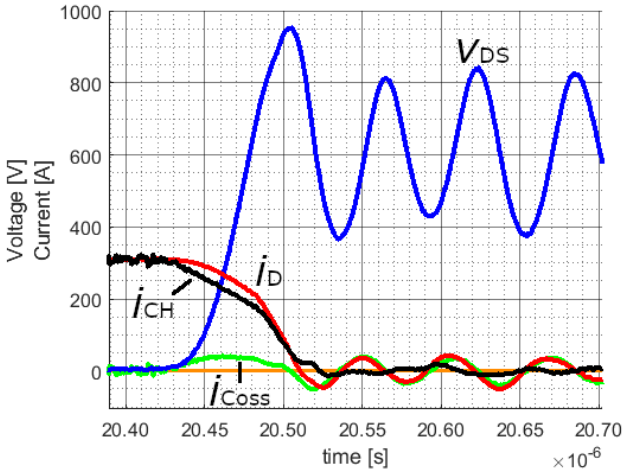

Fig. 13. Channel current i_{CH} estimation of Mitsubishi Electric FMF300BX-24A SiC MOSFET power module during the turn-off process

Following equation (3) and equation (4), energies stored in parasitic output capacitances of three SiC MOSFET power modules under test have been calculated for the selected operating point with the drain-source voltage equal to 600 volts and the drain current equal to 300 amps. The results have been presented in the Table 2. In order to determine the actual turn-on energy for hard-switching conditions, the energy stored in the parasitic output capacitance of the SiC MOSFET power module (E_{OSS}) should be added to the turn-on switching energy deter-

Table 1

Selected experimental results of the turn-off switching energy in Mitsubishi Electric FMF300BX-24A, Cree CAS300M12BM2, and Wolfspeed CAB400M12XM3 SiC MOSFET power modules determined using the commonly used method based on equation (1) marked as E_{OFF}, and comparison with the turn-off switching energy determined using the proposed method, marked as E'_{OFF}

	FMF300BX-24A			CAS300M12BM2			CAB400M12XM3		
i_D [A]	E_{OFF} [mJ]	E'_{OFF} [mJ]	E_{OFF}/E'_{OFF} [%]	E_{OFF} [mJ]	E'_{OFF} [mJ]	E_{OFF}/E'_{OFF} [%]	E_{OFF} [mJ]	E'_{OFF} [mJ]	E_{OFF}/E'_{OFF} [%]
50	0.6832	0.2609	261.86	0.9154	0.2798	327.16	0.3015	0.0385	783.12
100	0.9575	0.5298	180.73	1.5739	0.8651	181.93	0.3903	0.0849	459.72
150	1.5413	1.0622	145.11	2.7231	1.9234	141.58	0.6513	0.2830	230.14
200	2.7939	2.2144	126.17	4.5504	3.6702	123.98	1.1233	0.7083	158.59
250	4.1567	3.4972	118.86	6.3522	5.4024	117.58	1.6707	1.2478	133.89
300	5.7205	5.0118	114.14	8.2959	7.2935	113.90	2.2802	1.8643	122.31
350	–	–	–	10.3825	9.3344	111.23	2.9662	2.6249	113.00
400	–	–	–	12.7303	11.6380	109.39	3.7422	3.4653	107.99

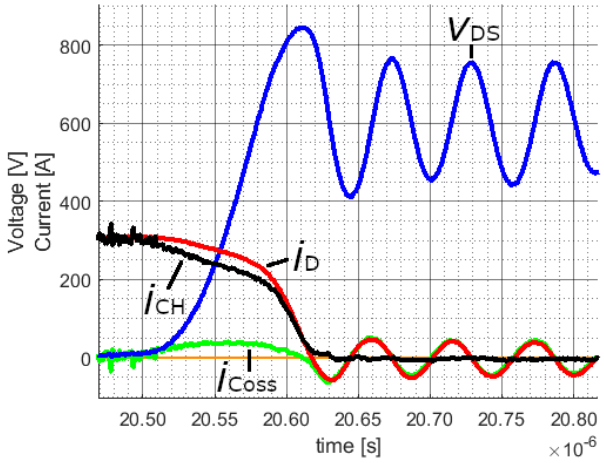

Fig. 14. Channel current i_{CH} estimation of Cree CAS300M12BM2 SiC MOSFET power module during the turn-off process

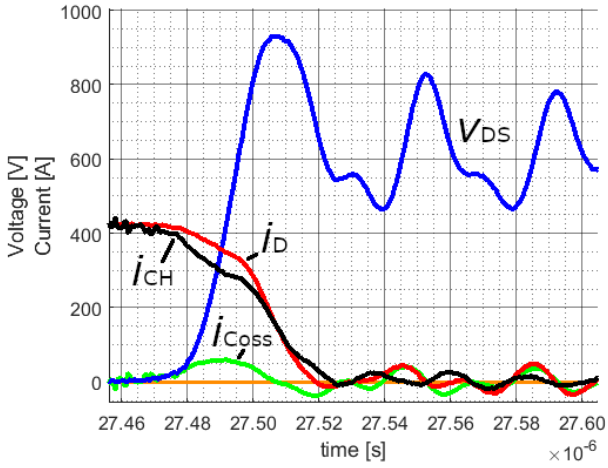

Fig. 15. Channel current i_{CH} estimation of Wolfspeed CAB400M12XM3 SiC MOSFET power module during the turn-off process

Table 2

Selected experimental results of calculated energies stored in parasitic output capacitances of Mitsubishi Electric FMF300BX-24A, Cree CAS300M12BM2, and Wolfspeed CAB400M12XM3 SiC MOSFET power modules (marked as E_{OSS}), and their impact on actual turn-on switching energies ($E_{ON}+E_{OSS}$) in the case of $v_{DS}=600$ volts, $i_D=300$ amps operating point

SiC MOSFET Module Type	E_{OSS} [mJ]	E_{ON} [mJ]	$\frac{E_{ON}+E_{OSS}}{E_{ON}}$ [%]
FMF300BX-24A	1.0139	7.4541	113.60
CAS300M12BM2	1.6004	5.6715	128.22
CAB400M12XM3	0.7014	2.0143	134.82

mined using the commonly used method based on equation (1) (marked as E_{ON} in the Table 2). Obtained results confirm that not considering energy stored in parasitic output capacitance of a SiC MOSFET may lead to a significant underestimation of the turn-on switching energy.

9. CONCLUSIONS

Nowadays, SiC MOSFET power modules are becoming a standard choice in many applications, replacing their slow-switching Si equivalents. However, their fast-switching capabilities come with new challenges in measurements and circuits design. A commonly used method of determining the transistor switching energies based on integrating the product of the instantaneous values of measured drain-source voltage and drain current during the switching process does not consider phenomena that, in the case of fast-switching transistors, have a meaningful impact on the correctness of the obtained results. Phenomena, like the significant capacitive current component in the measured drain current waveform during the turn-off process, or charged parasitic capacitance discharging through the MOSFET channel during the turn-on process have to be consid-

ered, as neglecting them may lead to a meaningful error in the process of determination of switching power losses. Depending on the application, such error may result in an overestimation of switching power losses, resulting in non-optimal power converter design, or underestimation of switching power losses and possible converter overheating or permanent damage. In this article, various problems connected with the correct determination of switching power losses and proposed solutions to overcome these issues in high-speed SiC MOSFET power modules have been described. Moreover, a method of achieving a correct time alignment of waveforms collected by voltage and current oscilloscope probes has been proposed and verified experimentally. A method of estimating SiC MOSFET channel current during the turn-off process based on the estimation of nonlinear parasitic capacitances current has also been provided and verified experimentally. During experiments, it has been found that the capacitive current component peak amplitude during the turn-off process for the Wolfspeed CAB400M12XM3 SiC MOSFET power module (1200 V, 400 A) switching load current of 415 amps can be as high as 75 amps. Usage of the commonly used method of determining transistor switching energies results in an 8% overestimation. However, as the load current decreases, the capacitive current component decreases slightly. This results in approximately 59% turn-off switching energy overestimation in the case of 205 amps load current. The lower the load current, the higher the impact of the capacitive current component in fast-switching transients on resulting overestimation of turn-off switching energy determined based on the commonly used method. For the turn-on process, it has been found that not taking into account the energy stored in the parasitic output capacitance of a SiC MOSFET may lead to a significant underestimation of its turn-on switching energy. In the case of Wolfspeed CAB400M12XM3 SiC MOSFET power module switching load current of 300 amps with the drain-source voltage equal to 600 volts, the turn-on switching energy determined using the commonly used method based on equation (1) is underestimated by close to 35%. It has been found that proposed methods are able to provide a more reliable estimation of the switching power losses as compared to the commonly used method. In future works, it is planned to verify obtained results with the usage of calorimetric methods. As new power electronics semiconductors like SiC MOSFETs dedicated for high power converters are getting increasingly faster, the determination process of switching power losses based on the electrical measurements may be associated with even higher errors due to measurement equipment limitations, especially current probes. A different approach and more advanced techniques for the proper switching power losses determination may be unavoidable and, in the future, further studies will be necessary. Fast current probes like wide-band current transformers or coaxial shunts are available on the market, featuring very high bandwidth, but their dimensions and shapes severely limit the possibility of preparing a circuit with very low parasitic inductance in the power loop. As the incoming new SiC MOSFET power modules are expected to switch even faster, a very low parasitic inductance in the power loop will be even more critical. Since the presence of parasitic inductance is responsible for overvoltages during SiC MOSFET turn-off processes, the full capabilities of these transistors can only be used in properly designed circuits (with the power loop parasitic inductance minimized). The goal of using increasingly faster transistors is to minimize energy consumption by maximizing the efficiency of power electronics converters. Minimizing switching power losses through high-speed switching processes is one of a few ways to achieve it.

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