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A MULTILEVEL SWITCHED |CAPACITOR DC-DC CONVERTER. AN ANALYSIS OF RESONANT OPERATION CONDITIONS*

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Abstract: This paper presents the research results of a multilevel switched capacitor DC-DC converter (MLSCC). The converter, for power electronic applications, can operate in ZCS mode by utilizing resonant circuits for recharging the switched capacitors. The main focus of this article is an in-depth original analysis of the waveforms and the converter voltage ratio. The concept of the converter is verified by simulation results of the circuit in MATLAB/Simulink Sim Power Systems. The formulas given in the mathematical analysis are evaluated for example parameters of the components with the use of numerical approach in MATLAB software. Plot sets are presented in order to judge the influence of the parameters on converter performance. All non-expected relations are explained based on mathematical analysis. The possibilities of the design optimization are identified and presented based on the anticipated results. The present analysis is important for the converter design process and can be used for numerical multi-object optimization to further improve the converter design.

Keywords: *multilevel, DC-DC, switched capacitor, resonant, converter, boost, step-up*

1. INTRODUCTION

Switched capacitor technology is commonly used in chip scale electronic circuits for measurements and supply purposes. Using switched-capacitor topologies in power electronics makes it possible to create a specific class of converters. Advantages of using such converters include less inductive topologies, fast dynamics, small dimensions and fair efficiency. On the other hand, switched capacitor converters usually utilize many more semiconductor switches than conventional switched-mode converters, so they are characterized by having more complicated topology and drivers. The specific energy conversion which uses recharging of capacitors is still a subject of in-

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depth analysis related to the operational condition, selection of parameters or efficiency [1]–[5]. For instance, a detailed analysis for multilevel-modular capacitor-clamped DC-DC converter towards the highest efficiency and the smallest size is presented in [1]. In [2], a selection of components of the switched capacitor voltage multipliers are analyzed. It is very important because the fast increase of recent years' scientific papers where switched capacitor power converters are analyzed in various topological configurations [1]–[16] is observed. Thus, various methods are used for analysis of various topologies and the presented approach for the MLSCC gives original findings.

The multilevel topologies of switched-capacitor converters are also implemented [11]–[14] in power converters as resonant ZCS circuits. In many cases [14], [15], the novel multilevel converters originate from the basic switched capacitor multilevel topology. Thus, an in-depth analysis of the operational conditions, resonant circuits utilization, control and voltage ratios of proposed converters is very important. This paper addresses such an analysis based on a multilevel switched capacitor converter (MLSCC). It focuses on a steady state analysis of oscillation conditions of resonant circuits and the converter's voltage ratio under two types of control. The analysis utilizes a mathematical approach partially supported by numerical methods. A set of figures is presented for arbitrarily selected parameters of the converter. The concepts of the converter topology as well as its driving strategy have been verified by computer simulations.

The analysis and findings are original in the case of the MLSCC circuit proposed. This paper proves that an important impact of resonant circuit parameters on the converter operational conditions as well as novel findings included in obtained models can be very useful in the design process of the converter and control.

2. THE MULTILEVEL SWITCHED CAPACITOR DC-DC CONVERTER: BASIC CONCEPT

Figure 1 presents the basic concept of the MLSCC converter. It is a kind of topology with a series connection of output capacitors. Each output capacitor (C_1–C_4) can be separately charged from the source, incorporating the output tank function and the resonant circuit part.

The output capacitor charging processes occur successively with symmetrical distribution over time (not overlapping themselves), reducing a voltage ripple of the total output voltage. The output voltage ripple can also be minimized by applying an output L_FC_F filter. The converter can operate with a $k_U = 2$ or $k_U = 4$ voltage ratio which is verified by using computer simulation in MATLAB/Simulink Sim Power Systems. The simulation model consists of ideal switches and ideal diodes whichever way

losses are modelled, by cumulated parasitic series resistance. Parameters of these models are listed in Table 1.

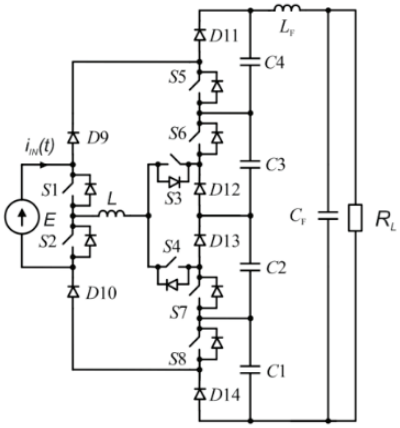

Fig. 1. The basic topology of the MLSCC DC-DC converter in the four-level case

$k_U = 4$ ratio All the output capacitors (C_1–C_4) are sequentially and separately charged. This mode of operation is presented in Fig. 2 and the simulation results are presented in Fig. 4.

$k_U = 2$ ratio The capacitors C_1 and C_2 (or C_3 and C_4) are charged together in a series connection. This mode of operation is clarified by Fig. 3 and the results of simulation of the converter are presented in Fig. 5.

Table 1 Parameters of the simulation model

Parameter		Mode		
		$k_U = 2$	$k_U = 4$	
Switching frequency	f	125	50	kHz
Inductance	L	200		nH
Capacitance of C_1,C_2,C_3,C_4	C	10		µF
Series parasitic resistance	R	45		mΩ
Length of charging interval	T_C	3.5	5	µs
Input voltage	E	30	30	V
Output current of the converter	I_o	3	3	A

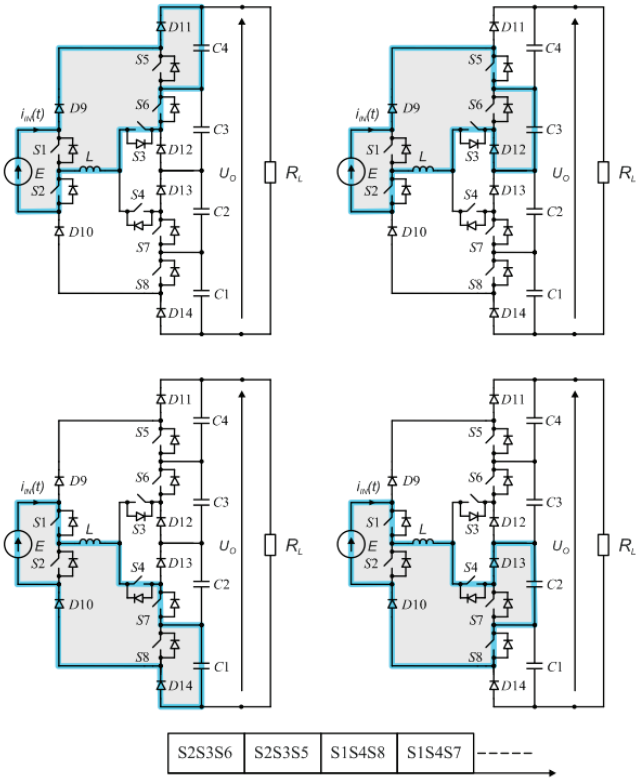

Fig. 2. Principle of operation of the proposed converter for voltage ratio $k_U = 4$

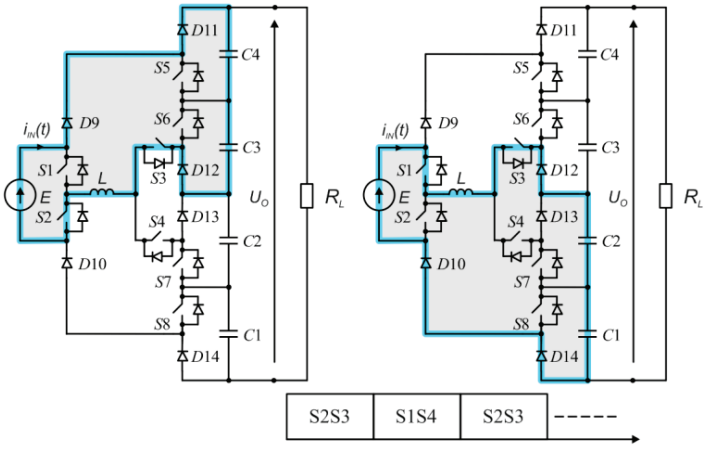

Fig. 3. Principle of operation of the proposed converter for voltage ratio $k_U = 2$

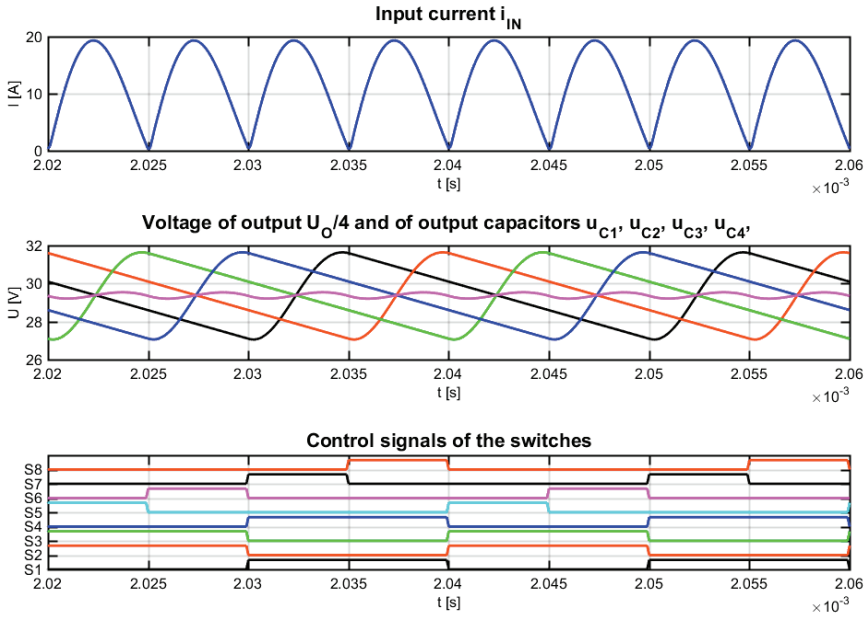

Fig. 4. Simulation result of the MLSCC for mode $k_U = 4$ (MATLAB/Simulink software)

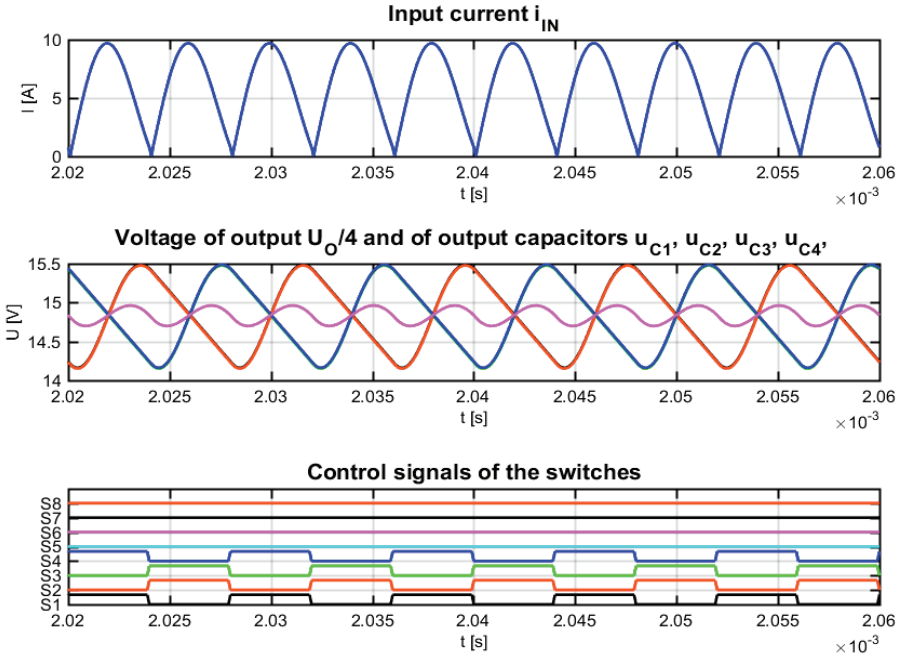

Fig. 5. Simulation result of MLSCC for mode $k_U = 2$ (MATLAB/Simulink software)

3. AN ANALYSIS OF MLSCC OPERATION

3.1. WAVEFORMS IN THE CONVERTER

The following assumptions have been introduced to simplify the analysis: all the output capacitors (C_1–C_4) have equal capacitances; driving signals are symmetrically distributed within the time domain, all output capacitors' charging circuits have equivalent parameters, and all switches operate in the *ZCS* mode (Zero Current Switching). The converter is loaded by the current source with the value of I_0, which represents the real system when the converter is equipped with an output *LC* filter for output voltage ripple minimization (however, within the analysis, the output filter influence is not considered in detail). Under such assumptions, analyzing the converter in a steady state of operation can be limited to only analyzing one of the output capacitors because they do not interact with each other. The other capacitor waveforms are the same as the analyzed ones, but with a time shift. In Fig. 6, the equivalent circuit for analyzing the output capacitor charging is presented. The resistance R represents the sum of all components' parasitic series resistances in the charging path. The parameter L is the inductance of the converter's resonant inductor and the capacitor C represents one of the output capacitors which is being charged. The current source I_0 is the load of the converter. The diode D is an equivalent of the multiple series connected diodes which exist in the charging path considered. Within the following model, forward voltage of the diodes is neglected.

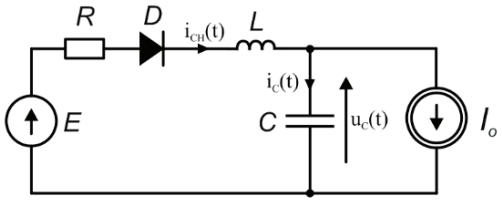

Fig. 6. Equivalent circuit of charging one output capacitor

The model circuit is described by the following set of equations

$$E - Ri_{CH} - L\frac{di_{CH}}{dt} - u_c = 0, \tag{1}$$

$$u_C = \frac{1}{C}\int (i_{CH} - I_0)dt + u_c(0) = -\frac{1}{C}I_0 t + \frac{1}{C}\int i_{CH}dt + u_C(0), \tag{2}$$

where $u_C(0)$ is the initial voltage of a capacitor. In a steady state of operation this value is the same for every cycle of operation and every capacitor. This voltage can also be calculated according to further derived equation (20), i_{CH} is the current of charging the output capacitor and u_C is the voltage across the output capacitor.

Using (2) in (1) gives

$$E - u_C(0) + \frac{1}{C} I_0 t - R i_{CH} - L \frac{di_{CH}}{dt} - \frac{1}{C} \int i_{CH} dt = 0. \tag{3}$$

Thus

$$I_{CH} \left[R + sL + \frac{1}{sC} \right] = L i_{CH}(0) + \frac{1}{s} [E - u_C(0)] + \frac{1}{s^2 C} I_0, \tag{4}$$

$$I_{CH} = \frac{s C i_{CH}(0) + \frac{1}{L} [E - u_C(0)] + \frac{1}{sLC} I_0}{s^2 + s \frac{R}{L} + \frac{1}{LC}}. \tag{5}$$

For the initial current $i_{CH}(0) = 0$

$$I_{CH} = \frac{\frac{1}{L} [E - u_C(0)] + \frac{1}{LCs} I_0}{s^2 + s \frac{R}{L} + \frac{1}{LC}}. \tag{6}$$

The time-domain solution of (3) can be found after the following conversions

$$I_{CH} = \frac{\left(E - u_C(0) - \frac{1}{2} I_0 R \right)}{L \omega_0} \frac{\omega_0}{(s+\alpha)^2 + \omega_0^2} - I_0 \left(\frac{s - \alpha}{(s+\alpha)^2 + \omega_0^2} + \frac{1}{s} \right) \tag{7}$$

where

$$\alpha = \frac{R}{2L}, \quad \omega_0 = \sqrt{\omega^2 - \alpha^2}, \quad \omega = \frac{1}{\sqrt{LC}}, \quad R < 2\sqrt{\frac{L}{C}}. \tag{8}$$

The inverse Laplace transform of (7) yields

$$i_{CH} = \frac{E - u_C(0) - \frac{1}{2} I_0 R}{L \omega_0} e^{-\alpha t} \sin(\omega_0 t) + I_0 [1 - e^{-\alpha t} \cos(\omega_0 t)]. \tag{9}$$

Finally, introducing the time offset t_0 to function (9), the charging current i_{CH} during the oscillation time period (between t_0 and t_3 in Fig. 7) is described by the following formula

$$i_{CH} = \mathrm{e}^{-\alpha(t-t_0)} \sqrt{\left(\frac{E - u_{C0} - \frac{1}{2} I_0 R}{L\omega_0} \right)^2} + I_0^2 \sin(\omega_0 t - \varphi - \omega_0 t_0) + I_0 \tag{10}$$

where $\varphi = \operatorname{arctg} \dfrac{I_0 L \omega_0}{E - U_{C(0)} - \dfrac{1}{2} I_0 R}$, $U_{C0} = u_C(t_0)$.

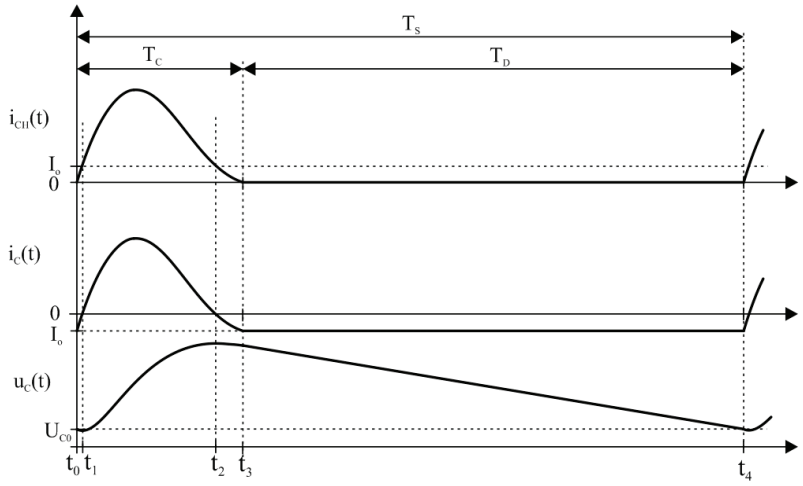

Fig. 7. The idealized waveforms for one output capacitor, related to equivalent circuit

When the capacitors are charged separately the charging process is not affected by one another. In a more detailed model the output voltage ripple can be taken into consideration, which can affect the current in resistive load. However, in a suitably designed converter the consideration of current ripples in the analytical model does not change the analysis significantly. Especially, when the output LC filter is used that reduces ripples of the output current. In the discharging interval T_D (between t_3 and t_4 in Fig. 7), the charging current i_{CH} equals zero because the serial diodes (represented by diode D in Fig. 6) or opened switches (Fig. 2) block negative current flow. The converter input current i_{IN} equals the current i_{CH}, which is calculated for the equivalent circuit, only in the charging interval Tc. Obviously, the additional current pulses occur within i_{IN} due to charging other output capacitors (which are not considered as part of the equivalent circuit for simplification of the analysis). To calculate i_{IN} for a specific time t, the adequate time shift should be put in relation to t_0. The capacitor current (i_C) in the charging interval T_C is given as

$$i_C = \mathrm{e}^{-\alpha(t-t_0)} \sqrt{\left(\frac{E - U_{C0} - \frac{1}{2} I_0 R}{L\omega_0} \right)^2 + I_0^2} \sin(\omega_0 t - \varphi - \omega_0 t_0). \tag{11}$$

During the time interval T_D $i_C = -I_0$.

Voltage across the capacitor C during the interval T_C can be calculated as follows

$$u_C = \frac{1}{C} \int i_C(t) dt + \mathrm{Const}, \tag{12}$$

$$u_C = -\frac{1}{c\omega} \sqrt{\left(\frac{E - U_{C0} - \frac{1}{2} I_0 R}{L\omega_0} \right)^2 + I_0^2} [\mathrm{e}^{-\alpha(t-t_0)} \cos(\omega_0 t - \varphi - \omega_0 t_0) - \cos(\gamma + \varphi)] + U_{C0}, \tag{13}$$

where $\gamma = \mathrm{arctg} \frac{\alpha}{\omega_0}$.

During the discharging interval (t_3 to t_4) voltage across the capacitor linearly decreases

$$u_C = u_C(t_3) - \frac{I_0}{C(t - t_3)}. \tag{14}$$

Figure 7 presents the draft of waveforms that corresponds to the relations between (10) and (14). The waveforms can be divided into the following intervals (a numerical solution of the model is presented in Fig. 8 for physical data):

- t_0–t_1 – The start of the oscillation, in which current in the inductor L is rising but is still smaller than the load current I_O, thus the capacitor is still being discharged. At t_1, the capacitor voltage is at its lowest.
- t_1–t_2 – The main charging oscillation, in which the capacitor voltage is rising and at t_2 it is at its highest.
- t_2–t_3 – The inductor current is lower than I_o; thus, the capacitor is partially discharging. At t_3, oscillation is finished and the inductor current is zero.

At time t_1 the capacitor voltage value is at its lowest and at t_2 it is at its highest. Thus, the voltage ripple value is given as

$$\Delta u_C = -\frac{1}{C\omega}\sqrt{\left(\frac{E - U_{C0} - \frac{1}{2}I_0 R}{L\omega_0}\right)^2 + I_0^2}\,[\mathrm{e}^{-\alpha(t-t_0)}\cos(\omega_0 t_1 - \omega_0 t_0 - \varphi - \gamma)$$

$$-\mathrm{e}^{-\alpha(t-t_0)}\cos(\omega_0 t_2 - \omega_0 t_0 - \varphi - \gamma - \omega_0 t_0)] \tag{15}$$

where $t_1 = \dfrac{\varphi}{\omega_0} + t_0, \quad t_2 = t_1 + \dfrac{\pi}{\omega_0}.$

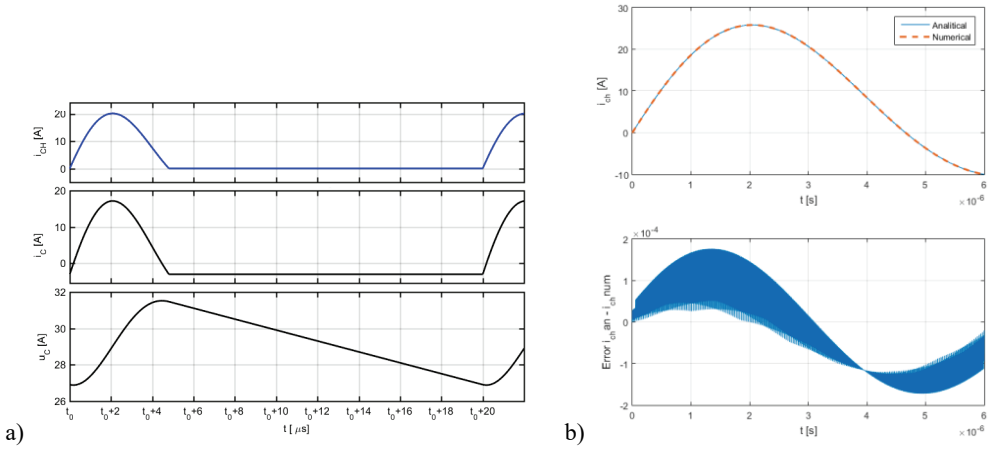

Fig. 8. The analyzed waveforms gained by simulation of the circuit of the converter with parameters according to Table 2. (a) Results of simulation of the converter in steady state with ideal switches and diodes, (b) numerical solution of equation (1) and evaluation of equation (9) (arbitrary U_{c0} = 26 V), (MATLAB/Simulink software)

It is important, for the driving controller design process, to determine the length of the interval T_C, because nearly after $t = T_C$, the next capacitor must be charged. To determine the T_C, only the t_3 has to be found by solving the following equation

$$i_{CH}(t) = 0, \quad t \in \left(t_0; \frac{2\pi + \varphi}{\omega_0} + t_0\right), \tag{16}$$

$$\mathrm{e}^{-\alpha(t-t_0)}\sqrt{\left(\frac{E - U_{C0} - \frac{1}{2}IoR}{L\omega_0}\right)^2 + I_0^2}\,\sin(\omega_0 t - \varphi - \omega_0 t_0) + Io = 0. \tag{17}$$

Equation (17) has the form $e^{-\alpha t}\sin(\omega t)$ = const which cannot be solved in an analytical approach for t when const $\neq 0$. However, for the first approximation, equation (17) can be solved assuming $R = 0$

$$t_3 = \frac{1}{\omega}\left[\pi + 2\arcsin\left(\frac{I_0}{\sqrt{\left(\frac{E - U_{C0}}{Z_F}\right)^2 + Io^2}}\right)\right] + t_0 \tag{18}$$

where $Z_F = \sqrt{\frac{L}{C}}$.

To achieve the result being closer to the real value, the angular frequency ω in (18) can be replaced by ω_0 which is an angular frequency for a dissipative circuit. The arcsin function in (18) can be approximated by a linear function which greatly simplifies the equation, and that is important for further analytical calculations. The error of this approximation for a real design range of the parameters is strongly dominated by the $R = 0$ assumption error. The relation is obtained by introducing these notes into (18)

$$t_3 \approx \frac{1}{\omega}\left[\pi + 2\left(\frac{I_0}{\sqrt{\left(\frac{E - U_{C0}}{Z_F}\right)^2 + Io^2}}\right)\right] + t_0. \tag{19}$$

The voltage U_{c0} is necessary for all given relations. In a steady state of operation, it can be calculated according to the following equation

$$\int_0^{t_4} i_C(t, U_{C0})dt = 0. \tag{20}$$

Formula (20) cannot be solved for a dissipative circuit by using an analytical approach, due to the unknown precise value of t_3 which is necessary for integration in (20). Calculating with the $R = 0$ assumption gives inexact results. The accurate values of t_3 and U_{C0} should be calculated numerically by solving equations (16) and (20), respectively.

3.2. VOLTAGE GAIN OF THE CONVERTER

In the equivalent circuit (Fig. 6), during interval T_C, the diode D is forward biased. Neglecting the forward voltage drop, Kirchhoff's equation for interval T_C can be written as

$$E + u_L + u_R = u_c. \tag{21}$$

Averaging both sides of equation (21) within interval T_C, the following relation is obtained

$$\mathrm{E} - \frac{1}{T_C}\int_{t_0}^{t_3} \mathrm{u}_L dt - \frac{1}{T_C}\int_{t_0}^{t_3} \mathrm{u}_R dt = \frac{1}{T_C}\int_{t_0}^{t_3} \mathrm{u}_c dt \tag{22}$$

where $T_C = t_3 - t_0$.

The instantaneous value of the inductor current at t_0 is the same as at t_3 (it equals zero), which means that the average voltage across the inductor during interval T_C equals zero

$$\frac{1}{T_C}\int_{t_0}^{t_3} \mathrm{u}_L dt = 0. \tag{23}$$

Since resistance R is assumed to be zero, equation (22) is simplified

$$\mathrm{E} = \frac{1}{T_C}\int_{t_0}^{t_3} \mathrm{u}_c(t) dt\ . \tag{24}$$

The waveform of capacitor voltage within the interval T_C becomes symmetric, which makes the following relations true

$$t_1 - t_0 = t_3 - t_2, \tag{25}$$

$$u_C(t_1) = u_C(t_2), u_C(t_0) = u_C(t_3), \tag{26}$$

$$\frac{1}{T_C}\int_{t_0}^{t_3} \mathrm{u}_c(t) dt = \frac{1}{T_D}\int_{t_3}^{t_4} \mathrm{u}_c(t) dt = \frac{1}{T_s}\int_{t_0}^{t_4} \mathrm{u}_c(t) dt = U_C, \tag{27}$$

where

$T_S = t_4 – t_0$ – the period of switching,

$T_D = t_4 – t_3$ – the discharging interval time length.

In a steady state, relations (24) and (27) are applicable for any of the converter output capacitors. Thus, the ideal converter voltage gain can be calculated as

$$U_0 = \sum_{n=1}^{n=N} U_{C_n}, \tag{28}$$

$$U_0 = NE, \tag{29}$$

$$k_u = \frac{U_0}{E} = N, \tag{30}$$

where N – the number of output capacitors are charged individually (for presented converter $N = 4$ or $N = 2$, depending upon control).

For the real converter, the assumption of $R = 0$ creates too strong a simplification to be ignored (in the majority of cases). Due to the relatively high number of the series conducting switches in the topology presented, assessing the converter's real voltage gain is essential for the design process including the selection of components. Relation (21) is also true for the case with nonzero resistance but the average voltage drop on the series resistance has to be calculated to complete (22)

$$\frac{1}{T_C}\int_{t_0}^{t_3} \mathrm{u}_{R_{(t)}}\, dt = \frac{R}{T_C}\int_{t_0}^{t_3} \mathrm{i}_{CH_{(t)}}\, dt. \tag{31}$$

For the converter operation to be in a steady state, the following relation between currents can be written

$$\frac{1}{T_C}\int_{t_0}^{t_3} \mathrm{i}_{CH_{(t)}}\, dt = I_o \frac{T_s}{T_C}, \tag{32}$$

$$\frac{1}{T_C}\int_{t_0}^{t_3} \mathrm{u}_c(t) dt = E - RI_o \frac{T_s}{T_C}. \tag{33}$$

Calculating the converter voltage gain while taking into account the parasitic series resistances is complicated, because in this case relations (25)–(27) are no longer true. Thus, the average voltage across the capacitor in the interval T_D (t_3 to t_4) has to be calculated

$$\frac{1}{T_D}\int_{t_3}^{t_4} \mathrm{u}_c(t) dt = \frac{\mathrm{u}_c(t_3) + \mathrm{u}_c(t_4)}{2}. \tag{34}$$

In a steady state of operation, the voltage value across the capacitor at time t_4 is the same as at t_0 and equals U_{C0}. Therefore, the capacitor's average voltage in the switching period T_S can be expressed as

$$U_C = \frac{1}{T_S}\int_{t_0}^{t_4} \mathrm{u}_c(t)dt = \frac{T_C}{T_S}\mathrm{E} - \mathrm{R}I_o + \frac{T_D}{T_S}\frac{\mathrm{u}_c(t_3) + U_{C0}}{2}. \tag{35}$$

The converter's output voltage is given as

$$U_0 = NU_C = \mathrm{N}\left[\frac{T_C}{T_S}\mathrm{E} - \mathrm{R}I_o + \frac{T_D}{T_S}\frac{\mathrm{u}_c(t_3) + U_{C0}}{2}\right]. \tag{36}$$

3.3. ANALYSIS OF THE GAINED RELATIONS

Equations gained in Sections 3.1 and 3.2 are complicated for the clear analytical estimation of the influence of different parameters on converter performance. To improve the analysis, based on the analytical formulas presented, sets of curves are plotted and presented in Figs. 9–11 according to the parameters which are given in Table 2. The time instant t_3 and voltage Uc_0 have been calculated numerically using the relationship between (16) and (20). The diodes' voltage drop was neglected. In Fig. 9, the influence of capacitance is presented. In calculations, the Ts and T_C were kept constant by adjusting the value of L. The output capacitance variation has almost no effect on the converter's average output voltage; however, there is a strong dependence of the output voltage ripple on C. The output voltage ripple should be minimized by using a bigger C value. In the figures presented, the damping of the output filter is not considered. The larger the C is, the lower the peak energy stored in inductor L will be, which is desirable (but for large C).

Table 2. Parameters for numerical analysis of analytical equations (if not otherwise stated in the plot)

Parameter		Value	
Number of voltage levels	N	4	–
Switching frequency	f	50	kHz
Inductance	L	180	nH
Output capacitors capacitance	C	10	μF
Series resistance	R	45	mΩ
Time length of charging interval	T_c	4.76	μs
Input voltage	U	30	V
Output current	I_o	3	A

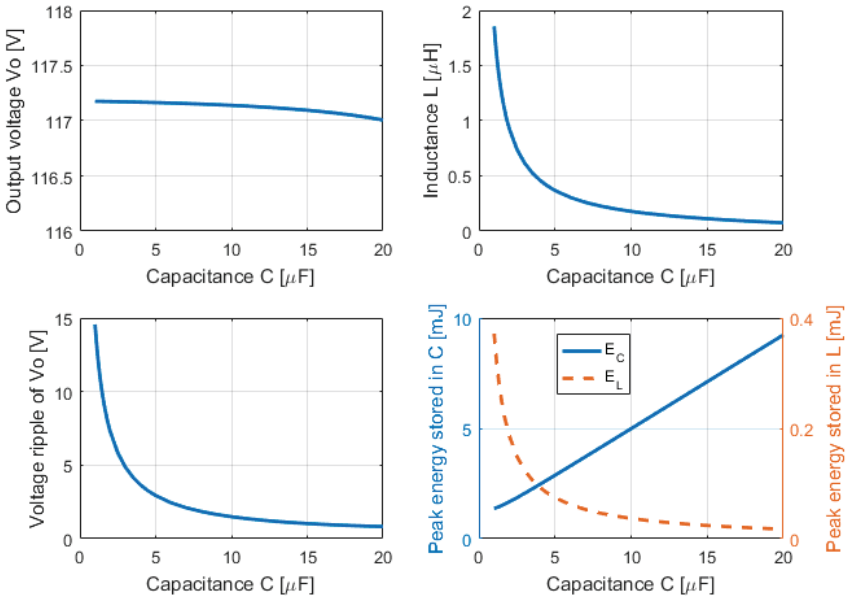

Fig. 9. Influence of the capacitance *C* on parameters of the converter.
All parameters listed in Table 2 are constant excluding capacitance *C* and inductance *L*

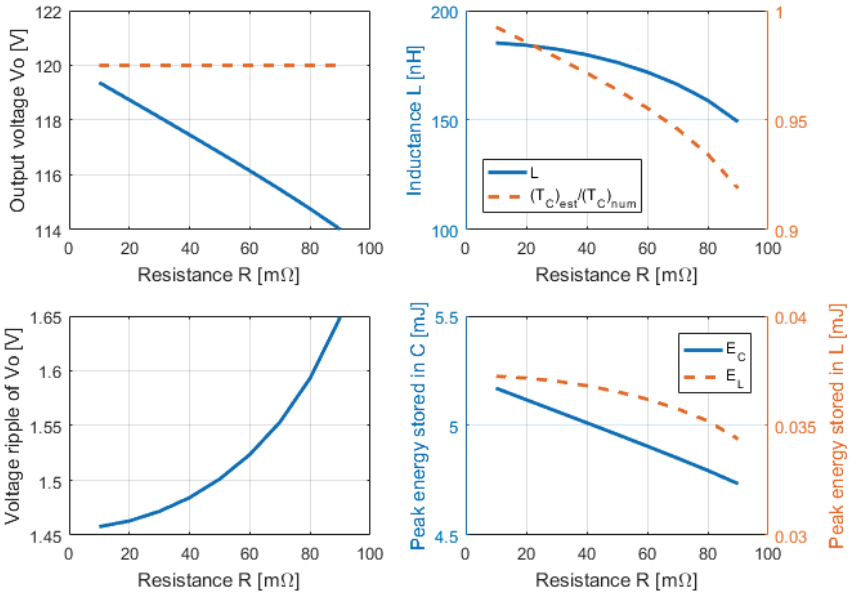

Fig. 10. Influence of resistance *R* on parameters of the converter.
All parameters listed in Table 2 are constant excluding resistance *R* and inductance *L*

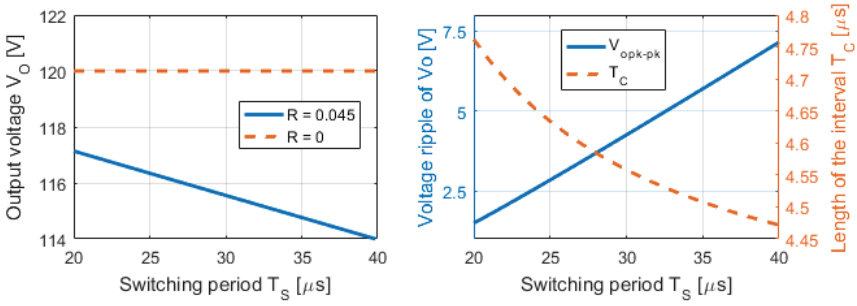

Fig. 11. Influence of the switching period T_S on parameters of the converter.
All parameters listed in Table 2 are constant excluding switching frequency and T_c

But this dependence weakens within a large C, and further increasing of C may be purposeless. However, limiting the peak energy stored in the inductor means limiting the magnetic component size, which is the right way for the switched capacitor converters. If the energy and inductance of the inductor L is minimized enough, the air core design may be used with fair effect. The value of C = 10 μF has been chosen as a trade-off between minimization of the magnetic component as well as the output voltage ripple and size of output capacitors. In Fig. 10, the influence of parasitic series' resistance is presented. For the present analysis, a constant length Tc is obtained for a different value of R by correcting the inductance L. The parasitic series resistance consists mainly of resistance of the inductor L and the resistance of conducting switches and diodes. The resistance has a negative influence on the converter performance and should thus be minimized. For the assumed parameters of the converter (Table 2), the parasitic resistance R = 45 mΩ seems to be achievable by using the modern MOSFET switches and diodes. The parasitic series resistance decreases the converter voltage gain, which is strongly undesirable since the switched capacitor converters have constant voltage gain with no easy way to control and maintain it. This is proved analytically by equation (36) where it can be seen that resistance R affects the converter's output voltage by means of increasing the converter's equivalent output series resistance. The parasitic series resistance increases the output voltage ripple and has almost no influence on the peak energy stored in the inductor and capacitors. In Fig. 10, the curve showing the ratio T_C is also plotted, estimated by using (19) to more accurately define T_C, calculated numerically according to (16). The estimated value has a negative error that arises with parasitic resistance (in other words, with damping the resonant circuit factor).

In Fig. 11, the influence of switching period T_S on converter performance is presented. The switching period should be minimized with a specific lower boundary to ensure the zero current switching of transistors. The topology is quite complicated; therefore, it needs a considerable area and long connections, which are

important for practical implementation. This is a drawback, especially for minimizing the parasitic inductances that may cause unwanted ringing in the case of overlaps of the charging processes (hard switching). The longer the switching period is, the higher the output equivalent series resistance of the converter is, as well as the converter's higher output voltage ripple. In Fig. 11, the dependence of the T_C against switching period T_S is plotted. This relation is relatively weak but can be unexpected. This phenomenon is proved analytically by equation (19). If the switching interval is longer, the ripple voltage across the capacitor C is higher, which means that U_{C0} is lower, the denominator of (19) is larger and thus t_3 is lower (shorter T_C).

4. CONCLUSIONS

The main focus of this article was the mathematical analysis of multilevel switched capacitor DC-DC converters' topology under a steady state operation. The impact of particular parameters of resonant circuits, including series parasitic resistance, on the operational features of the converter is very important for the design. The analytical solutions to obtain clear relationships can be very complicated; thus the original assumptions have been proposed to simplify the analysis. The important influence of the parasitic resistance on the converter operation is identified and a mathematical model taking the resistance into account is presented. Due to the limitations of mathematical modeling, the numerical approach is proposed for solving a few of the given equations.

The obtained relations are evaluated with the example parameters of the converter and a set of curves is plotted for further reference. Based on the plots, the influence of different parameters on performance of the converter is analyzed. The unexpected dependence of the charging interval T_C on the switching period T_S has been discovered and explained, based on a prepared analytical model. The possible optimization of output capacitors and an input inductor has been identified and discussed. The conclusions derived allow for a careful design of the MLSCC converter regarding component selection. The present analysis can be used for numerical multi-object optimization to further improve the converter design. The concept of topology and drive has been proven by simulation in MATLAB/Simulink software.

FUTURE WORKS

In the further research, experimental tests will be performed to verify the analytical model and achieve other results such as those referring to efficiency. The model prepared for this purpose is presented in Fig. 12. A work on the efficiency of the converter versus operational parameters is also very important.

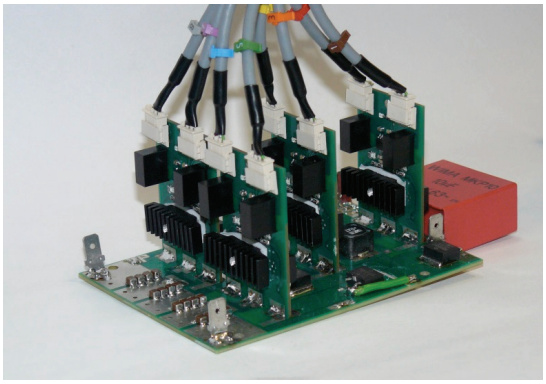

Fig. 12. The experimental setup of the MLSCC

REFERENCES

[1] CAO D., JIANG S., PENG F.Z., *Optimal Design of a Multilevel Modular Capacitor-Clamped DC-DC Converter*, IEEE Transactions on Power Electronics, 2013, 28, 8, 3816–3826.

[2] WARADZYN Z., STALA R., MONDZIK A., PIROG S., *Switched Capacitor-Based Power Electronic Converter – Optimization of High Frequency Resonant Circuit Components*, in *Advanced Control of Electrical Drives and Power Electronic Converters*, ser. Studies in Systems, Decision and Control. Gewerbestrasse 11, 6330 Cham, Switzerland: Springer International Publishing AG, 2017, 361–378.

[3] LEI Y., PILAWA-PODGURSKI R.C.N., *A general method for analyzing resonant and soft-charging operation of switched-capacitor converters*, IEEE Trans. Power Electron., 2015, 30, 10, 5650–5664, DOI: 10.1109/TPEL.2014.2377738.

[4] XIONG S., WONG S.C., TAN S.C., TSE C.K., *Optimal Design of Complex Switched-Capacitor Converters Via Energy-Flow-Path Analysis*, IEEE Transactions on Power Electronics, 2017, 32, 2, 1170–1185.

[5] CAO D., PENG F.Z., *Zero-current-switching multilevel modular switched-capacitor DC-DC converter*, IEEE Trans. Ind. Appl., 2010, 46, 6, 2536–2544, DOI 10.1109/TIA.2010.2073432.

[6] YEUNG Y.P.B., CHENG K.W.E., HO S.L., LAW K.K., SUTANTO D., *Unified analysis of switched-capacitor resonant converters*, IEEE Transactions on Industrial Electronics, 2004, 51, 4, 864–873.

[7] SHEN M., PENG F.Z., TOLBERT L.M., *Multilevel DC-DC Power Conversion System With Multiple DC Sources*, IEEE Transactions on Power Electronics, 2008, 23, 420–426.

[8] PENG F.Z., ZHANG F., QIAN Z., *A magnetic-less DC-DC converter for dual-voltage automotive systems*, Industry Applications, IEEE Transactions on, 2003, 39, 511–518.

[9] KAWA A., STALA R., MONDZIK A., PIROG S., PENCZEK A., *High Power Thyristor-Based DC-DC Switched-Capacitor Voltage Multipliers. Basic Concept And Novel Derived Topology with A Reduced Number of Switches*, IEEE Transactions on Power Electronics, 2016, 31, 10, 6797–6813.

[10] MONDZIK A., WARADZYN Z., STALA R., PENCZEK A., *High efficiency switched capacitor voltage doubler with planar core-based resonant choke*, 2016 10th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Bydgoszcz, 2016, 402–409.

[11] KEISER O., STEIMER P.K., KOLAR J.W., *High power resonant Switched-Capacitor step-down converter*, Power Electronics Specialists Conference, PESC 2008. IEEE, 2008, 2772, 2777.

[12] MONDZIK A., KAWA A., PIRÓG S., PENCZEK A., STALA R., *The Optimization of the Shape of Input Current in Thyristor Based Boost Switched Capacitor Converter with Sequence Charging, Studies*

and Research, Problems Concerning Electric Machines, Drives and Measurements, 35, Wrocław, Poland, 2015.

[13] BABAEI E., SHEERMOHAMMADZADEH GOWGANI S., *Hybrid Multilevel Inverter Using Switched-Capacitor Units*, IEEE Transactions on Industrial Electronics, PP, 99, 1,1.

[14] LIU J., CHENG K., YE Y., *A Cascaded Multilevel Inverter Based on Switched-Capacitor for High Frequency AC Power Distribution System*, IEEE Transactions on Power Electronics, PP, 99, 1,1.

[15] CERVERA A., EVZELMAN M., PERETZ M.M., BEN-YAAKOV S.S., *A high efficiency resonant switched capacitor converter with continuous conversion ratio*, Energy Conversion Congress and Exposition (ECCE), IEEE, 2013, 4969–4976.

[16] WU B., LI S., MA SMEDLEY K., SINGER S., *A Family of Two-Switch Boosting Switched-Capacitor Converters*, IEEE Transactions on Power Electronics, 2015, 30, 10, 5413–5424.

[17] SANO K., FUJITA H., *Voltage-Balancing Circuit Based on a Resonant Switched-Capacitor Converter for Multilevel Inverters*, IEEE Transactions on Industry Applications, 2008, 44, 6, 1768–1776.

[18] CAO D., PENG F.Z., *Multiphase Multilevel Modular DC–DC Converter for High-Current High-Gain TEG Application*, IEEE Transactions on Industry Applications, 2011, 47, 3, 1400–1408.

[19] GITAU M., KALA-KONGA C.L., *Compact energy efficient switched-capacitor multilevel DC-DC converters for interfacing DC-buses with common ground*, 2011 IEEE International Symposium on Industrial Electronics, Gdańsk, 2011, 1845–1850.

[20] PENG F.Z., CAO D., *A family of zero current switching switched-capacitor DC-DC converters*, Applied Power Electronics Conference and Exposition (APEC), Twenty-Fifth Annual IEEE, 2010, 1365–1372.

[21] PENG F.Z., *A generalized multilevel inverter topology with self voltage balancing*, IEEE Transactions on Industry Applications, 2001, 37, 2, 611,618.