"INTERACTIVE POWER DEVICES FOR EFFICIENCY IN AUTOMOTIVE WITH INCREASED RELIABILITY AND SAFETY" – THE EUROPEAN PROJECT CONCERNING THE MAIN AUTOMOTIVE AND TRANSPORT APPLICATION DOMAINS

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Summary

The overall objective of the IDEAS project is to develop advanced packaging for power supply components and new generation memory systems applicable to Electric and ICE propelled vehicles, with paying attention to considering also the aspects that have not been addressed yet in the running ENIAC and ARTEMIS Automotive projects. A major challenge related to electronic devices in the automotive applications is the reliability of power supply systems which must be capable to assure the functionality of subsystems in all operating conditions, inclusive of ageing. The control systems, which rely on multi-core microcontrollers and complex software architectures, require increasingly stringent constraints from the memory devices which need to be designed for very high bandwidth, speed and reliability. In the following thesis, a few aspects of the IDEAS project will be presented: a review of important factors that affect the reliability and life-cycle endurance of NAND flash memories, multispeed gear application in electric drives and its influence on the energy efficiency. The problem of electromagnetic compatibility of electronic devices will also be dealt with in the paper.

Key words: Electric vehicle, NAND flash memory, reliability, EV powertrain, electric drive efficiency

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1. Main factors influencing the reliability of the NAND flash memory

The flash memory has been an important driving force due to the increasing popularity of mobile devices with large storage requirements. The flash memory is considered in many applications as a storage medium due to its high access speed, non-volatile type of storage (Fig. 1), and low-power consumption. There is a wide range of non-volatile memories, and they all offer various characteristics based on the complexity of array organization and structure of the selected cell type [27].

Flash memories are becoming widely deployed in many applications such as solid state drives (SSDs) for embedded controllers and traditional computing storage. NAND flash memories are becoming more and more popular due to their usage as Solid-State Drives (SSDs) [1] and USB Flash drives which are in general called flash storage devices.

Another area of application is the non-volatile memory in the systems that allow system reconfiguration, software updates, changing of stored identification codes, or frequent updating of stored information (i.e. smart cards). Electrically erasable and programmable read-only memories (EEPROM's) will only be made for specific applications, because they use larger chip areas and are more expensive.

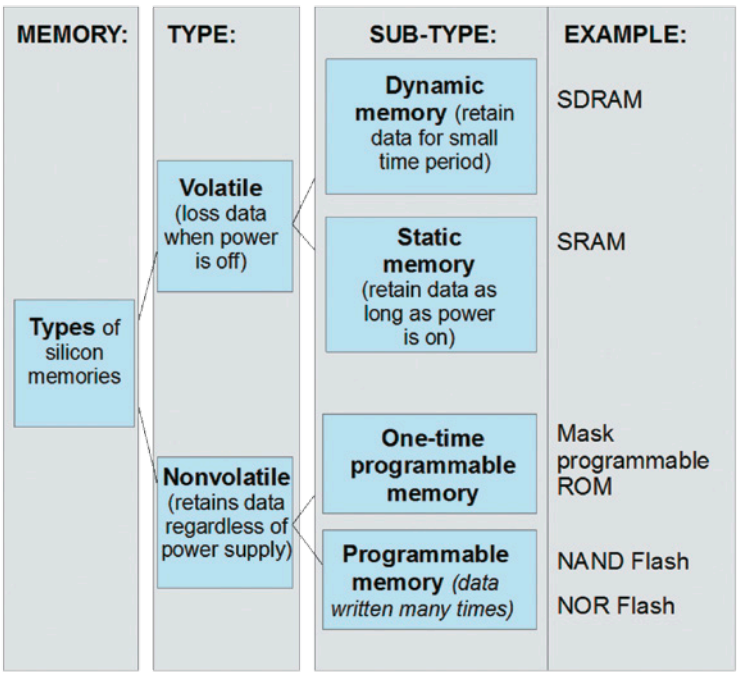

Fig. 1. Flash memories as a type of memory device characterized by non-volatility

Following on from these advantages, the manufacturers of memories started to consider the role of flash memories for a new range of applications. These include hard disk caches, solid-state drives, mobile sensor networks, and data-centric computing. Many microcontrollers have an integrated flash memory for non-volatile data storage. The flash memory is also used in many applications where data retention in power-off situations and reliability are crucial requirements, (i.e. embedded computers or wireless communication systems).

Nowadays, the flash memory is one of the most popular, reliable, and flexible non-volatile memories to store constant data values and software code.

1.1. NAND flash memory architecture

The overall architecture of the NAND flash device is shown in Fig. 2. The figure shows a NAND Flash Controller which gives interface to application processors. The page register is a critical data holding area in NAND operations. The register is incorporated in order to receive new data while the data register simultaneously programs the NAND flash array. Unlike most memory technologies, NAND flash is ordered in pages which are written and read as a unit. The elementary unit of operation for a NAND flash device is one page of data with control commands of the whole block (multiple pages) or the whole chip [13]. Therefore data can be written to only one page at once.

Due to their excellent scalability and performance, NAND flash devices have achieved very high density in terms of bits per mm^2 and feature size scaling. With TLC (triple-level cell), the NAND floating-gate transistors can finally be manufactured at a 6.5 nm process and the density jumps to a supreme level of 1,700 GB per chip.

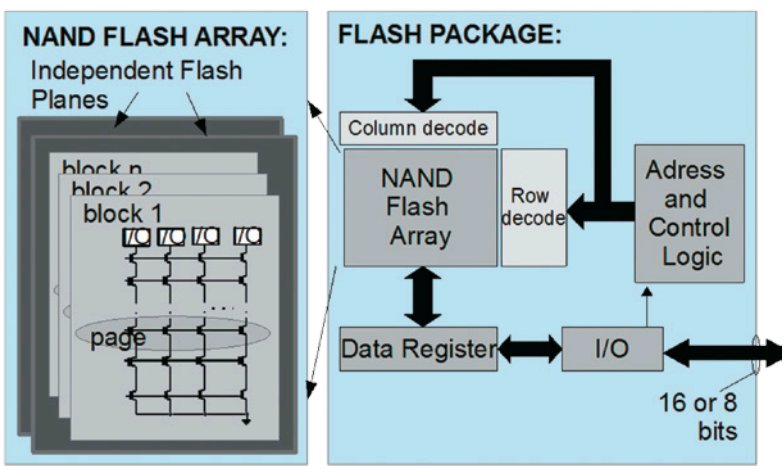

Fig. 2. Architecture of the NAND Flash Device [5]

1.1.1. Flash translation layer, wear levelling and garbage collection

Flash Translation Layer (FTL) is a software layer, which is between the NAND flash storage physical media access layer and the File System layer. The FTL is a part of the NAND controller and performs the functions of logical-to-physical address translation (data locations are represented by their physical addresses), wear levelling mechanism to prevent the early wear out of a block, bad block management, ECC and interleaving operations. The operating system can write to the memory on a page basis without worrying about the details of its physical address space [21].

Due to the nature of NAND flash, wear out is unavoidable when writing to such a device. A related problem is to write to the same address space and create uneven wear of the memory block. The blocks keeping often-updated data are stressed with a large number of write/erase cycles, while the blocks keeping data updated infrequently are much less stressed. The endurance of the NAND flash memory can be significantly enhanced by taking advantage of the wear levelling mechanism, which is able to distribute the memory usage uniformly over the memory blocks array [6]. Wear levelling is a process that spreads out the load of frequently rewritten memory blocks over the NAND flash array as much as possible. When the host application needs an updating of the same (logical) sector, the NAND controller dynamically maps the data into a different (physical) sector, keeping track of the mapping. With regard to the need of minimizing the impact on performance, a garbage collection process is run in the background [21].

There are two types of wear levelling algorithms: dynamic wear levelling and static wear levelling. In the case of the dynamic wear levelling algorithm, the NAND controller internally maintains a map which links the logical block addresses with their corresponding physical flash memory addresses. The NAND controller than assigns a new empty page for every write operation and links the new page to the original address. In the static wear levelling mode, rarely updated static data are kept in the "static" blocks while the cells of low usage are relocated to a new page, which results in almost the same number of rewrite cycles [18].

The wear levelling techniques are based on an assumption of sufficient availability of free sectors. When the number of free sectors falls below a threshold value, there is an algorithm for sector back-up "compaction" and copying the last valid replication, thanks to which the obsolete copies can be deleted. The garbage collection prevents the erasing of a block with valid data and optimizes the process of cleaning the memory. The cleaning policies are set according to the criteria used to pick up the block that is to be erased for garbage collection purposes [21]. The NAND flash memory is free from complex scheduling of the overhead like hard drive disk scheduling, but it is affected by the garbage collection issue [19].

1.2. NAND flash memory characteristics

The development of NAND flash memories has been driven by a gradual progress in novel cell structures and architectural solutions oriented to both reducing the cell size and

upgrading the product functions. The NAND flash memory has become an indispensable component in embedded systems for its flexible features. Applications may need lesser or greater erase counts, different error correction capabilities, and a range of storage longevity requirements. The NAND flash devices differ in many parameters and characteristics, which include cell types, architectural, performance, timing parameters and command set. The subsequent chapters provide an overview of the typical characteristics.

1.2.1. Flash memory non-volatility

The flash memory is non-volatile, which implies that it retains data even without being powered-on. Non-volatility comes from the types of the transistors used, which are floating-gate transistors. Since the data stored are retained even when the memory device is not electrically powered, this device does not need power to maintain its data. The NAND flash is the only memory that offers both high GB density and non-volatility.

1.2.2. NAND flash memory programming and erasing based on block-wise operation

The flash memory has the ability to be programmed and erased electrically, thus combining the advantages of EPROMs and EEPROMs. This increases its flexibility as compared with that of the electrically programmable read-only memories (EPROM's), which are electrically programmable but erasable by ultraviolet (UV) radiation. The dissimilarity between the flash memory and EEPROM lies in the fact that the EEPROM erases and rewrites its content byte by byte. Since the flash memory erases or writes its data in entire blocks, this makes it very fast in comparison with the EEPROM. A single cell can be electrically programmed and a large number of cells (block, sector, or page) can be electrically erased almost at the same time. Since the NAND flash does not offer a random-access external address bus, the data required are read on a block-wise basis (also termed as page access), where each block keeps hundreds to thousands of bits, like in a kind of sequential data access.

1.2.3. Serial storage properties

From the system designer's perspective, the biggest difference is that the NAND flash is a serial storage device whereas most other memories are random access memories (RAM). The serial storage device requires longer access times for the obtaining of data. The result is that the NAND flash as a serial storage device does not give a random-access external address bus and needs a special NAND flash controller to access data and therefore is hardly ever used as the main memory of the system. System designers must reflect these differences when interfacing the end system with the NAND flash device. Since most microprocessors and microcontrollers require byte-level random access, this is one of the main explanations why the NAND flash is inappropriate to replace the RAM memory. The speed at which the DRAM or SRAM may access data and also their capability to address at byte level is incomparable with the flash memory.

1.2.4. Noise in the reading process

In the NAND flash, the only way to access a discrete cell for either reading or writing is across the other cells in its bit line. This enhances noise related to the read process [2], and also needs attention during writing to ensure that adjacent cells in the string are not disturbed. Many of the more difficult characteristics of the NAND flash are due to this organization, which removes much of the decoding overhead found in other memory technologies.

1.2.5. Restricted write endurance

Since cells in a flash chip will fail after a limited number of writes, the limited write endurance is a key characteristic of a flash memory [11]. Infrequently cycled blocks will have longer retention and the blocks that are often cycled will have shorter retention. It is highly important to employ a wear levelling mechanism, which would ensure equal memory block load rather than cycling and potentially destroying the same block. The wear levelling is necessary on MLC (multi-level cell) devices where blocks can normally support less than 10 000 erase program cycles and offers additional advantages on SLC (single-level cell) devices where blocks can offer up to 100 000 erase-program cycles.

1.2.6. Some extended features

There are some extended features offered in addition to those basic ones:

- device operation status read and manufacturer ID read;
- one-time-programmable area (OTP area) to keep vendor unique data such as serial number;
- locking or unlocking the blocks to avert data loss on unintended software operation;
- internal movement of the block into another memory location to avoid the time consuming data relocations from and back to a chip (copy-back);
- only a portion of a page may be programmed at a time and the rest may be programmed at some other time, avoiding block erasing (partial page programming);
- boot-like feature, where page 0 is loaded into data register automatically after reset or power-on;
- supplementary cache register (cache operation) for read operation or pipe-lined program.

1.3. Error correction code in NAND flash memories

In digital communication, the quantity of bit errors is the number of the received bits of a data stream sent through a communication channel that have been changed due to interference, noise, bit synchronization errors or distortion. The bit error rate or bit error ratio (BER) is the number of bits that have errors divided by the total quantity of transmitted bits throughout a given time interval. BER is a unitless measure, frequently formulated as a percentage. The raw bit error rate relates to the probability of a bit error occurring in an

individual bit cell on a flash device [9]. Fig. 3 shows that the bit error rate (BER) is much worse in the parts that have consumed erase, program, and read cycles and that it is different for the SLC, MLC and TLC NAND flash technology.

1.3.1. Noise sources in the NAND flash

There are many noise sources existing in the NAND flash, such as cell-to-cell interference, read or program disturb, retention process, random-telegraph noise, background-pattern noise, charge leakage and trapping generation, etc. [40]. Such noise sources considerably shrink the storage reliability of a flash memory. Over time, the quantity of affected cells increases, see Fig. 3. Fig. 4 shows that the Read Disturb Error Rate is empirically much worse in devices that have consumed erase, program, and read cycles than in uncycled devices [16]. The quality of data retention for uncycled or cycled devices is a natural consequence of memory cell's limited life.

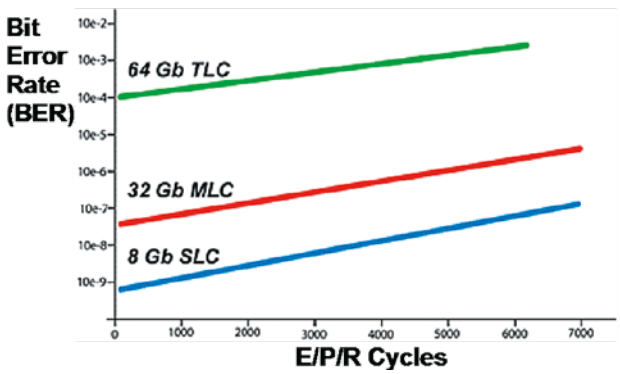

Fig. 3. Bit error rate versus Erase/Program/Read cycles for the Micron NAND flash [16]

Bit errors are a natural consequence of uncertainty when any data storage operation is performed and must be moderated by software or hardware so that the integrity of the original information is not compromised [9]. For the NAND flash, this is implemented by using protecting groups of bits with a higher-level error correction algorithm. To reduce possible errors, Error Correcting Codes (ECC) are widely used in the NAND memories. Through ECC, it is possible to fill the discrepancy between the error probability offered by the memory and the desired error probability. The ECC algorithm takes care of the failures during the life of the device and improves the reliability of the read operation in the customer final application [21]. Preferably, all the storage errors should be adjusted [42]. In reality, the algorithm offers protection against a range of errors that are likely to happen.

Over time, the NAND flash has augmented the storage density by storing more bits per cell and changing to smaller geometries. As the NAND flash memory tends towards more progressive process nodes, the cost of the devices declines, but the cells become more vulnerable [39]. The quantity of bits kept per cell increases, and bit values are represented

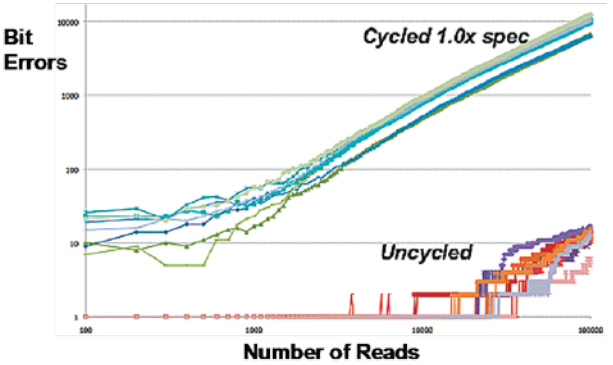

Fig. 4. Bit errors versus number of reads [16]

by smaller voltage ranges, generating more uncertainty in the value stored in the bit cell due to more ambiguity in the amount of charge [9]. As the bit cells get smaller, the individual cells are more vulnerable to failure brought by high-voltage stress because fewer electrons can be trapped in the floating gates. The effect is to narrow the valid voltage ranges for a given value, increasing the probability of program and read disturbances. Since this solution requires higher levels of error correction mechanism in order to ensure the integrity of the data on the flash device, the new technology needs more Error Correction Code (Deal, Hamming, RS, BCH, LDPC) [10].

The accepted uncertainty upsurges the probability for data to be stored or read incorrectly, requiring higher levels of error correction for the MLC flash than for the SLC flash [9] (see Table 1.). The devices using the NAND flash must offer very high error correction levels in order to guarantee support for flash devices of the next generation.

The Multi-Level Cell (MLC) flash has entailed the necessity of using more powerful correction algorithms capable of correcting four to eight bits to manage the higher bit error

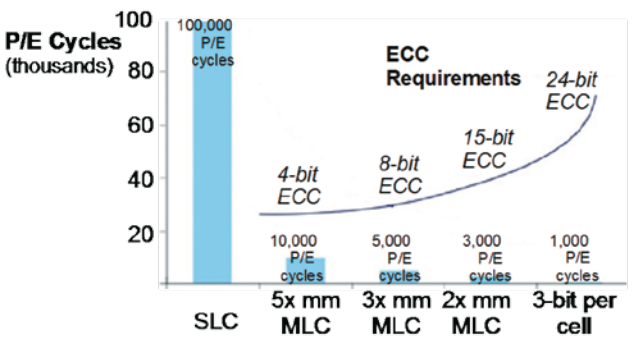

Fig. 5. ECC and a life cycle comparison of the NAND flash by process mode: an increase in the correction capability is not sufficient to maintain adequate endurance of the cell [26]

rates arising from the greater uncertainty of charging and to detect the various voltage ranges in a single bit cell (see Fig. 5) [9].

1.3.2. Error detection and correction in the NAND flash memories

The error correction code (ECC) permits the data being read or transmitted to be checked for errors and, when necessary, corrected. The ECC is a valuable means of recovering the incorrect value from the residual good data bits [13]. The error detection and correction or error control includes techniques that permit reliable transfer of digital data by the detection of errors and reconstruction of the original data, corrected to be error-free. Even if the ECC cannot correct the error throughout the read, it may still detect the error. The ECC is used together with the NAND flash parts to compensate the bits that could fail during device operation. The on-chip error correction code resolves many supposed complications of working with a NAND solution [24]. The on-chip ECC techniques have rarely been adopted [23]; instead, the NAND controller includes hardware that supports ECC calculations. Currently, the error correction is an integral NAND flash part that guarantees data integrity.

Up to now, more error correction has been required for the MLC NAND technology, whereas the SLC NAND has characteristically required only 1-bit ECC for densities up to 4 Gbits fabricated at 43 nm [39]. Current trends in the NAND flash market lead to changes that must be made in the error correction algorithms to preserve the integrity of data stored in the next-generation NAND flash devices [9]. The SLC NAND flash devices, fabricated at 32 nm or 24 nm, require 4-bit or 8-bit ECC, respectively, per 512 bytes [39].

1.3.3. NAND Flash ECC Algorithms

The NAND flash devices need appropriate error correction algorithms to diminish the errors that occur during the programming and read operations [9]. The life span of the NAND flash could be prolonged without more ECC bits thanks to the operation algorithm specially proposed. The error detection is usually realized by using an appropriate hash function or checksum algorithm. A hash function adds a fixed-length tag to a piece of data, which can be whenever recalculated and verified.

The basic system of the ECC theory is to enlarge some redundancy for protection. The redundancy permits the receiver to detect a limited number of errors that may happen anywhere in data, and usually to correct these errors without retransmission. Different ECC techniques are necessary in various types of the flash memory.

Error correction codes are typically divided into two classes: block codes and convolution codes. The difference between them lies in the encoding principle [22]. The block coding works with messages of fixed length. In the block codes, the information bits are followed by parity bits. In convolutional codes, the information bits are spread along the sequence [7]. Hamming codes, Bose-Chaudhuri-Hocquenghem (BCH) codes [25], Reed-Solomon (R/S) codes, and Low-Density Parity Check (LDPC) codes are the most notable block codes

and have been widely used in communication, optical, and other systems [40]. The choice of the most effective correction code is a compromise between the number of symbol errors that need to be corrected and the additional storage requests for the generated parity data. The early designs implementing the SLC NAND used either no error correction or marginally correcting Hamming codes, which offer single error correct and double error detect capabilities [9]. Given the low bit error rates of the early flash, this was satisfactory to correct the sporadic bit error that might arise. As bit error rates grew with each successive generation of both the SLC and MLC flash, designers progressed to more complex cyclic codes such as Reed-Solomon (R/S) or Bose-Chaudhuri-Hocquenghem (BCH) algorithms to increase the correction capability [9]. Both of the algorithms are similar to each other; however, the R/S codes can correct multi-bit symbols while the BCH makes correction over single-bit symbols.

The routinely computed ECC, i.e. the whole code-word, is kept in the spare area of the page to which it relates. Throughout the reading operation, a decoder circuit examines errors in a code-word, and corrects the mistaken bits within its error-processing capability, thereby recovering the code-word [40].

Table 1. ECC recommendations

NAND Type	SLC	MLC	TLC
Datasheet ECC Requirement	1-bit ECC per 528 bytes of data	12-bit ECC per 539 bytes of data	60-bit ECC per 1146 bytes of data
Bit Error Rate	0.02%	0.28%	0.65%
Suggested ECC	SEC/DEC Hamming Code or Reed-Solomon Code	BCH Algorithms	Low Density Parity Check (LDPC) Codes

Table 2. Number of bits required for various ECC correction strengths [25]

Error Correction Level	Bits Required in the NAND Flash Spare Area		
	Hamming	Reed-Solomon	BCH
1	13	18	13
2	N/A	36	26
3	N/A	54	39
4	N/A	72	52
5	N/A	90	65
6	N/A	108	78
7	N/A	126	91
8	N/A	144	104
9	N/A	162	117
10	N/A	180	130

When the unit of data is demanded for reading, a code for the stored and about-to-be-read word is calculated with the use of the algorithm. The ECCs are again calculated, and these values are compared to the ECC values held in the spare area. If the codes match, the data is free of errors. The outcome of this assessment yields an ECC "syndrome" that shows whether errors occurred, how many bits are in error, and, if the errors are recoverable, the bit position of incorrect bits. If the codes do not match, the missing or incorrect bits are determined through the code comparison and the bit or bits are corrected or supplied. The additional information representing the redundancy added by the code is recycled by the receiver to recover the original data. The decoding phase can reduce the read performance as well as the memory response time.

A typical ECC will correct a one-bit error in each 2048 bits (256 bytes) with using 22 bits of the ECC code, or a one-bit error in each 4096 bits (512 bytes) with using 24 bits of the ECC code. However, as raw BER increases, the 2-bit error correction BCH code becomes a desired level of the ECC.

1.4. Summary

Today, the flash memory is one of the most popular, reliable, and flexible non-volatile devices to store data. The NAND flash memory has become very popular for being used in various applications where a large quantity of data has to be stored. This article discusses important aspects related to the NAND flash memory, storage reliability and the actual bit error rate.

A NAND flash device is composed as a memory array, which is separated into several blocks. In general, it performs three basic operations: programming a page, erasing a block, and reading a page. There are many noise sources that exist in the NAND flash, which considerably shrink the storage reliability of the flash memory. The paper presents a preliminary technology review, which was conducted in connection with the preparation of an experiment for evaluating the reliability of the NAND flash memory. The purpose of this study was to summarize the theoretical background. The preliminary aim was to identify the factors that affect the NAND flash reliability for potential use of the methodology of a statistical planned experiment (DOE, Design of Experiments).

Acknowledgments

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2. Advantages of multispeed gear application in electric drive

Electric vehicles are far more efficient than vehicles using internal combustion engines. However, their efficiency can be increased. Small and medium synchronous machines are most suitable for this purpose. The efficiency of electric machines of this kind is high in a specific range of output torque and rotational speed values. In the case of operation at low speeds and high torques, the efficiency values can be lower than 85%. The same problem can also be observed for inverters, where the efficiency may drop below 85% in the specified operating ranges. It will have a strong influence on the energy consumption. In a pure electric drive system, the battery power is transferred to the electric motor via an inverter. This means that, in some cases, the efficiency may be lower than 72%. The total efficiency of the drive system will particularly decrease when the vehicle operation conditions are characterized by low speeds and high output torques of the vehicle motor. The motor operation conditions should be shifted to the area of high efficiency to prevent energy losses. This can be achieved by applying a mechanical transmission that would cause the electric motor to operate at a lower output torque and a higher shaft speed, according to the mechanical transmission ratio.

In many cases, the best solution may be the application of continuously variable transmissions (CVTs). One of the most popular systems is a belt transmission, where polymer V-belts strengthened with Kevlar or carbon fibres are employed. The disadvantages of a classical CVT may be relatively high cost and low efficiency due to friction. Another solution is the use of an Electric Variable Transmission (EVT) [28]. This solution contains an electric machine incorporated with an electric substitute of a planetary gear. In the EVT, the motor torque is transmitted by a magnetic field. Such a concept seems to be more suitable for a hybrid drive system with a thermal engine. The second group can be defined as systems with multispeed toothed mechanical transmissions. Generally, the dual clutch [35] and planetary gear [29] solution of mechanical transmission may be very easily adapted for electric drives. The controlling of such systems is practically identical to that of conventional drives, to which these solutions have originally been dedicated.

Because of mass production and low cost, the manual transmission with a synchronizer mechanism should be considered. However, if a manual transmission is to be adapted for an electric drive system, its operation should be automated. This means that the multispeed transmission unit should be provided with a dedicated control system with appropriate actuators, which should pursue an appropriate control strategy. The control system and the control strategy must be designed with taking into consideration the behaviour of the entire system during vehicle drive, especially during the gear-shifting process. Based on the assumptions made, the general control system and the control strategy for a four-speed manual transmission will be proposed in this paper.

The effect of the application of a mechanical transmission to an electric vehicle is particularly conspicuous when the energy consumption is taken into account. Depending on the driving cycle type applied during tests, the energy consumption of the electric vehicle may be reduced by 5 % to 10 % in the case of a four-speed manual gearbox and by 6 % to 12 % in the case of a CVT gearbox [32]. Additionally, the electric vehicle equipped with a mechanical transmission shows better acceleration performance. For example,

the acceleration time is shortened and the energy consumption during this process is reduced [41].

To check the effect of the application of a four-speed mechanical transmission to an electric vehicle, a computer simulation for such a vehicle of 650 kg total mass was carried out. The objective was to compare the drive parameters with a one-gear and a multispeed transmission at identical output conditions represented by the test cycle referred to as NEDC (New European Driving Cycle). To assess the effect of the application of a four-speed mechanical transmission to an electric vehicle, the travelling range was chosen as a criterion. The percentage gain in the travelling range depending on the configuration of the electric drive system has been shown in Fig. 6.

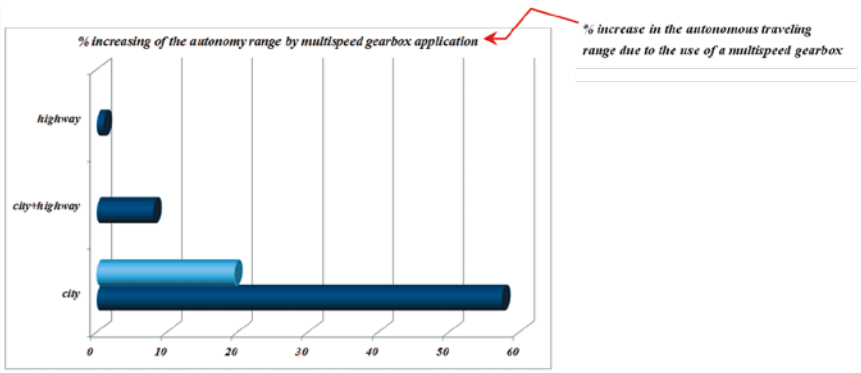

Fig. 6. Influence of gearbox use on the travelling range, depending on vehicle operation conditions

The gain in the travelling range is about 8 % in the case of a multispeed gearbox being used (see Fig. 6). It seems to be not very high. The same effect may be achieved by, for example, increasing the battery capacity. The result obtained may lead us to a conclusion that the use of a multispeed transmission is unreasonable because of the cost and complication of its controlling.

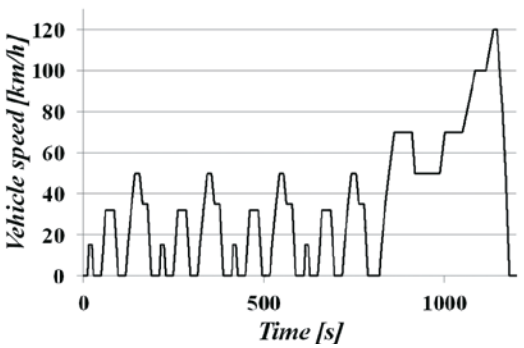

Fig. 7. Standardized NEDC (New European Driving Cycle) test conditions

The computer simulation was done for the NEDC test conditions shown in Fig. 7. It was found that during the operation in urban conditions, the vehicle consumed only 11.4 % of the total energy of the NEDC test. The rest, i.e. 88.6% of the NEDC energy, was consumed during the driving with high speeds. This means that for the NEDC test, the dominant part in the energy consumption has the highway part of the cycle. Because of that, the driving conditions for the vehicle with the constant ratio gearbox and the multispeed gearbox are practically the same. Most of the energy needed for vehicle movement is delivered at a constant gearbox ratio. To check how the energy consumption is distributed between the highway drive and the city drive, a further analysis was done separately for the defined parts of the NEDC test. For the vehicle operation in highway drive conditions, it is seemingly useless to equip the electric propulsion system with a multispeed transmission. The decrease in the energy consumption is very small. However, the situation is different for the city part of the NEDC test. It is easy to note that the travelling range for the drive with the multispeed gearbox is longer by about 57% than that for the drive with the constant ratio gearbox, thanks to appropriate selection of the gear ratios and limitation of the PM Synchronous Motor output torque only. Another thing is that the constant ratio transmission is only favourable for the highway drive conditions and practically useless in the city. To increase the travelling range in the case of a constant ratio transmission being used, the transmission ratio should be changed. The appropriate adjustment of the constant ratio to the vehicle operation in the city driving conditions results in decreasing the difference in the travelling range to 19.5%. But the use of this ratio makes it impossible to drive the vehicle with torques and speeds as required by the NEDC test conditions applicable to the highway part of the test cycle.

Based on the analyses results, the application of a mechanical multispeed transmission is very important for the EV, especially in the city driving conditions. One of the reasons is the fact that the mechanical transmission enables the PM motor to operate with its maximum efficiency during the driving cycle, thanks to which the total efficiency of the electric drive system is raised. Another argument for applying multispeed transmissions to electric vehicles is the high resistance of such transmissions to vehicle operation conditions. The simulation analyses have shown that the application of mechanical multispeed transmissions to electric vehicles is promising for both the city and highway operation conditions.

The drive efficiency depends on the appropriate selection of the transmission ratio as well as on the use of an adequate control system operating with speed and torque feedback. The control system and the actuators must be compatible with the type of the transmission used in the electric vehicle and with the type of the electric motor. Additionally, the system must be able to operate in the conditions of both vehicle acceleration and regenerative braking. In consideration of the system efficiency, the use of a PM motor was assumed for further analyses.

Within the IDEAS project, the WUT in cooperation with DEST will carry out further research on the possibility of the automation of a manual four-speed gearbox and the application of such a gearbox to electric drive systems.

2.1. Gear-shifting process

The synchronized side of the transmission consists of the gearbox input shaft and the associated gears. The synchronizing side is composed of mechanical parts down to the vehicle wheels. The gear-shifting mechanism consists of forks and shafts moved by actuators. The classic synchronizing mechanism consisting of synchronizer with one conical surface clutch is shown in Fig. 8.

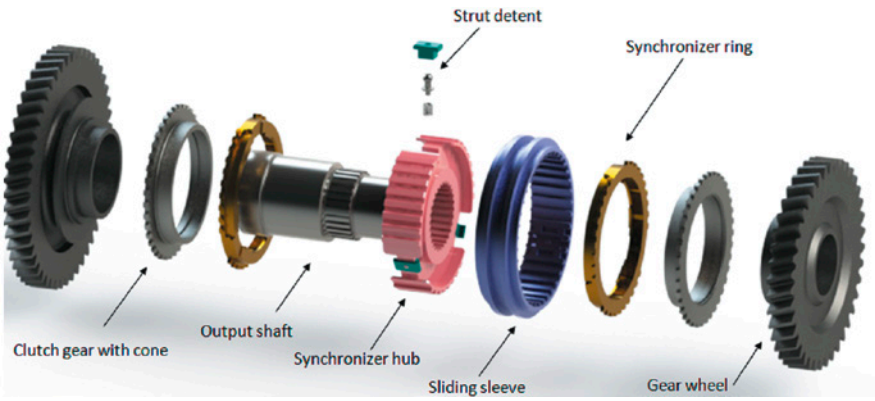

Fig. 8. Exploded view of a synchronizer [3, 6]

The main parts of this mechanism are as follows [3]:

1.1 **Synchronizer hub** rigidly connected to the shaft (input or output).

1.2 **Sliding sleeve** movable only axially from the neutral position to an engaged position.

1.3 **Synchronizer ring**. Its external teeth give a possibility to interlock with the internal teeth of the sliding sleeve. Its conical surface fits to the conical surface of the clutch body ring. Thanks to that, it is possible to produce the friction torque needed to synchronize the input and output shafts.

1.4 **Clutch gear with cone** matches the speed of the gear with the speed of the synchronizer ring and hub.

1.5 **Gear wheel:** connected to the main shaft by a needle bearing for relative rotation between both components and secured against axial movement relative to the shaft.

1.6 **Strut detent** is used for pre-synchronization, which means that it generates the load on the synchronizer ring to perform the synchronization process.

The process of gear engaging can be divided into 8 phases as follows [20].

First free fly (Phase 1). In this phase, the sleeve moves forward axially without significant mechanical resistance and displaces the strut detent, which pushes the synchronizer ring towards the cone of the gear.

Start of the speed synchronization (Phase 2). The axial pushing force applied to the sleeve

increases. This force is transmitted from the sleeve to the strut detent and then to the synchronizer ring. After the transmitted force has reached a prescribed level, the sleeve slightly moves forward and its internal teeth come into contact with the external teeth of the synchronizer ring. The conical surface of the synchronizer ring meets the conical surface of the gear clutch. At the end of this phase, the axial velocity of the sleeve is zero.

Angular velocity synchronization (Phase 3). The axial force increases and then it is maintained practically at a constant high level. The difference between the angular velocities of the sleeve and the gear decreases to zero thanks to the friction on the conical surfaces of the gear clutch and the synchronizer ring. As long as an angular velocity difference exists, the equilibrium of axial and tangential forces present on the spline chamfers prevents continuation of the sleeve movement. This phase usually lasts for about half of the gear-shifting time and is crucial for this process.

Turning of the synchronizer ring (Phase 4). When the angular velocity difference reaches zero, the friction phenomenon fades away. The resistance force component on the sleeve spline chamfers disappears. The sleeve starts to move axially and, at the same time, a decrease in the axial force can be noticed. The displacement of the sleeve turns the synchronizer ring and the gear while the chamfers remain in contact.

Second free fly (Phase5). The synchronizer ring stops turning when the spline chamfers separate from each other. The sleeve moves forward axially until approaching the spline chamfers of the gear. The angular velocity of the gear is assumed to be equal to that of the sleeve.

Start of the second bump (Phase 6). The axial force steeply increases to stop when the tangential force component from the force equilibrium on the chamfers gets high enough to turn the synchronizer ring previously stuck on the cone. The synchronizer ring then becomes free and the sleeve can continue its axial displacement. The consecutive increase in the axial force is the first component of the phenomenon called double bump.

Turning the gear (Phase 7). After separation of the synchronizer ring and the gear cone, the sleeve turns the gear when moving forward with a low axial velocity. The value of the axial force required for turning depends on the relative position of the sleeve splines and the gear splines. This position is obtained at the end of the synchronization phase.

Final free fly (Phase 8). After turning the gear, the sleeve moves forward axially and meshes with the splines of the gear. The gear is thus locked.

As the behaviour of these mechanical parts is complicated because of a large number of the elements involved, it is not easy to analyse the entire gear-shifting process in detail. When the gear is engaged, the torque from the electric machine is transferred to the wheels thanks to rigid connection between the internal and external teeth of the sleeve and gear clutch. Additionally, the relative position of this connection prevents the gear from disengagement thanks to the friction force between the teeth of these elements. For the gear shifting to be possible, it is necessary to decrease this force by reducing the output torque of the electric machine. The absence of the driving torque is also required during the synchronization process. The alignment of the input and output shafts is done by the

friction on the conical surfaces of the synchronizer ring and gear clutch. The dimensions of these surfaces are relatively small, which means that the torque transmitted by the friction must be limited. This translates into a requirement that the output torque of the electric machine should be reduced almost to zero. Due to all the above, the gear synchronization phase is most interesting from the electric drive control point of view.

All the conditions mentioned above must be fulfilled for the gear shifting in the electric drive system to be possible. Therefore, all of them must be included in the algorithm of controlling the electric drive system with a multispeed transmission.

For the gear shifting analyses, a simplified mathematical model of the synchronizer was used.

The synchronizer's behaviour during gear shifting is described by the following equations:

$$I_{ME}\frac{d\omega_1}{dt} \quad T_m - T_f sign\,(\omega_1 - \omega_2) \tag{1}$$

$$I_v\frac{d\omega_2}{dt} \quad -T_v - T_f sign\,(\omega_1 - \omega_2) \tag{2}$$

where:

I_{ME} – moment of inertia of the motor and all the system components on the motor side of the synchronizer, reduced to the synchronizer ring;

I_v – moment of inertia of the vehicle and all the system components on the gear wheel side of the synchronizer, reduced to the gear clutch;

T_m – electric machine torque (for the synchronization process, it is equal to 0);

T_f – friction torque on the gear clutch;

T_f – vehicle resistance torque reduced to the gearbox input shaft on the next gear;

ω_1 – motor speed reduced to the synchronizer ring;

ω_2 – vehicle speed reduced to the gear clutch.

Due to the synchronizer construction, the friction torque was defined as the torque developing on the conical surface of the gear clutch; therefore, it may be expressed as follows:

$$\mathrm{T_f} = \frac{\mathrm{F_w\,D_m\,\mu}}{2\sin\alpha} \tag{3}$$

D_m – average diameter of the clutch friction plates;

μ – coefficient of friction;

F_w – axial force acting on the synchronizer ring;

α – cone angle.

2.2. Virtual test bench

A virtual test bench has been prepared in the MATLAB/Simulink environment and it consists of four basic elements represented by their mathematical models: motor with inverter,

transmission (including the components involved in the synchronization process), electrochemical battery, and vehicle [36, 37, 38]. Such a way of electric drive modelling offers a possibility to modify in an easy way the system configuration just by replacing a single box with another one representing a different component type.

An additional block in the simulation model is the control block where two things have been implemented: electric machine voltage control according to the real and reference speed (PID controller) and electric machine torque control during gear shifting (zero active motor torque during gear change).

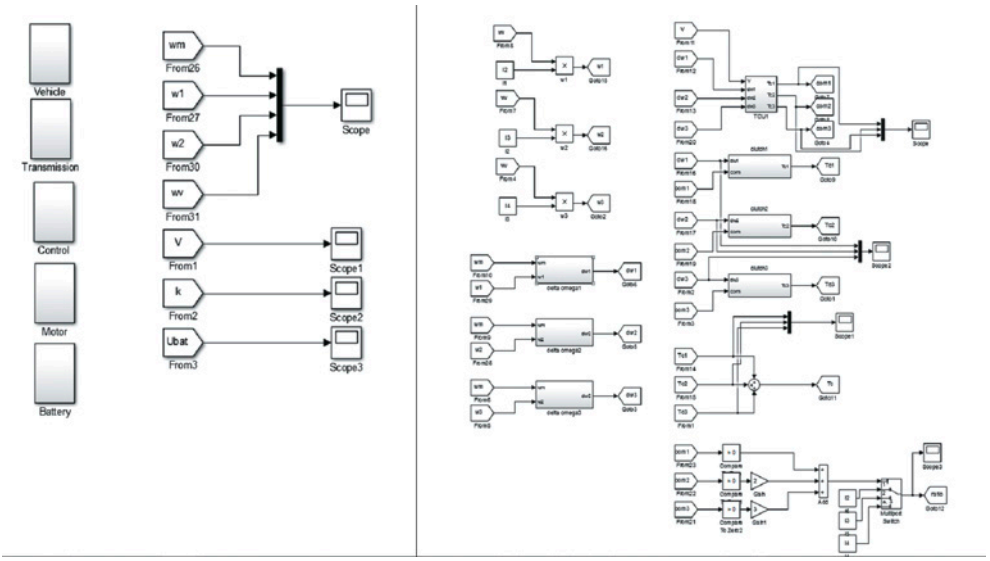

Fig. 9. Virtual test bench representation in MATLAB/Simulink®

Such a method of building a mathematical model of an electric drive system with a mechanical transmission offers a possibility of analysing different drive control strategies. A general assumption made at modelling the controlling of the drive system during vehicle acceleration and forward drive has been described below. Before starting a drive, the gearbox is shifted into the first gear by appropriate action of the actuators. The parking brake is released and the brake lamp is switched off. The traction motor is controlled by pressing the accelerator pedal. The motor shaft and transmission output shaft speeds are measured. The measured speed is compared with the reference gear-shifting thresholds shown in Fig. 10. The thresholds with the accompanying hysteresis loops must be predefined for individual gears.

The gear-shifting procedure is executed when the appropriate speed threshold is reached. Immediately before the gears are to be changed, the motor torque is reduced to the minimum, which is detected by measuring the motor current. The actuators change their positions when the motor torque reaches its minimum. To change gears from first

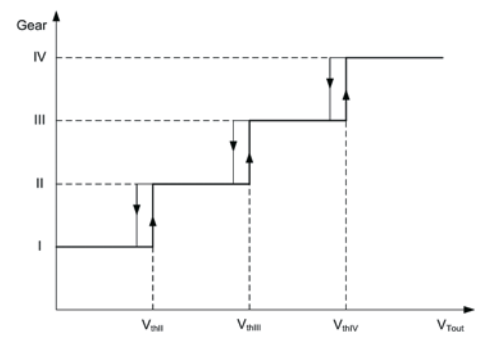

Fig. 10. Gear-shifting thresholds for the four-speed gearbox

to second (see Figs. 10 and 11), actuator 2 must stay in the same position and actuator 1 goes to position 2, putting the gearbox to neutral (N), and then it goes to position 3, shifting into second gear. After the gear shifting process is completed, the motor torque is set to the desired value. The algorithm of gear shifting in the forward drive mode has been presented in Fig. 11.

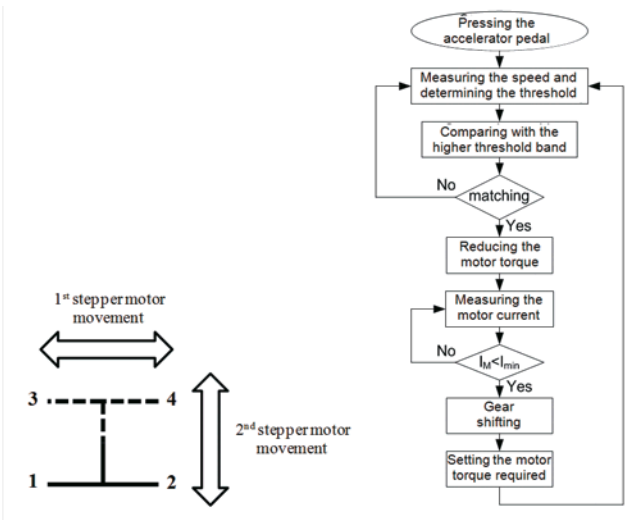

Fig. 11. Algorithm of gear shifting in the forward drive mode

During the vehicle regenerative braking, the gear shifting is accomplished likewise and all this makes a basis for the electric drive control strategy.

For the control strategy details to be correctly defined, the influence of various parameters on the interactions between the main components of the electric drive system must

be known. This knowledge can be acquired by simulation testing of the electric drive system under consideration with taking into account different input parameters and analysing their influence on the behaviour of system components.

One of the parameters of the greatest importance from the drive control point of view is the time of synchronization during gear shifting. The simulation tests were carried out with taking into account the influence of such parameters as vehicle speed thresholds for specific gear changes, motor inertia (which is important because the motor shaft is permanently fixed to the gearbox input shaft), longitudinal force acting on the synchronizer, and active torque on the motor shaft (at both the acceleration and regenerative braking). For smooth gear shifting in manual transmissions, the synchronization time should be within the limits from 0.2 s to 0.6 s [3, 4]]. Therefore, an assumption was made for the subsequent selection of parameters for the control strategy that the gear-shifting time should be shorter than 0.6 s. The gear-shifting time values are inversely proportional to the longitudinal force, which means that the application of higher forces results in the shortening of the synchronization time. Actually, the values of the said forces range from 500 N to 700 N, according to [3, 4]. The simulation results for the longitudinal force of 600 N have been shown in Fig. 12. In this case, the synchronization time was shorter than 0.5 s (0.3 s for the shifting from 1st to 2nd gear).

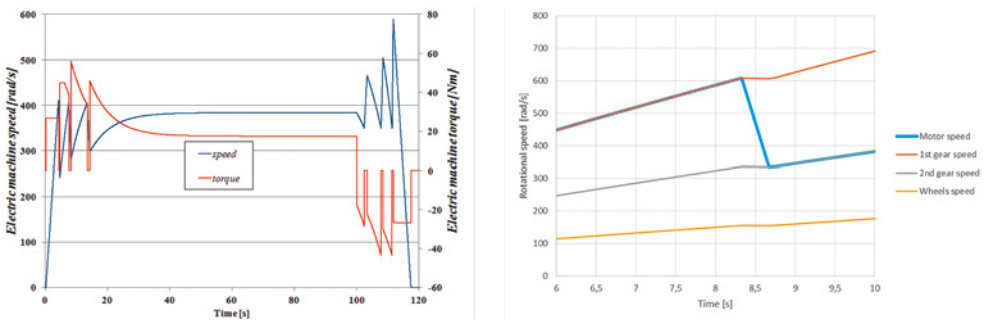

Fig. 12. Example results of the simulation tests

The simulation tests results obtained with the use of the virtual test bench will provide a basis for defining the control strategy that would then be implemented at the laboratory bench tests.

2.3. Laboratory test bench

The structure of the electric drive system with an automated manual transmission is shown in Fig. 13. The electric machine is powered from a battery via a Traction Motor Controller. The electric machine shaft is coupled with the wheels through a multispeed gearbox.

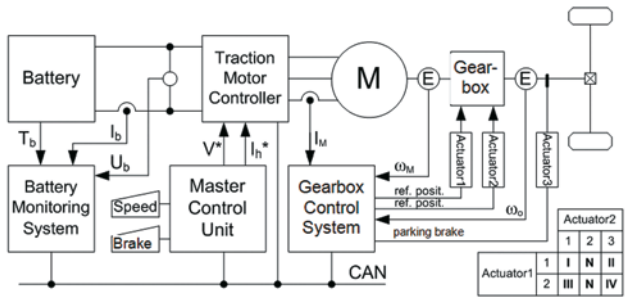

Fig. 13. Structure of the electric drive system with an automatic-shifting gearbox

In the automated gearbox, gears are shifted by two actuators. Actuator 1 can be set in three positions. The outer positions enable gears selection and the middle one (N) makes it possible to put the transmission in neutral. The N position is a transient state between two gears. Information about the position of Actuator 1 is necessary for proper indication of the gear selected. As the actuators, DC stepper motors have been applied. Every stepper motor to be used for this purpose must be equipped with an angular position sensor, e.g. an optical encoder. The motor shaft moves in accordance with the number of pulses generated by the controller; therefore, the actuator position can be determined by counting the pulses. Actuator 2 can be set in two positions and they can be indicated by pulse counting as well. The actuators' operation is managed by a Gearbox Control System (GBCS). The parking brake is engaged by Actuator 3. The Master Control Unit (MCU) is responsible for the implementation of the overall control strategy.

One of the very important components of the electric drive control system is the Battery Monitoring System (BMS). The travelling range of an electric vehicle strongly depends not only on the energy stored in the electrochemical battery but also on the way how the energy is utilized. This can be seen from results of the analyses of the influence of the application of a multispeed transmission on the vehicle travelling range (see Fig. 6). A further reduction in the battery energy consumption may be attained by properly adjusting the drive system parameters depending on the energy condition of the electrochemical battery. The state of charge (SOC) is a parameter defining the energy available from the battery. The knowledge of the battery energy parameters makes it possible to adjust the controlling of the drive system so that the battery energy is most effectively utilized, according to the current depth of discharge (DOD) of the battery.

In the Multisource Propulsion Systems Department of WUT, a laboratory test bench was made (see Fig. 14) to verify the assumed strategy of controlling an electric drive system with a multispeed transmission.

The main parts of the laboratory test bench are Li-ion battery, PM Synchronous motor, 4-speed transmission controlled by stepper motors via a screw mechanism, and dynamometer representing the vehicle load.

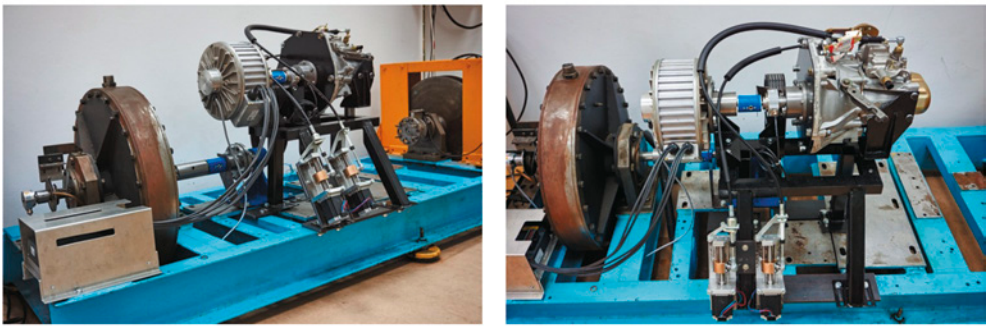

Fig. 14. Laboratory test bench

The control strategy is implemented by a control system consisting of Master Controller (MC), Permanent Magnet Synchronous motor Control Unit (PMSCU), Gearbox Control System (GBCS), and Battery Monitoring System (BMS). The MC works in a closed loop with speed feedback and stepper motor screw mechanism position feedback. The MC sends an acceleration signal to the PMSCU. The PMSCU speeds up the electric machine. When the vehicle speed reaches a prescribed level, the MC sends a signal to the PMSCU to reduce the PMS current. When this is done, the MC sends a signal to the GBCS and the stepper motor makes an appropriate number of steps. When the gear-shifting operation is finished, the GBCS sends a signal to the MC and then the PMSCU continues the motor speeding up.

The data acquisition system consists of speed, torque, voltage, and current sensors.

Battery Monitoring System BMS

The identification of the initial battery parameters is necessary for proper operation of the electric drive. The state of charge (SOC) of the battery determines the possible range and dynamic performance of the electric vehicle. Apart from the SOC, voltage balance on the battery cells must be checked. For safety reasons, the maximum cell voltage must be controlled and limited. The cell with excessive voltage is bypassed by a resistor. The state of charge can be calculated based on the electromotive force (EMF) and internal resistance curves obtained from laboratory tests and with using the feedback from battery voltage, current and temperature measurements.

The Warsaw University of Technology (WUT) in cooperation with DEST worked out a Battery Monitoring System for the 24-cell Li-ion battery. The proposed system shown in Fig. 15 can be extended up to 192 cells.

The BMS integrates a digital signal processor (DSP) and a precise analog to digital converter (ADC); its function is to measure the battery cell voltages and current with high accuracy and the controllable bypass current with the use of resistors and FETs for individual cell balancing. The Main Processor Unit controls cell balancing of individual cells by managing

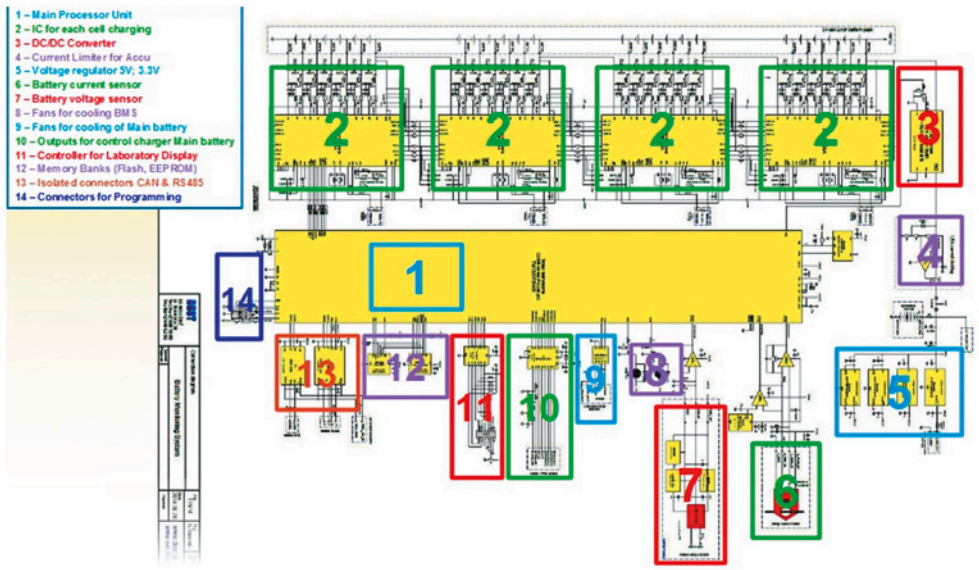

Fig. 15. Schematic diagram of the BMS with connections

ICs via SPI. The IC is a battery monitor, stackable into a series of three to six units intended to serve individual lithium-ion battery packs; it incorporates an ADC and independent cell voltage and temperature protection systems. The 24-cell battery monitoring system consists of 4 ICs stacked in series with SPI communication. The BMS is powered from the battery stack. The DC-DC converter with a 15 V output and Current Limiter are applied to charge a 12 V backup accumulator. The output circuits of the sensors are connected to the ADC of the Main Processor Unit.

Fig. 16. Battery Monitoring System with cables and connectors

DEST prepared a hardware application of the BMS, based on an elaborated concept and shown in Fig. 16. The WUT performed laboratory tests of the Li-ion battery and prepared charging and discharging characteristics. The indication of the balancing of the SOC and battery cell voltages will be verified by laboratory bench testing of the electric drive system with an automated gearbox. The Battery Monitoring System is ready for operation with a 24-cell lithium-ion battery.

The system includes a current bypass circuitry based on FETs and resistors. A unique heat-sensing system with fans of controllable speeds makes it possible to bypass each cell of the battery. The BMS comunnicates with the MC via a CAN bus.

Gearbox Control System

A schematic diagram of the Gearbox Control System is shown in Fig. 17. The Main Processor Unit communicates via SPI with power driver for stepper motors ICs denoted by 7 in the schematic. The integrated power MOSFETs in the driver handle motor currents of up to 2.2 A RMS continuously or 2.8 A RMS boost current per coil at an operating voltage of up to 30 V.

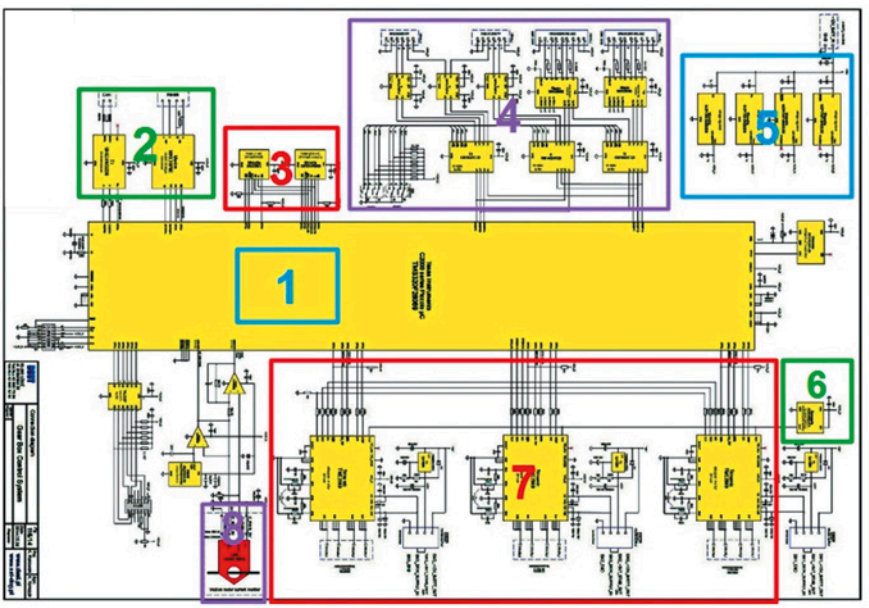

Fig. 17. Schematic diagram of the Gearbox Control System (GBCS)

The Main Processor Unit initializes the driver by sending commands through an SPI bus to write the control parameters and operation mode. The MPU can control the motor position by sending pulses on the STEP signal while indicating the direction on the DIR signal. The stepper motor driver has a microstep counter and a sine table to convert these signals

into the coil currents, which control the motor position. The current fed into the motor coils is controlled by using a cycle-by-cycle chopper mode.

A practical realization of the Gearbox Control System is shown in Fig. 18.

Fig. 18. Gearbox Control System

3. Electromagnetic compatibility (EMC) in electric vehicles

In the recent years, the electromagnetic compatibility of electric vehicles has become an important technological issue in the research and development works on EV's. Steady growth in the popularity and use of electric and hybrid vehicles results in the generation of electromagnetic interferences (EMI) of new types and intensity levels. Vehicles with internal combustion engines (ICE) usually produce two main EMI types: broadband interferences, generated by the ignition system, switches and electrical motors, and narrowband interferences emitted by electronic sub-assemblies (ESA's). Electric vehicles, which use high-power electronics to drive their motors, generate electromagnetic interferences of high level and low frequency. In hybrid vehicles, this new emission type is added to that caused by the ignition system. The charging process of the EV's requires the introduction of new devices in the power supply network, so additional considerations must be taken into account in this case, too [34].

All the aspects mentioned above indicate that the integration of electric drive systems into motor vehicles poses a serious problem. The power required by the electric drive is much higher than the power demand of the whole electric system of the comparable conventional vehicle. The voltage in high-voltage buses can reach 900 V. This is the reason why standard test procedures are not sufficient for such components due to, among others, the power involved and the noise emitted [15]. The standards and setups must be modified to manage this new EMI issue. The measurements cannot be carried out in the idle state, the electric motor must be running and appropriately loaded and the tests meeting this requirement have to be performed in anechoic chambers, and this poses a new challenge to the high-tech test sites. The assessment of devices connected to the high-voltage network requires the use of power supply networks of new type with stabilized line impedance. The strong currents flowing in the system may induce magnetic

fields inside the vehicles, which can have a harmful impact on people's health, so adequate safety requirements must be determined. Radiated transient disturbances constitute another new issue that must be considered in EV's and HEV's [34].

According to UN ECE Regulation No. 10, revision 4, the electric vehicles and their sub-assemblies, which are connected to high-voltage networks, have to be subjected to the following tests [30]:

For vehicles:

- measurement of radiated broadband electromagnetic emissions from vehicles;
- measurement of radiated narrowband electromagnetic emissions from vehicles;
- testing for immunity of vehicles to electromagnetic radiation;
- testing for emission of harmonics generated on AC power lines from vehicles;
- testing for emission of voltage changes, voltage fluctuations and flicker on AC power lines from vehicles;
- testing for emission of radiofrequency conducted disturbances on AC or DC power lines from vehicles;
- testing for emission of radiofrequency conducted disturbances on network and telecommunication access from vehicles;
- testing for immunity of vehicles to electrical fast transient/burst disturbances conducted along AC and DC power lines;
- testing for immunity of vehicles to surges conducted along AC and DC power lines.

For electrical and electronic sub-assemblies (ESA's):

- measurement of radiated broadband electromagnetic emissions from electrical/electronic sub-assemblies;
- measurement of radiated narrowband electromagnetic emissions from electrical/electronic sub-assemblies;
- testing for immunity of electrical/electronic sub-assemblies to electromagnetic radiation;
- testing for immunity to and emission of transients of electrical/electronic sub-assemblies.

The new, 5th revision of the UN ECE Regulation No. 10 provides additional requirements for ESAs [31]:

- testing for emission of harmonics generated on AC power lines from an ESA;
- testing for emission of voltage changes, voltage fluctuations and flicker on AC power lines from an ESA;
- testing for emission of radiofrequency conducted disturbances on AC or DC power lines from an ESA;
- testing for emission of radiofrequency conducted disturbances on network and telecommunication access from an ESA;
- testing for immunity of an ESA to Electrical Fast Transient/Burst disturbances conducted along AC and DC power lines;

– testing for immunity of an ESA to surges conducted along AC and DC power lines.

It is apparent that the EMC measurements for hybrid and electric vehicles have become a very complex issue, which requires advanced and innovative equipment solutions and highly experienced and specialized scientific and technical staff.

3.1 Selected EMC test results for the electronic devices having been developed

All the developed components of the electric vehicle control system (MCU, GBCS, BMS) were tested for their radiated electromagnetic emissions. The measurements were performed in a GTEM 1000 cell in a frequency range of 30–1000 MHz. The test results are presented in Figs. 19–21.

The results presented show that the electromagnetic emissions from the Master Control Unit and Battery Monitoring System did not exceed the permissible level. It can also be seen that the Gearbox Control System generated disturbances in both the broadband and narrowband range. The GBCS module was subjected to additional validation tests. The functional tests of the unit were carried out with dedicated testing software being used. During the tests, particular attention was paid to the device's resistance to the interferences introduced by a running stepper motor. The issues observed with special care also included correct SPI communication with the stepper motor driver, communication with the LCD and the EEPROM memory, and proper operation of the analog-to-digital converter, incremental encoder, and CAN communication. The excessive electromagnetic interference generated

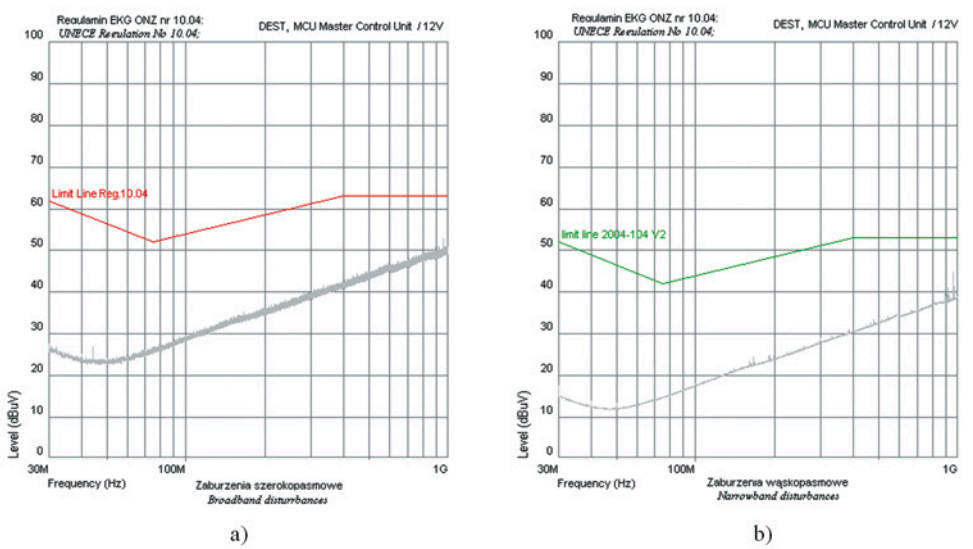

Fig. 19. Electromagnetic interference generated by the Master Control Unit: a) broadband interference; b) narrowband interference

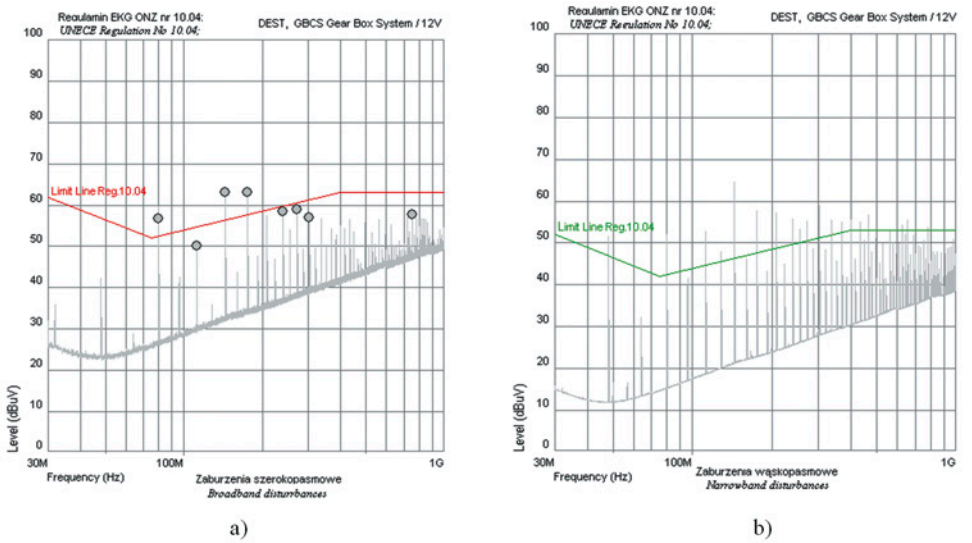

Fig. 20. Electromagnetic interference generated by the Gearbox Control System: a) broadband interference; b) narrowband interference

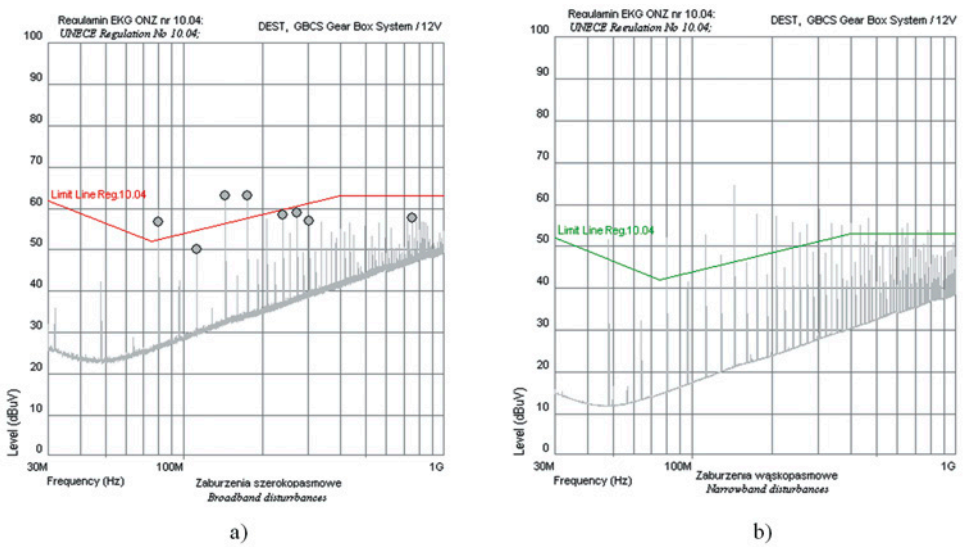

Fig. 21. Electromagnetic interference generated by the Battery Monitoring System: a) broadband interference; b) narrowband interference

by the GBCS was caused by incorrect construction of the electronic system, which has to be modified to meet the EMC requirements. In result of the validation tests, a number of modifications were introduced to the system.

4. Energy consumption in relation to energy efficiency

One of the main objectives of the IDEAS project is to increase the energy efficiency of the vehicle drive train by developing new components of the drive and control system.

In the ICE-propelled vehicles, only about 14–30 % (depending on the driving cycle) of the fuel energy is used to cause the vehicle movement. The rest of the energy is lost due to the engine and driveline inefficiencies or used to power the vehicle accessories (Fig. 22) [43].

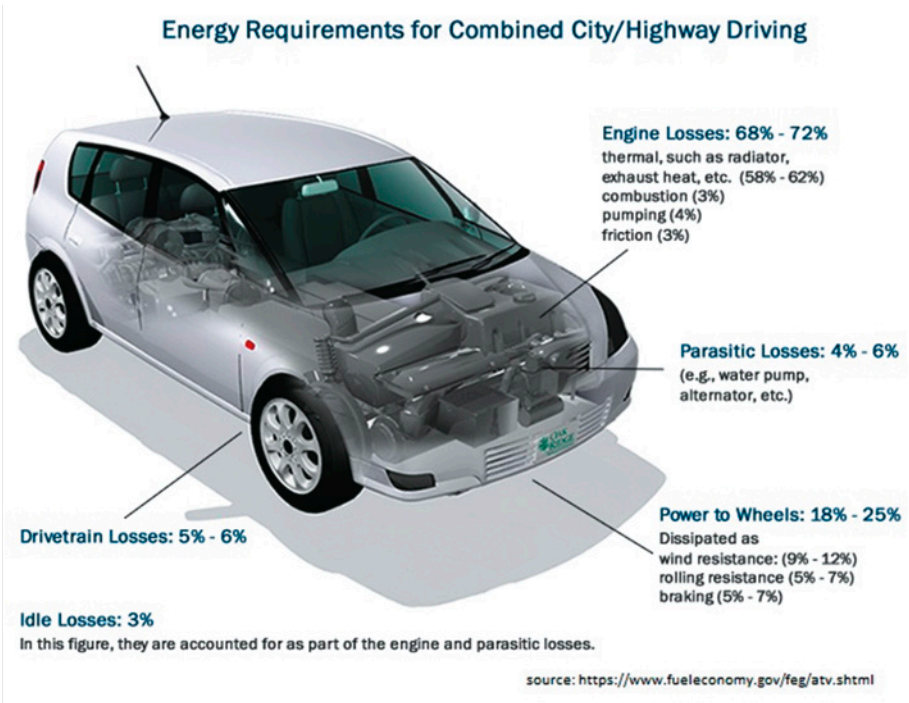

Fig. 22. The energy losses and efficiency of the ICE-propelled vehicle for a combined driving cycle [43]

For comparison, the electric vehicles convert about 59 – 62 % of the electrical energy drawn from the grid into the power at wheels (Fig. 23). In the case of EV's, this parameter not only influences the absolute energy consumption and thus the life cycle balance but also has a major impact on the driving range or required battery capacity and, in consequence, on the vehicle weight and cost [17].

The standardized test cycles (e.g. NEDC) used to evaluate the energy efficiency do not offer a possibility of the obtaining of results that would represent the energy consumption for realistic usage profiles and would be related to individual consumption parameters [12], e.g. air conditioning or heating.

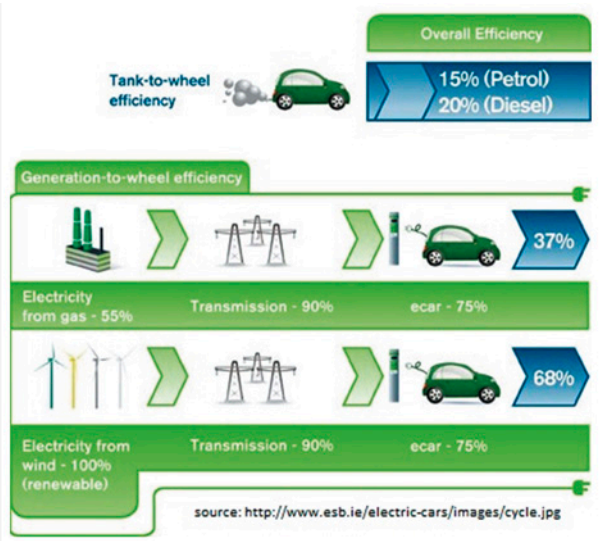

Fig. 23. Energy efficiency of conventional and electric vehicles (includes the source of the grid energy) [44]

The advantage of EV's, which cannot be discounted, is that electric vehicles charged with additional renewable energies lead to a significant improvement in the greenhouse gas balance, but other electricity sources lead to no substantial improvement or even higher life cycle emissions. This is why it is so important to realize that the market penetration of EV's should be based on the use of renewable sources [17].

4.1. Energy efficiency assessment of the vehicle prototype

One of the next stages of the IDEAS project will be the implementation of a vehicle prototype (based on the vehicle shown in Fig. 24.) with using the developed components of the electric vehicle control system (MCU, BMS, GBCS). The mechanical components (Fig. 25) and the main connections for the drive train (Fig. 26) have already been made and the software necessary to continue the research work is being developed at the Warsaw University of Technology (Politechnika Warszawska).

When the prototype is built and all the necessary control system components are programmed, based on the results obtained from the laboratory bench tests, the actual energy consumption will be measured and the energy efficiency will be evaluated [14].

The measurements will be performed on a roller dynamometer test bench, built in accordance with the schematic diagram presented in Fig. 27.

The results to be obtained will give an answer to the question about the validity of the multispeed gear application and functioning of the vehicle control system.

Fig. 24. Vehicle prototype, to be used as a base for the installation of the control system units having been developed (MCU, BMS, GBCS)

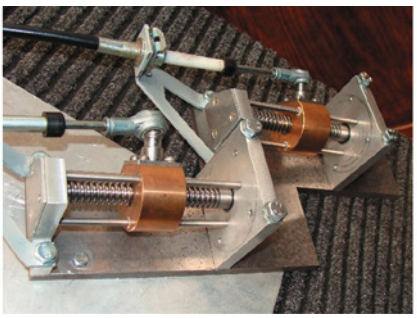

Fig. 25. The base of the stepper motors

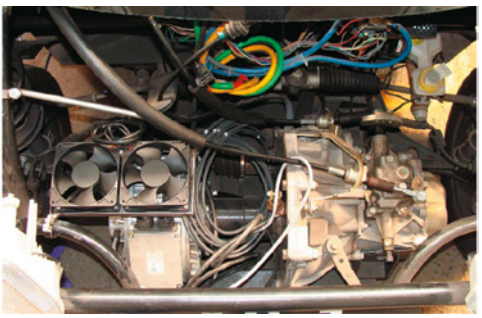

Fig. 26. Engine compartment of the vehicle prototype

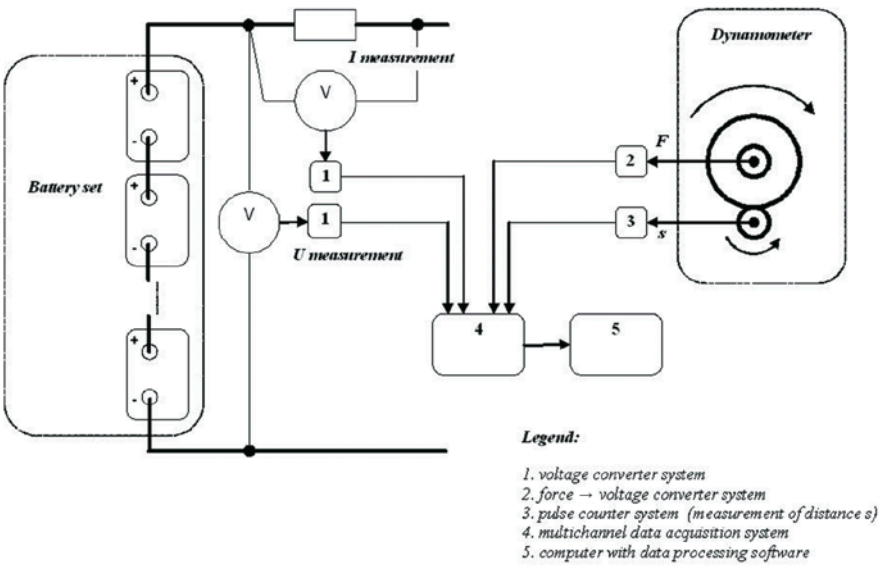

Fig. 27. Schematic diagram of a test setup to evaluate the energy efficiency of the system

5. Conclusions

Today, the flash memory is one of the most popular, reliable, and flexible non-volatile devices to store data. The NAND flash memory has become a very popular solution suitable for use in various applications where large amounts of data have to be stored. This article discusses important aspects related to the NAND flash memory, data storage reliability, and actual bit error rate.

A NAND flash device is composed as a memory array, which is separated into several blocks. In general it performs three basic operations: programming a page, erasing a block, and reading a page. There are many noise sources that exist in the NAND flash, which considerably shrink the storage reliability of the flash memory. The paper presents a preliminary technology review, which was conducted in connection with the preparation of an experiment for evaluating the reliability of the NAND flash memory. The purpose of this study was to summarize the theoretical background. The initial aim was to identify the factors that affect the NAND flash reliability for potential use of the methodology of a statistical planned experiment (DOE, Design of Experiments).

The "Interactive Power Devices for Efficiency in Automotive with Increased Reliability and Safety" (IDEAS) Project deals with problems that are very important for modern electric drives. One of such issues is the efficiency of electric drives. This efficiency can be raised by optimizing both the structure and control strategy of such systems. It is very important that the control strategy must be matched to the structure of the electric drive.

The adding of a multispeed transmission to the electric drive will result in an increase in the drive efficiency. Thanks to that, the electric vehicle driving range will be extended, especially in cities. However, the transmission must operate in the automated mode both during acceleration and at regenerative braking; it must be equipped with special electronic devices and actuators.

The WUT in cooperation with DEST worked out project design requirements for the devices mentioned above. Based on that, DEST has built prototypes of the Gearbox Control System and the Battery Monitoring System. The said electronic devices will be used for the construction of a laboratory test bench. Simultaneously, a virtual test bench has been developed with using the unique mathematical models of all the electric drive components including the transmission with a synchronizer mechanism. Thanks to the virtual test bench, different system control strategies can be tested. Based on the virtual tests, the best strategy will be applied to the laboratory test bench. The principles of the control strategy of an electric drive system with an automated manual multispeed transmission will be checked.

Both the laboratory test bench and the virtual test bench will be operated during classes at the Electric and Hybrid Vehicles Engineering course of study.

The passenger safety and environmental protection are critical issues, which must not be neglected by the automotive industry. All vehicles and components used for the vehicle construction are subject to stringent requirements. The conformity with the requirements is verified, first of all, by approval tests.

In order to ensure marketability of the solutions having been developed, the electronic devices designed within the IDEAS project were subjected to the necessary tests. A vehicle prototype was mechanically prepared for the electromagnetic compatibility and energy consumption tests. The results obtained from the laboratory bench tests will be taken as a basis for the energy efficiency evaluation during subsequent roller dynamometer tests.

The IDEAS project, due to the implementation by the international consortium, is very complex and many different concepts are developed by all partners. In this paper, only a few aspects of the IDEAS project have been described and as the project is still on foot, the final achievements will be probably presented in further publications after the project completion.

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