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Digital-to-Time Converter for pulse train generation based on Look-Up Tables in FPGA

Abstract

A Digital-to-Time Converter (DTC) is presented which allows to generate pulse train with resolution of 250 ps within 32 ns operation range. The converter is implemented in off-the-shelf Spartan-6 Field-Programmable Gate Array (FPGA) device, manufactured by Xilinx in 45 nm CMOS technology. The design is implemented with the use of Look-Up Tables (LUT) as delay elements. "Manual" Place and Route (P&R) process was involved to improve conversion linearity. Developed DTC can be used to improve the functionality of time interval generators.

Keywords: Digital-to-Time Converter, time interval generator, programmable delay line, programmable devices.

1. Introduction

Precise time interval generators are commonly used in the Automatic Test Equipment (ATE). Their task is to generate patterns of electric pulses that can be used in e.g. semiconductor industry to test integrated chips [1], or time metrology to characterize time counters parameters [2]. Digital-to-Time Converters (DTC) are usually referenced to simple electronic circuits that can be used as a core of the time interval generators. In Field-Programmable Gate Array (FPGA) devices the DTCs or time interval generators can be implemented with the use of built-in dedicated functional blocks for clock management (e.g. Phase-Locked Loop) [3, 4] or delay lines that consist of programmable logic blocks [5, 6]. The dedicated functional blocks greatly facilitate implementation of the device by giving ready-made procedures for frequency synthesis or phase shifting. Moreover, they are relatively high resistant to process, voltage and temperature variations. The delay lines implemented using elements of programmable logic blocks give more design freedom. Thus, unique features can be obtained and, in some cases, better resolution as well [5].Recently proposed DTC implemented in FPGA device [7] has an advantage of pulse train generation with 20 ps resolution. Its design is based on a specific construction of a multi-input delay line in which multiplexers are used as delay elements. The drawback lies in a very short operation range resulting in a strongly restricted number of pulses in a pulse train (up to 3 in [7]). A possible solution to extend the range, at the cost of resolution, is to use a delay line formed with the use of Look-Up Tables (LUTs) instead of a fast carry chain. Such solution is described in this article.

2. Method

The idea of the DTC is presented in Fig. 1. The converter consists of two main parts: a delay line and a pattern register. The delay line consists of 2-input multiplexers. The trigger signal is connected to their selector inputs (S). The data that represents expected shape of the pulse train (i.e. time relation between edges of the pulses) is stored in a digital form (logic states '1' and '0') in the pattern register. This data is fed into multiplexers' inputs A. The delay line is formed by connecting together the outputs (O) and the next multiplexers' inputs (B). The initial signal (Init) is used to set the final state of the pulse train (logic state '0' or '1').

In the idle mode the trigger signal selects inputs A and connect them to the multiplexers' outputs. Thus, the appropriate bits of pattern are passed there. The pulse generation is initialized when trigger logic state switches at the same time all B inputs to the multiplexers' outputs forming the delay line. The logic states from B inputs propagate through the DTC output with the delay proportional to the propagation time of a single multiplexer (τ).

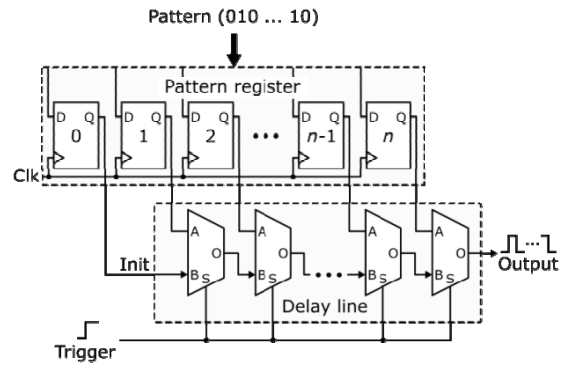

Fig. 1. DTC design

At the moment of pulse train initialization, each B input can be set to different logic states, according to the pattern applied. Therefore, pulse train can be formed at the DTC output with resolution equal to the delay time τ. The DTC with similar construction was used as a pattern generator built-in the wave union based Time-to-Digital Converter (TDC) [8]. The aim of the pattern generator was to produce multiple pulses in a possibly narrow time range. Generally, the more pulses generated, the higher TDC resolution and precision. The pattern was constant and the pulse train was fed directly into another delay line, that was a part of the TDC. In contrast, the DTC presented in this article creates programmable pulse train in relatively wide range.

3. Implementation

The DTC was implemented in a Spartan-6 FPGA device (*Xilinx*). A key element that determines described converter parameters is the way of delay line implementation inside programmable logic. The best way to get the highest delay line resolution is to use so called carry multiplexers. Originally, they are made to perform fast arithmetic operations in the FPGA devices. However, due to their unique feature (shortest propagation time among all FPGA resources), they have been used for many years to implement high resolution delay lines [6, 9]. Thus, in the first approach of the method described in [7], the carry multiplexers were used in the DTC providing 20 ps time resolution. The shortest propagation time can be achieved only when subsequent carry elements are placed in a single column of the basic Spartan-6 programmable elements (called Slices). The length of the column depends on FPGA device size. The relatively small Spartan-6 device (*xc6slx9*) contains only 256 carry elements in a series. Taking into account a short propagation time of the carry multiplexers (20 ps) the DTC operation range is strongly limited. In the mentioned work [7] obtained operation range was less than 5 ns. One way to overcome this limitation is to use other delay elements.

A typical way to implement combinational logic in FPGA is to use LUT. The LUT content is determined during programming process. While operating, its inputs serve as an address to the content. Thus, multiplexers are typically implemented in the FPGA using LUTs. Each Spartan-6 Slice contains 4 LUTs which can be combined using interconnect resources (connecting paths between programmable elements).Connecting paths play an important role

for LUT-based delay line resolution and therefore it has to be taken carefully into consideration at routing stage.

The implementation of the carry elements is facilitated by the software. The software design library includes CARRY4 primitive. When it is connected to another element of its kind the software automatically places them in consecutive Slices of a single column. The build of the delay line using LUTs, as applied in this work, is much more difficult. To have full control over such delay line the FPGA designer has to initialize LUT primitive with proper content. Then, the primitives have to be manually placed possibly close to each other. That would give repeatable results of the implementation between project compilations but still do not ensure the best possible resolution. The compiler automatically locate 4 LUTs in consecutive sides of the Slice (sides A, B, C and D) and then tries to establish inter connections. However, better results can be obtained by manual choosing of the Slice's sides for each LUT element according to the shortest connection paths between them. The manual P&R includes also selecting at which of 6 LUT inputs the particular multiplexer port should be connected. The whole procedure is time consuming but allows to get much better delay line resolution than automatic Place and Route (P&R) process execution.

Finally, in this work the delay line was composed of 128 LUTs that were manually P&R. The trigger signal was distributed with the use of a global clock network. The clock network ensures low skew signal which is needed for proper operation of the DTC. Fig. 2 presents visualization of an FPGA layout with LUTs' sides realignment and without it. In the second case some paths are not connected optimally. They cross two switching matrixes which results in longer path propagation time.

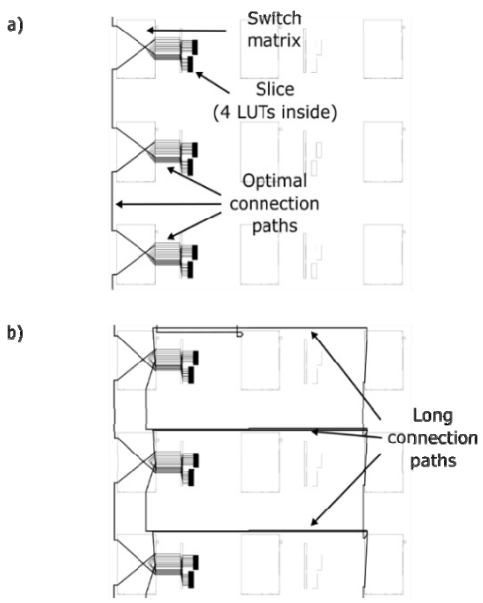

Fig. 2. DTC implementation with (a) and without (b) LUTs' sides realignment

4. Experimental study

The DTC was implemented in Spartan-6 (*xc6slx9*)FPGA device and utilized in time interval generator TIG101 [2]. The TIG 101 is equipment with a highly-stable clock signal of 50 MHz frequency. This clock was divided by 10 inside FPGA and distributed through global clock network as a trigger signal to the DTC. The output of DTC and the divided trigger signal (5 MHz clock) were applied to two channels of a high performance oscilloscope DSA90804A (*Keysight*). Both the DTC and the oscilloscope were controlled by a dedicated application running on a PC computer. The oscilloscope measured the mean value and the standard deviation from about 1000 samples of selected time intervals (e.g. delay between the trigger and DTC output pulses) This test setup was used to examine DTC operation to generate absolute delay (in relation to the trigger signal) and to generate pulse trains.

In the beginning, the second pattern bit was set to high logic state while other bits remained low. Thus, one short pulse was generated. This pulse propagated through 127 delay multiplexers, so it defines the maximum absolute delay to the trigger signal. By changing consecutive bits in the pattern register to logic '1', the pulses width was enlarged and the delay to the trigger was decreased. The first and the last (129th) pattern bits remained low to get rising and falling edges of the generated pulse. Finally we get 126 delay steps. The step sizes were tested for DTC project with and without LUTs' sides realignment. The result is shown in Fig. 3.

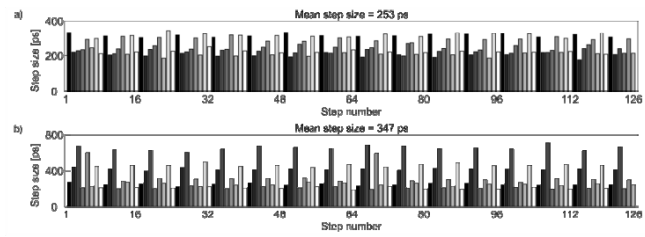

Fig. 3. DTC step sizes with (a) and without (b) LUTs' sides realignment

The use of bin realignment allowed to improve the DTC resolution by about 27% (from 347 ps to 253 ps). In both cases some repeatability of the step sizes can be seen. It comes from the DTC structure – each 8 delay multiplexers are implemented in the same manner and duplicated. The 126 delay steps with 253 ps mean resolution result in almost 32 ns operation range of the DTC for absolute delay generation.

While the delay line length can be further extended for even longer operation range the other problem appears. Due to differences in propagation time for low-to-high (t_{pLH}) and high-to-low (t_{pHL}) transitions the pulses that propagate through the delay line change their width. The effect is commonly known as a pulse shrinking or stretching [9, 10]. The longer the delay line, the stronger the effect. In the faster carry chain-based DTC [7] this effect has minor impact. However, it plays an important role in the presented design and it is perfectly seen during the pulse train generation.

Fig. 4 presents pulse train generated by applying following pattern: 0x0 E1830100 80100100 04000400 00800002. First eight pulses, starting from the right, are generated by setting a single pattern bit into high logic state. Hence, a single pulse should be generated with the width from 200 ps to 350 ps, depending on the step number selected. However, the more delay elements to pass, the wider the pulse width at the DTC output. For example, the first pulse, after passing 126 carry multiplexers, is stretched from about 0.3 ns to 5.5 ns. This issue increases difficulties in DTC control and gives extra restriction for pulses widths.

Fig. 4. The longest pulse train generated by the designed DTC (11 pulses within 38 ns range)

In the last experiment pulse-pair generation was tested. One pulse was generated by setting last six bits of pattern to 011110b. Then, the other bits were subsequently changed to high logic state (the pattern was changed from 0x0 F000-0002 to 0x0 F07F-FFFE). As a result, two pulses were observed in the oscilloscope – one with constant width and the latter whose width was changed. While the width was increasing the rising edge of the second pulse was approaching the first one. The time interval between two rising edges was measured. Fig. 5 presents the obtained time intervals (ΔT) and its jitter.

The longest time interval is generated when both pulses are generated on the opposite side of the delay line. Hence, the second pulse has to pass more delay elements to get the DTC output. Each LUT-based delay multiplexer has significant impact on the time interval jitter. This correlation is much stronger than in the carry chain based DTC [7]. The reason for this is the use of much longer connecting paths that includes witch matrixes. After about 110 elements the jitter is on the level of 10 ps while in the best case it is of about 3.3 ps. The minimum and maximum time intervals achieved in the design were 2.5 ns and 32.7 ns, respectively. Similar experiment in the DTC [7] revealed that the width of the first pulse was depending on the latter one. The presented design has the advantage that the first pulse remains stable with the width of 1.287 ns ±3 ps.

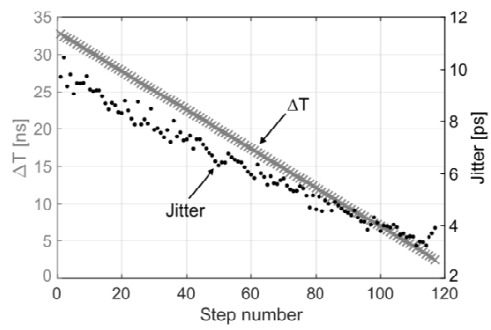

Fig. 5. Time interval between two generated pulses (ΔT) and its jitter

5. Conclusion

The LUT-based DTC is presented that has a unique feature of pulse train generation. The design is implemented in a Spartan-6 FPGA device. The use of LUTs result in 32 ns DTC's operation range and 250 ps delay resolution. In comparison to [7] the device allows to generate up to 11 pulses. The experimental study shows that the presented solution is strongly vulnerable to pulse stretching effect. That makes it difficult to control the device and obtain high performance. Finally, the length of the presented DTC delay line has to be carefully selected to get a tradeoff between the obtained operation range, time interval jitter and the DTC control difficulty.

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