A simplified control strategy for single-phase UPS inverters

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Abstract. Though there are many strategies to control single-phase uninterruptible power supply (UPS) inverters, they suffer from some drawbacks, the main being complexity. This paper proposes a simple dual-loop controller for the single-phase UPS inverter with the LC filter. The suggested control scheme uses the capacitor current as the feedback signal in the inner current loop. No fictitious phase generation or reference frame transformations are required, and simple proportional gains are employed as both voltage and current regulators. A feedforward of the derivative of the output voltage is also proposed, which significantly improves the performance of the closed loop control system. Then, based on the model of the inverter with the proposed control strategy, a simple and systematic design procedure is presented. Finally, the theoretical achievements are supported by extensive simulations.

Key words: single-phase UPS, multi-loop feedback, feedforward.

1. Introduction

Uninterruptible power supply systems (UPSs) are traditionally utilized to provide reliable as well as high quality electricity for critical loads. Recently, due to ever increasing use of dispersed energy storage systems, such as fuel cells, compressed air energy storage devices and flywheels, and more availability of renewable energy sources, such as wind and photovoltaic generators, single-phase UPS inverters have found wide application in supplying local electric power networks. In these applications, UPS inverters are intended to supply the loads with regulated and high quality electric power.

There are many control schemes for single-phase UPS inverters. Most recent advances include digital control strategies such as repetitive control [1–4], dead-beat control [5–7], and discrete-time sliding mode control [8–11]. Digital repetitive control offers excellent ability to eliminate periodic disturbances. On the other hand, slow dynamics, poor tracking accuracy, large memory requirement, and poor performance in response to non-periodic disturbances are the main limitations of this technique. Dead-beat and sliding mode controllers exhibit excellent dynamic performance in direct control of the instantaneous inverter output voltage. However, they suffer from some drawbacks, such as complexity, sensitivity to parameter variations and loading conditions, and non-zero steady-state error. The proportional-resonant (PR) control can successfully eliminate the steady-state error associated to the tracking problem of ac signals. This technique has been also employed to control the instantaneous voltage of single-phase UPS inverters [12–14]. Although simple to implement, some disadvantages have been associated with the PR control, the mains being exponentially decaying response to step changes, and great sensitivity and possibility of instability to the phase shift of sensed signals [15]. The synchronous reference frame proportional-integral (SRFPI) control is also proposed in [16–18]. In the SRFPI control, electrical signals are all transformed to the synchronous reference frame, where quantities are dc and, as a consequence the zero steady-state error is ensured by using a conventional PI regulator. Besides the need for several reference frame transformations, the SRFPI requires at least two orthogonal signals, so a fictitious second phase signal which is shifted in phase 90 electrical degrees regarding to the real signal, must be generated.

In industrial applications, usually, LC smoothing filters are used to effectively mitigate the harmonic contents of the inverter output waveforms. However, an ideally loss-less LC circuit is highly susceptible to resonances with harmonic components generated by the inverter. Yet, it is possible to employ a single loop instantaneous voltage regulator along with a damping resistor in the filter circuit, it is more advantageous to use a dual-loop control to improve the system stability and dynamic performance and at the same time actively damp the resonance oscillations. Depending on the inner loop feedback variable and the type of controllers, several dual-loop control schemes have been proposed [4, 8, 16–24]. The dual-loop control for the single-phase UPS inverter includes an outer voltage loop which regulates the output voltage and ensures zero steady-state error and stability over a wide range of operating conditions and an inner current control loop which compensates the load disturbances and actively damps the possible resonances. It is shown that regardless of the controller type, in dual-loop techniques, the capacitor current feedback brings better disturbance rejection capability than the inductor current feedback [18, 19].

This paper proposes a simple dual-loop controller for the single-phase UPS inverter with an LC filter. The suggested control scheme uses the capacitor current as the feedback signal in the inner current loop. No fictitious phase generation or reference frame transformations are required. Besides, simple proportional gains are employed as both voltage and current regulators. A feedforward of the derivative of the output volt-

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age is also proposed which significantly improves the performance of the closed loop control system. Section 2 presents the dual-loop controller with voltage feedforward and derives a simplified mathematical model for the inverter based on the proposed control strategy. Using this model, Sec. 3 presents a simple and effective design procedure for the voltage and current controllers. In Sec. 4 the theoretical achievements are supported by extensive simulations. Finally, Sec. 5 concludes the paper.

2. Dual-loop control of single-phase UPS inverters

Figure 1a shows the configuration of a single-phase UPS inverter which is connected to an *AC* load with impedance Z through the LC filter. The parameters of the converter circuit are summarized in Table 1. The equivalent series resistance (ESR) of the filter capacitor is ignored, since it is usually such small that the break frequency becomes much higher than the range of concern. Assuming that the switching frequency is far above the fundamental frequency, Fig. 1b shows the averaged switching model of the inverter with the LC filter. In this block-diagram, $v_i(s)$ and $v_o(s)$ are the averaged converter output voltage and the load voltage, respectively. Here, the PWM modulator is assumed to be an ideal unity gain. The load impedance, Z, can be a combination of resistive, inductive, capacitive, or even nonlinear ac loads.
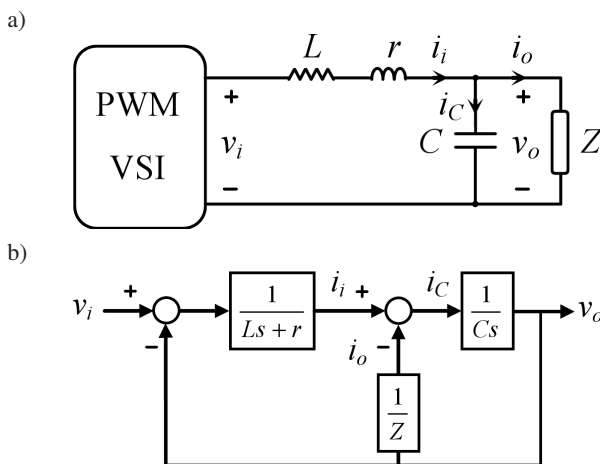
a)

b)

Fig. 1. Single-phase UPS inverter: a) power circuit, b) block-diagram representation

Table 1
System parameters

Parameter	Description	Value
L	filter inductance	500 μH
r	inductor filter resistance	0.2 Ω
C	filter capacitance	220 μF
f	fundamental frequency	60 Hz
f_s	switching frequency	20 kHz
V_{dc}	DC-link voltage	300 VDC

As aforementioned, in all dual-loop control schemes suggested for the single-phase UPS inverters, the inner and outer loops are used for current and voltage control, respectively [4, 8, 16–24]. While these techniques exhibit an acceptable performance, the design of the feedback control loops is complicated. However, it is shown in [25] that if the dual-loop feedback control is augmented with feedforwards of the derivative of the reference voltage and the output current, then simple proportional gains for the current and voltage controllers can eliminate the steady-state voltage tracking error and provide robustness to the load disturbances. Despite the fact that it seems interesting, this technique suffers from major drawbacks that prohibit its use for practical applications, the main being the need for two current sensors (i_o, and i_i), imposed extra calculations including the derivative of the output current, and the necessity of an exact estimation of the output filter parameters (L, r, and C) to realize the controller. So, it is less convincing that this method is simpler than others.

The block diagram of the proposed dual-loop control system with only the voltage feedforward is presented in Fig. 2. Compared to the method of [25], the proposed technique has only one feedforward path and only measures the capacitor current. It is simpler and definitely more cost effective to sense the capacitor current instead of the higher ampere inductor and/or output currents. Also, no information about the inductor parameters and the derivative of the output current are required. The idea of the proposed dual-loop control of the output voltage of the UPS inverter with an LC filter in the output stage involves an outer and an inner regulation loop. The outer loop tracks the reference signal with a zero steady-state error while the inner loop ensures a fast dynamic compensation for disturbances and stability over a wide range of operating conditions. To further improve the UPS system performance, disturbance feedforward compensation is also included in the proposed scheme.

At first, assume that the feedforward path (dashed line) is not present. It is a simple task to obtain the output voltage transfer function from the block diagram of Fig. 2:

$$v_o = \frac{k_i k_v}{LCs^2 + k_i Cs + k_i k_v + 1} v_{o,ref}$$
$$- \frac{Ls}{LCs^2 + k_i Cs + k_i k_v + 1} i_o, \tag{1}$$

where k_i and k_v are the gains of simple proportional current and voltage regulators, respectively, and the effect of inductor resistance is neglected. However it is possible to use PI controllers, they cause unwanted phase delay in the sinusoidal references and only complicate the controller design. By using simple proportional controllers, the phase delay problem is prevented and the system analysis and controller design are significantly simplified. However, in the outer voltage regulation loop, this leads to a high proportional gain to considerably reduce the steady-state error. As it will be shown, the voltage feedforward path in the proposed strategy solves the problem.
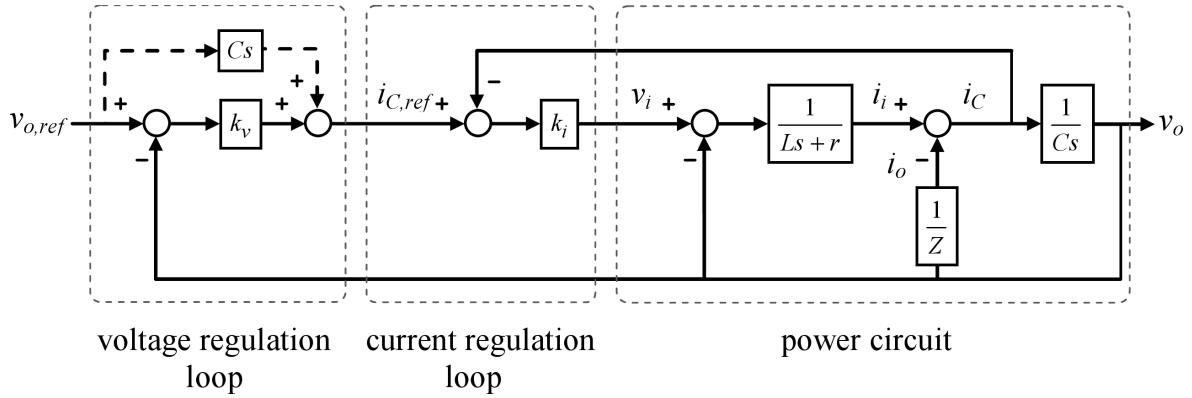
Fig. 2. Block diagram of the proposed dual-loop control system

It is obvious from (1) that the steady-state error of the output voltage is composed of two components: the static tracking error (first term in the right hand side of (1)) and the error caused by i_o variations (second term in the right hand side of (1)). From the control point of view, the product of loop gains $k_i k_v$ must be selected large enough to significantly reduce the steady-state error. For an arbitrary large $k_i k_v$ a perfect tracking of reference voltage, a perfect blocking of load disturbances and a near instantaneous dynamic response would be achieved. Indeed, with this assumption, the transfer function (1) simplifies to:

$$v_o \cong v_{o,ref}. \tag{2}$$

As mentioned before, the inner current control loop is responsible for fast compensation for load disturbances and providing near instantaneous damping for possible resonances caused by the LC filter at the output stage of the converter. So, the current regulator gain, k_i, is practically preferred to be large. However, the choice of the outer voltage loop gain, k_v, is a trade-off between the attainable voltage dynamic response and the overall control loop stability. In practice, to ensure stability over a wide range of operating conditions, k_v should not be too large.

So, if one assumes that k_i is large enough while k_v may not be, the transfer function (1) becomes:

$$v_o \cong \frac{k_v}{Cs + k_v} v_{o,ref}. \tag{3}$$

As it can be seen, an amplitude as well as phase error in the output voltage is expected. To obtain a zero steady-state error, the transfer function (3) must take the following form:

$$v_o \cong \frac{Cs + k_v}{Cs + k_v} v_{o,ref} = v_{o,ref}. \tag{4}$$

From the block diagram algebra, this can be conveniently achieved by adding a feedforward path from $v_{o,ref}$ with a gain of Cs, as highlighted in Fig. 2 with dashed lines. With this feedforward path, the transfer function of output voltage becomes:

$$v_o = \frac{k_i(Cs + k_v)}{LCs^2 + k_iCs + k_ik_v + 1} v_{o,ref} \\ - \frac{Ls}{LCs^2 + k_iCs + k_ik_v + 1} i_o. \tag{5}$$

The Bode diagrams of $v_o/v_{o,ref}$ of transfer functions (1) and (5) are plotted in Fig. 3 for $k_i = 100$ and $k_v = 0.1$. The steady-state phase and magnitude errors at the fundamental frequency, the phase margins (PMs), and the closed-loop bandwidths (BWs) are also compared in Table 2. As expected, the steady-state error is considerably reduced and the closed-loop bandwidth is increased resulting in a faster dynamic response. The stability is not affected by the feedforward path, because it does not affect the closed-loop pole locations. Indeed, the controller with the feedforward is unconditionally stable, since (5) exhibits a positive phase margin (assuming that $k_v > 0$) as shown in (6), in which ω_c is the open loop gain cross-over frequency.

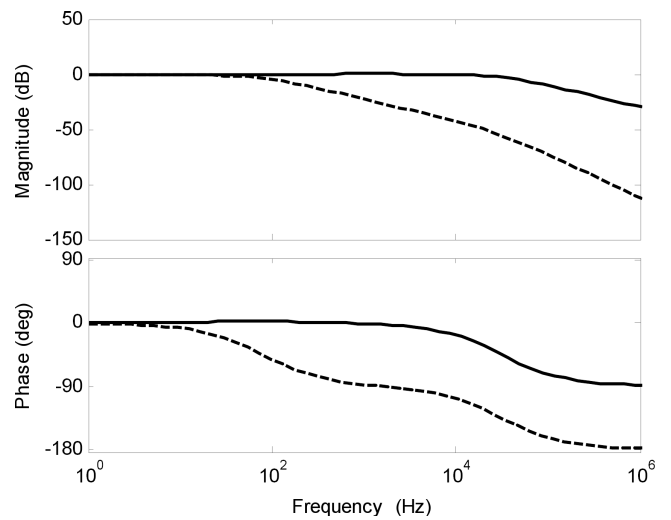$$PM = \arctan\left(\frac{C\omega_c}{k_v}\right) > 0 \tag{6}$$

Fig. 3. Bode plots of $v_o/v_{o,ref}(s)$ with (solid line) and without (dashed line) the voltage feedforward

Table 2
Performance comparison of dual-loop controller with and without the voltage feedforward

	Magnitude error [%]	Phase error [deg]	PM [deg]	BW [Hz]
without feedforward	28	−37	95	80
with feedforward	5	2	90	37000

3. Controller parameters design

Under light loads, the phase margin and the closed loop stability are slightly reduced. Physically, under no-load or light load conditions, the lightly damped characteristic of the output filter can cause a sharp reduction in the open loop phase and, consequently, reduce the phase margin. As a result, controllers are normally designed under light-load condition in order to ensure the fulfillment of stability requirements. Hence, the closed-loop transfer function of (5) under no-load condition can be rewritten as:

$$\frac{v_o}{v_{o,ref}} = \frac{k_i(Cs + k_v)}{LCs^2 + k_iCs + k_ik_v + 1}$$

$$= \frac{\dfrac{k_i}{L}s + \dfrac{k_ik_v}{LC}}{s^2 + \dfrac{k_i}{L}s + \dfrac{k_ik_v + 1}{LC}}. \tag{7}$$

Assuming that $k_ik_v \gg 1$ the above equation can be approximated by a standard second-order transfer function:

$$\frac{v_o}{v_{o,ref}} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \tag{8}$$

where $\zeta = \frac{1}{2}\sqrt{\frac{k_iC}{k_vL}}$ and $\omega_n = \sqrt{\frac{k_ik_v}{LC}}$ are the damping factor and the natural frequency, respectively.

There are numerous publications attending the properties and discussing different design aspects of the standard transfer function of (8). Though a damping factor, ζ, of $1/\sqrt{2}$ is recommended in literature, to select the natural frequency, one

has to make a compromise between the control bandwidth (and consequently the transient response) and the disturbance rejection capability. In this application, ω_n is chosen to be $2\pi 2$ krad/s, which is one-tenth the switching frequency and ensures the switching noise immunity. Based on these selections, the controller parameters are calculated as:

$$\begin{cases} k_i = 2\zeta\omega_nL \cong 10 \\ k_v = \frac{C\omega_n}{2\zeta} \cong 2 \end{cases}.$$

4. Performance evaluation

To confirm the effectiveness of the proposed control strategy, the single-phase inverter system was developed in MATLAB/Simulink. System parameters are summarized in Table 1. Practical effects such as regular sampling with 20 kHz frequency, non-ideality of IGBT switches, and dead-time delays are included in simulations to emulate the real system performance as closely as possible. The steady-state performance was investigated by simulating the UPS behavior at various loading conditions and the results are shown in Figs. 4–6. The effect of load power factor on the steady-state output voltage and current waveforms is depicted in Fig. 4, which relieves that the proposed system can successfully produce a perfect sinusoidal voltage with minimum total harmonic distortion (THD = 0.08%) at resistive, and highly inductive or capacitive loading conditions. Figure 5 shows the effect of varying the switching frequency on the THD of the output voltage.
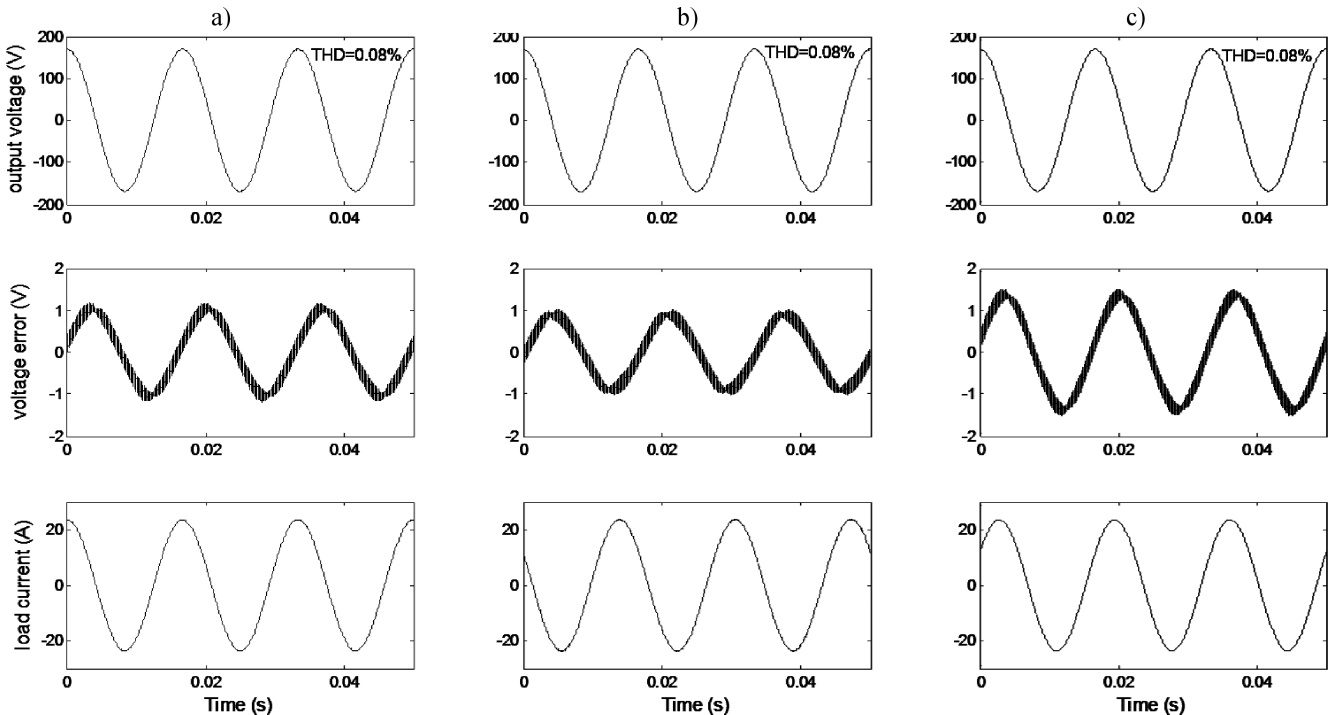

Fig. 4. Steady-state waveforms under (a) unity, (b) 0.5 leading, and (c) 0.5 lagging power factor load
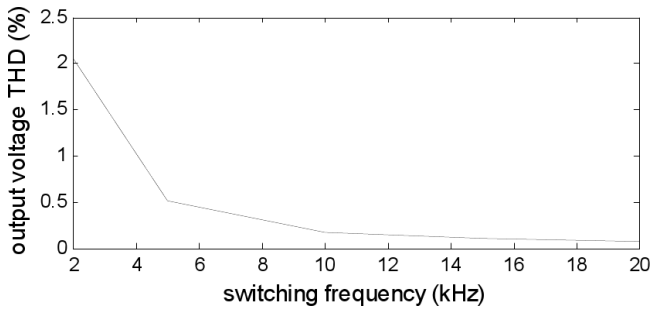
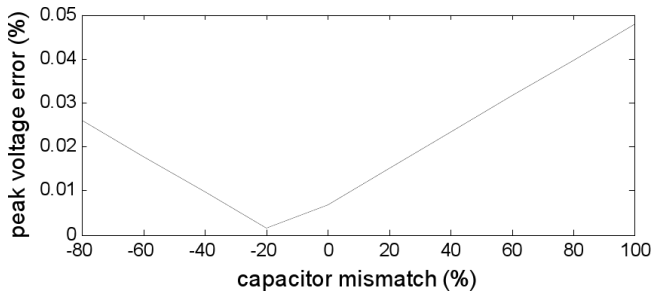Fig. 5. Effect of switching frequency on the output voltage THD

Fig. 6. Effect of capacitor mismatch on the peak output voltage error

It can be seen that the proposed controller keeps very low THD even for low switching frequency operation. Also, it was investigated that the variations of the load impedance magnitude have almost no effect on the output voltage THD.

As evident in Fig. 2, the operation of proposed feedforward voltage control depends on the capacitor value. Therefore, the performance of the converter system considering mismatch in the capacitance value is investigated and results are summarized in Fig. 6. It can be seen that, however the peak voltage error remains almost negligible, the lowest error occurs for -20% mismatch not for zero mismatch. This small deviation is a result of including practical effects, such as sampling and PWM delays, non-ideality of switches, and dead-time delays, in the simulations which are not included in the small-signal model of the converter system.

Figure 7 shows the performance of the proposed control scheme under nonlinear load conditions. The nonlinear load is a diode rectifier bridge feeding a series R-L or a parallel R-C circuit. One can see in Fig. 7 that while the load current is highly distorted, the output voltage waveform remains sinusoidal. This promising behavior is a consequence of providing enough control bandwidth (about 2 kHz). Figure 8a shows the transient performance for 100% step change in the load from no-load to full load and then removing it. The UPS system offers a very fast transient response with excellent output voltage regulation from no-load to full load and vice versa. Only a little change in the output voltage can be observed at the instance of applying the full load, indicating that the proposed control technique brings a stiff output voltage. Figure 8b shows the dynamic performance at the start-up and the shutdown. Clearly, the converter response to step changes of reference voltage is almost instantaneous with negligible transients.
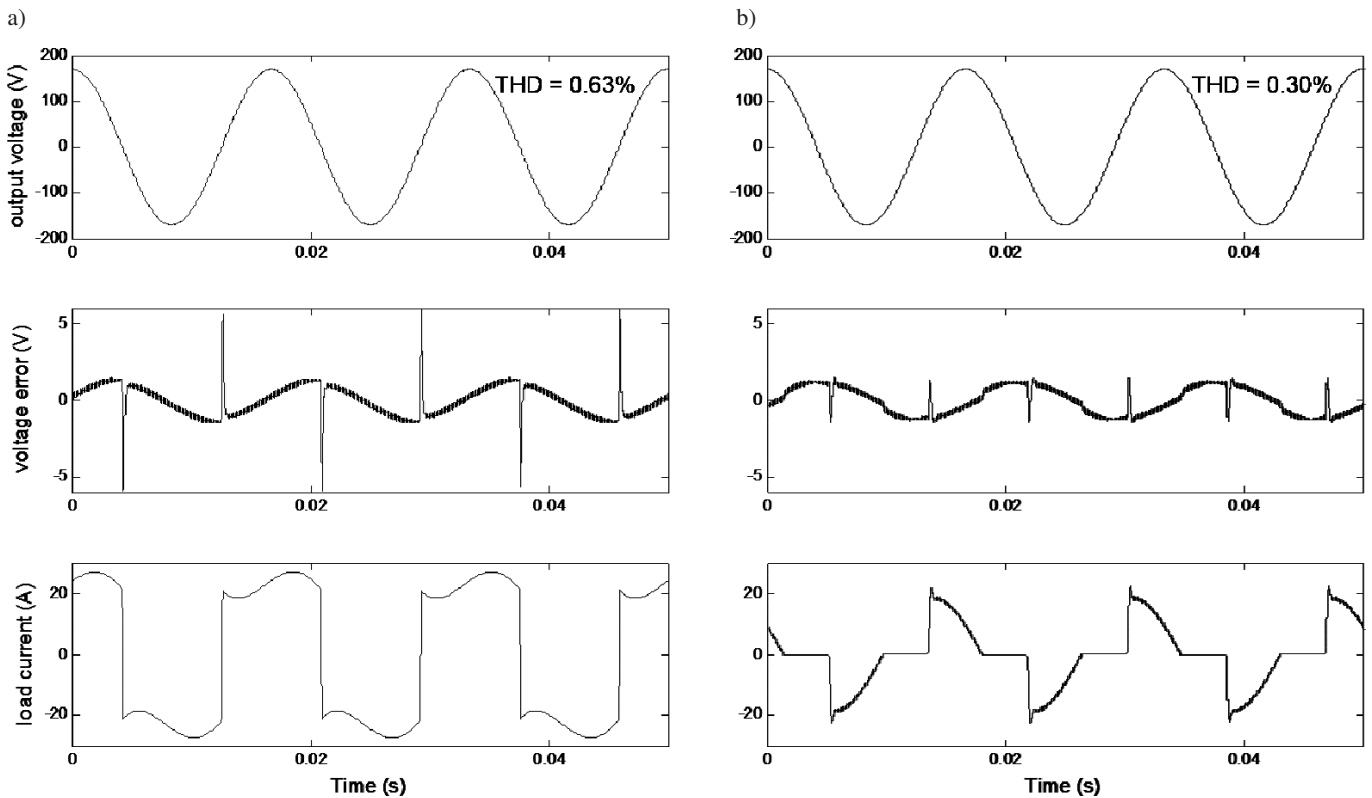
a)

b)

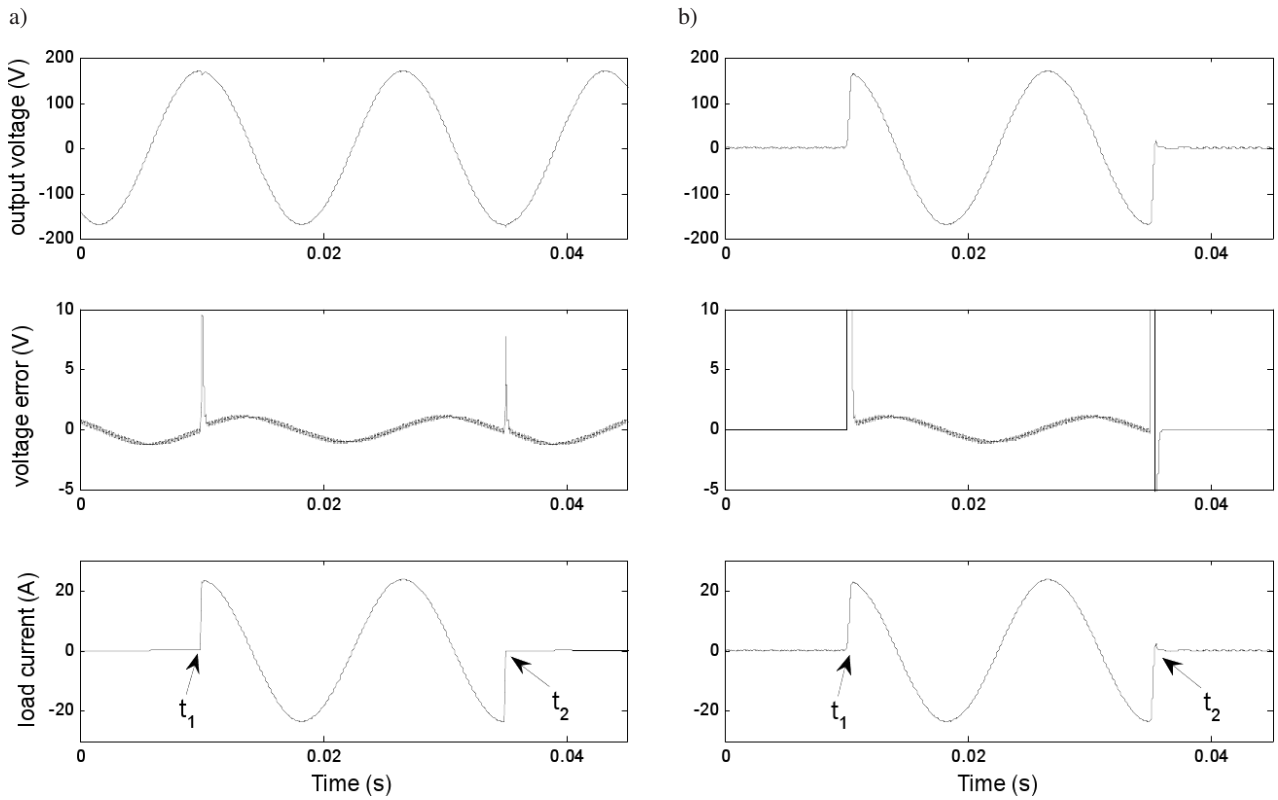Fig. 7. Steady-state waveforms for a full bridge rectifier load with a) a series R-L load, and b) a parallel R-C load

a)

b)

Fig. 8. Transient waveforms: a) 100% application (at t_1) and 100% removal (at t_2) of load, and b) 100% jump (at t_1) and 100% fall (at t_2) of reference voltage
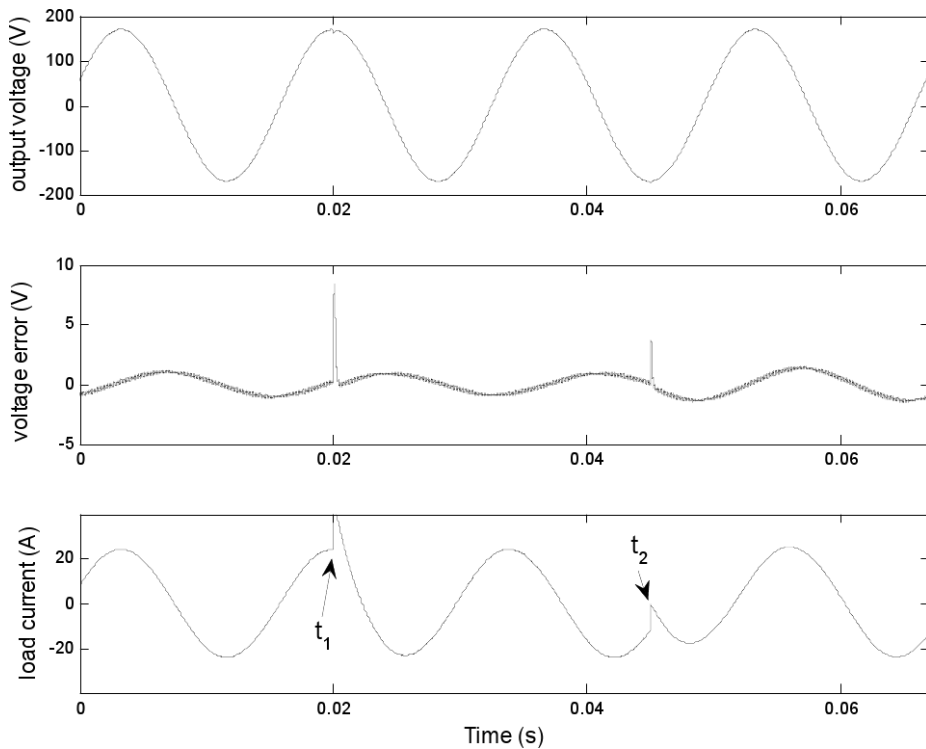

Fig. 9. Transient waveforms in response to the load power factor step change from unity to 0.5 leading (at t_1) then to 0.5 lagging (at t_2)

Transient response to the load power factor step change from unity to 0.5 leading and then to 0.5 lagging is depicted in Fig. 9. Again an excellent transient performance is attained following a considerable phase shift in the load current.

5. Conclusions

This paper has proposed a simple dual-loop feedback controller with a feedforward path to regulate the instantaneous output voltage of the single-phase UPS inverter. The feedback controller ensures stability, active damping, and improves disturbance rejection, while the feedforward path boosts the tracking performance. Based on the model of the inverter with the proposed control strategy, a straightforward design procedure has been suggested. The performance of the proposed control strategy has been confirmed through extensive simulations.

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