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New Aspects of Fault Diagnosis of Nonlinear Analog Circuits

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***Abstract*—The paper is focused on nonlinear analog circuits, with the special attention paid to circuits comprising bipolar and MOS transistors manufactured in micrometer and submicrometer technology. The problem of fault diagnosis of this class of circuits is discussed, including locating faulty elements and evaluating their parameters. The paper deals with multiple parametric fault diagnosis using the simulation after test approach as well as detection and location of single catastrophic faults, using the simulation before test approach. The discussed methods are based on diagnostic test, leading to a system of nonlinear algebraic type equations, which are not given in explicit analytical form. An important and new aspect of the fault diagnosis is finding multiple solutions of the test equation, i.e. several sets of the parameters values that meet the test. Another new problems in this area are global fault diagnosis of technological parameters in CMOS circuits fabricated in submicrometer technology and testing the circuits having multiple DC operating points. To solve these problems several methods have been recently developed, which employ different concepts and mathematical tools of nonlinear analysis. In this paper they are sketched and illustrated. All the discussed methods are based on the homotopy (continuation) idea. It is shown that various versions of homotopy and combinations of the homotopy with some other mathematical algorithms lead to very powerful tools for fault diagnosis of nonlinear analog circuits. To trace the homotopy path which allows finding multiple solutions, the simplicial method, the restart method, the theory of linear complementarity problem and Lemke's algorithm are employed. For illustration four numerical examples are given.**

***Keywords*—analog circuits, fault diagnosis, local and global diagnosis, multiple soft faults, nonlinear circuits, single hard faults**

I. Introduction

ELECTRONIC circuits diagnosing and testing is an essential area of scientific research. The integrated circuit manufacturing process in imperfect, and as a result defects are introduced into some of the fabricated chips. Discovering whether an integrated circuit operates in accordance with its specifications and its parameters are within their tolerance ranges is a key question of integrated circuits design. The testing of electronic circuits represents up to 70 % of the total product cost. It is estimated that the testing of the analog components of the mixed-signal integrated circuits contributes up to 90 % of the total cost. On the other hand analog testing lags far behind digital testing. Although the problem has been of considerable interest during the past decades [1]–[5], [7]–[8], [10]–[19], [21]–[32], [35]–[38] there is no all-purpose procedure for fault diagnosis of analog circuits. In 2013 the data base SCOPUS registered 99 papers devoted to testing and diagnosing of analog circuits, including 46 journal articles. There are several reasons which make fault diagnosis of analog circuits difficult. In modern fabrication process only a very limited number of nodes is accessible for measurement and excitation, the values of fault-free elements are distributed within their tolerance ranges and some circuit elements form ambiguity groups.

Much work in fault testing and diagnosing exploits some heuristic methods, artificial neural networks, different evolutionary techniques, support vector machines, and elements of fuzzy logic [1]–[4], [10]–[15], [17]–[18]. Some researches concentrate on self-testing of analog circuitry of mixed-signal systems using built-in self test blocks [7], [37]–[38]. Most attention in fault diagnosis has been paid to fault detection and location of a single fault in linear circuits using a fault dictionary. Fewer results relate to the multiple fault diagnosis in nonlinear circuits where several parameters are faulty [8], [26], [29], [31]–[32], [35]. A fault can be catastrophic (hard) if it leads to some topological changes or parametric (soft) if a parameter is drifted from its tolerance range. Parametric faults may be global or local. Local variations of the parameters are due to local defect mechanisms or local variations in parameters across a chip. Global variations in parameters are due to imperfect control in integrated circuits manufacturing. They arise due to statistical fluctuations in process parameters such as oxide thickness, doping, line width, and mask misalignment. Such variations affect all transistors and capacitors on a chip. If most of circuit simulations take place before any testing the diagnostic method is classified as the simulation-before-test (SBT) approach. Otherwise, the method is classified as the simulation-after-test (SAT) approach.

Some of diagnostic methodologies exploit a system of nonlinear test equations of algebraic type with unknown parameters. If the parameters are slightly drifted from their nominal values the equations can be linearized which simplifies the diagnosis. Unfortunately, such approach is not allowed if the parameters deviate considerably from their nominal values and the equations are strongly nonlinear. In such a case several sets of the parameters can meet the test because the system of nonlinear equations may actually possess multiple solutions. Most algorithms are generally capable of finding only one solution (one set of the parameter values), even if the system of nonlinear equations possesses several solutions. However, finding just one specific solution, which is not necessarily the actual one, is rarely of interest. Finding the actual set of the parameters in such cases is a very difficult task, particularly in circuits manufactured in submicrometer technology, due to

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very complex models of the devices. E.g., BSIM 4 model of MOS transistors is described by approximately 300 equations, mostly nonlinear. In such a case the test equation cannot be presented in explicit analytical form.

This paper is focused on nonlinear analog circuits, with the special attention paid to circuits comprising BJ and MOS transistors manufactured in micrometer and submicrometer technology. New aspects of fault diagnosis of this class of circuits are discussed and some recently obtained results in this area presented. They include: multiple soft fault diagnosis of nonlinear circuits considering the problem of existing multiple solutions of the test equations, hard fault diagnosis of circuits possessing multiple operating points, and global fault diagnosis of CMOS circuits.

II. Diagnostic Test

The diagnostic methods described in this paper are based on a diagnostic test. For the circuit comprising parameters considered as possibly faulty the test is arranged as in [29], [31]–[32]. The circuit under test is driven by the power supply voltage sources $v_s^{(1)}, \ldots, v_s^{(w)}$ applied at the nodes accessible for excitation and the output voltages $v_1, \ldots, v_r$ are read at r nodes accessible for measurement (see Fig. 1). For m sets of the input voltages values $\left\{v_s^{(1)}, \ldots, v_s^{(w)}\right\}_i$ $(i = 1, 2, \ldots, m)$ mr values of the output voltages are measured, where $mr \geq n$, where n is the number of parameters considered as possibly faulty. We take n of the voltages and consider them as elements of the vector $\mathbf{u} = [u_1 \cdots u_n]^{\mathrm{T}}$, where T means transposition. Each of the voltages is a certain function of the circuit parameters $x_1, \ldots, x_n$, $u_i = \widehat{f}_i(\mathbf{x})$, $i = 1, 2, \ldots, n$, where $\mathbf{x} = [x_1 \cdots x_n]^{\mathrm{T}}$. As a result we write the equation

$$\widehat{\mathbf{f}}\,(\mathbf{x}) = \mathbf{u}\,, \tag{1}$$

where $\widehat{\mathbf{f}}\,(\mathbf{x}) = \left[\widehat{f}_1(\mathbf{x}) \cdots \widehat{f}_n(\mathbf{x})\right]^{\mathrm{T}}$. This equation will be presented in the form

$$\mathbf{f}\,(\mathbf{x}) = \mathbf{0}\,, \tag{2}$$

where $\mathbf{f}\,(\mathbf{x}) = \widehat{\mathbf{f}}\,(\mathbf{x}) - \mathbf{u}$, and called a test equation. When the parameters assume the prescribed values $\left\{x_1^{dn}, \ldots, x_n^{dn}\right\}$ the measured voltages are labeled $\left\{u_1^{dn}, \ldots, u_n^{dn}\right\}$. In such a case the equation

$$\widehat{\mathbf{f}}\left(\mathbf{x}^{dn}\right) = \mathbf{u}^{dn} \tag{3}$$

holds, where $\mathbf{x}^{dn} = [x_1^{dn} \cdots x_n^{dn}]^{\mathrm{T}}$, $\mathbf{u}^{dn} = [u_1^{dn} \cdots u_n^{dn}]^{\mathrm{T}}$. The aim of the fault diagnosis of analog circuits is finding the parameters $x_1, \ldots, x_n$ considered as possibly faulty, that meet the diagnostic test equation (2). Solving this task the following restrictions must be taken into account.

- In real nonlinear circuits function $\widehat{\mathbf{f}}\,(\mathbf{x})$ is not given in explicit analytical form.
- Nonlinear test equation (2) may possess multiple solutions, what means that more than one set of the parameters $\{x_1, \ldots, x_n\}$ meet the diagnostic test.

Several diagnostic methods considering the above-mentioned requirements are discussed in this paper. All the methods exploit the homotopy concept [9], [20]. This is why the next section gives a background of the homotopy method.

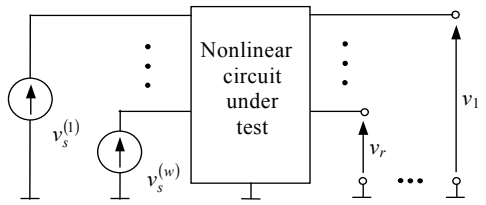

Fig. 1. Arrangement of a diagnostic test

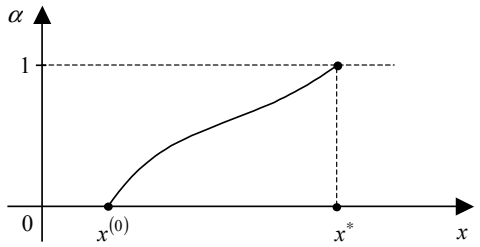

Fig. 2. A regular homotopy path

III. Concept of Homotopy

Homotopy is a powerful tool for studying many problems of nonlinear analysis [9]. In this paper it is shown that the homotopy is very useful in fault diagnosis of nonlinear analog circuits. Below the background and underlying concept of the homotopy are briefly described.

Let us consider a system of nonlinear algebraic equations

$$\begin{aligned} f_1(x_1, \ldots, x_n) &= 0\,, \\ &\vdots \\ f_n(x_1, \ldots, x_n) &= 0\,, \end{aligned} \tag{4}$$

where $x_1, \ldots, x_n$ are unknown variables forming vector $\mathbf{x} = [x_1 \cdots x_n]^{\mathrm{T}}$. The set of equations (4) can be written in the compact form

$$\mathbf{f}\,(\mathbf{x}) = \mathbf{0}\,, \tag{5}$$

where $\mathbf{f}\,(\mathbf{x}) = [f_1(\mathbf{x}) \cdots f_n(\mathbf{x})]^{\mathrm{T}}$. Let $\mathbf{x} = \mathbf{x}^*$ be a solution of this equation. To find the solution we create the homotopy equation

$$\mathbf{h}\,(\mathbf{x}, \alpha) = \mathbf{0}\,, \tag{6}$$

where $\alpha \in [0, 1]$ is called a homotopy parameter. At $\alpha = 0$ equation $\mathbf{h}\,(\mathbf{x}, 0) = \mathbf{0}$ has known or easy to finding solution $\mathbf{x}^{(0)}$, whereas at $\alpha = 1$ equation (6) becomes the original equation (5) possessing the solution $\mathbf{x}^*$, which we seek. The main idea of the homotopy is increasing parameter α, starting with $\alpha = 0$ and every time solving equation (6), taking into account the solution obtained in previous step. If increment of α is small, it is justified to expect that the solution will slightly changed going from one step to the other. To find the new solution the Newton-Raphson algorithm can be used, starting with the previous solution. As a result a path is traced that we can follow from $\alpha = 0$ to $\alpha = 1$, thereby solving the original equation (5) as shown in Fig. 2. The point of intersection of the homotopy path with the line $\alpha = 1$ determines the solution $\mathbf{x}^*$. The most common homotopies are specified below.

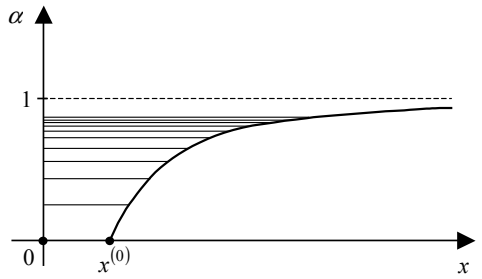

Fig. 3. An exemplary homotopy path

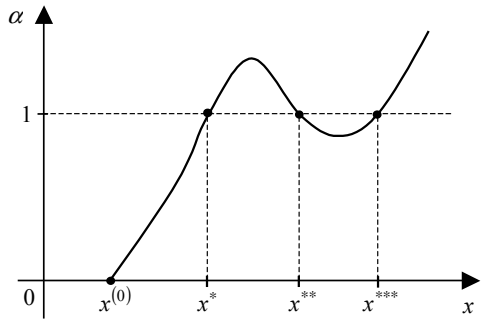

Fig. 4. Homotopy path leading to three solutions

Newton homotopy:

$$\mathbf{h}\left(\mathbf{x},\alpha\right)=\mathbf{f}\left(\mathbf{x}\right)-\left(1-\alpha\right)\,\mathbf{f}\left(\mathbf{x}^{(0)}\right)\ , \tag{7}$$

where $\mathbf{x}^{(0)}$ is an arbitrary n-dimension vector.

Fixed-point homotopy:

$$\mathbf{h}\left(\mathbf{x},\alpha\right)=\left(1-\alpha\right)\left(\mathbf{x}-\mathbf{x}^{(0)}\right)+\alpha\,\mathbf{f}\left(\mathbf{x}\right)\ , \tag{8}$$

where $\mathbf{x}^{(0)}$ is an arbitrary n-dimension vector.

Linear homotopy:

$$\mathbf{h}\left(\mathbf{x},\alpha\right)=\alpha\,\mathbf{f}\left(\mathbf{x}\right)+\left(1-\alpha\right)\,\mathbf{g}\left(\mathbf{x}\right)\ , \tag{9}$$

where $\mathbf{g}\left(\mathbf{x}\right)$ is a function possessing a known solution $\mathbf{x}^{(0)}$.

It should be emphasized that the homotopy path is not necessarily the regular curve as shown in Fig. 2. In some cases it can be infinite spiral or a bifurcation curve what makes difficulty to apply the homotopy method. Figure 3 shows a homotopy path whose tracing requires systematic decreasing of the increment of parameter α. As a result the number of the required analyses increases dramatically and the method is inefficient.

The described above variant of the homotopy method is called a discrete homotopy. Continuous version of this method is obtained by differentiating of homotopy equation (6) with respect to parameter α and solving numerically the initial value problem

$$\frac{\partial\mathbf{h}\left(\mathbf{x},\alpha\right)}{\partial\mathbf{x}}\,\frac{\mathrm{d}\mathbf{x}}{\mathrm{d}\alpha}+\frac{\partial\mathbf{h}\left(\mathbf{x},\alpha\right)}{\partial\alpha}=\mathbf{0}\ ,\quad \mathbf{x}(0)=\mathbf{x}^{(0)} \tag{10}$$

in interval $[0,1]$.

In both variants of the standard homotopy method parameter α is systematically increased from 0 to 1. However, the method can be extended as follows. Parameter α is considered similarly as the variables $x_1,\ldots,x_n$ and homotopy path is traced in more sophisticated manner. In such a case the range of changing of parameter α is not limited to $\alpha=1$, what allows finding multiple solutions of equation (5). This is illustrated in Fig. 4, where the homotopy path leads to three solutions $\mathbf{x}^{*}$, $\mathbf{x}^{**}$, and $\mathbf{x}^{***}$.

IV. Fault Diagnosis Using the Parametric Homotopy

This section discusses multiple soft fault diagnosis of nonlinear circuits, with the special attention paid to the circuits comprising bipolar and MOS transistors manufactured in micrometer technology. To solve the test equation a method based on the parametric homotopy will be used. The details of this method are presented in reference [29].

Let us consider equation (2) repeated below

$$\mathbf{f}\left(\mathbf{x}\right)=\widehat{\mathbf{f}}\left(\mathbf{x}\right)-\mathbf{u}=\mathbf{0}\ .$$

Using the Newton homotopy (7) we write the homotopy equation

$$\mathbf{h}\left(\mathbf{x},\alpha\right)=\widehat{\mathbf{f}}\left(\mathbf{x}\right)-\mathbf{u}-\left(1-\alpha\right)\ \left[\widehat{\mathbf{f}}\left(\mathbf{x}^{(0)}\right)-\mathbf{u}\right]\ , \tag{11}$$

where $\mathbf{x}^{(0)}$ is a vector consisting of the parameters having nominal values. Under the denotation $\mathbf{x}^{(0)}=\mathbf{x}^{dn}$ the equation $\widehat{\mathbf{f}}\left(\mathbf{x}^{(0)}\right)=\mathbf{u}^{dn}$ holds (see (3)). Substituting this equation into (11) yields

$$\mathbf{h}\left(\mathbf{x},\alpha\right)=\widehat{\mathbf{f}}\left(\mathbf{x}\right)-\mathbf{u}^{dn}-\alpha\ \left(\mathbf{u}-\mathbf{u}^{dn}\right)=\mathbf{0}\ . \tag{12}$$

To find vector $\mathbf{u}^{dn}$ we perform numerical analysis of the circuit, with nominal values of the parameters, driven by the same sources as in the test. For $\alpha=0$ homotopy equation (12) becomes $\widehat{\mathbf{f}}\left(\mathbf{x}\right)-\mathbf{u}^{dn}=\mathbf{0}$. It is satisfied by vector $\mathbf{x}=\mathbf{x}^{dn}$ whose elements have nominal values. At $\alpha=1$ equation (12) is identical to the test equation.

Denote $\alpha=x_{n+1}$ and form vector $\widehat{\mathbf{x}}=[x_1\cdots x_n,x_{n+1}]^{\mathrm{T}}$. Then the homotopy equation (12) becomes

$$\widehat{\mathbf{h}}\left(\widehat{\mathbf{x}}\right)=\widehat{\mathbf{f}}\left(\mathbf{x}\right)-\mathbf{u}^{dn}-x_{n+1}\ \left(\mathbf{u}-\mathbf{u}^{dn}\right)=\mathbf{0}\ . \tag{13}$$

As $x_{n+1}=\alpha$ varies starting from $x_{n+1}=0$, the homotopy path is traced. Let us parametrize the path with respect to the arc length s [29]. Then

$$\mathrm{d}s=\sqrt{(\mathrm{d}x_1)^2+\cdots+(\mathrm{d}x_n)^2+(\mathrm{d}x_{n+1})^2}\ . \tag{14}$$

Using the parameterization we form the set of equations

$$\widehat{\mathbf{h}}\left(\widehat{\mathbf{x}}\right)=\mathbf{0}\ ,\qquad \sum_{i=1}^{n+1}\left(\frac{\mathrm{d}x_i}{\mathrm{d}s}\right)^2=1 \tag{15}$$

consisting of $n+1$ individual equations. The derivative $\frac{\mathrm{d}x_i}{\mathrm{d}s}\left(s_{j+1}\right)$ can be expressed in terms of $x_i\left(s_{j+1}\right)$ and $x_i\left(s_j\right)$ using the approximate formula

$$\frac{\mathrm{d}x_i}{\mathrm{d}s}\left(s_{j+1}\right)=\frac{1}{h}\left(x_i\left(s_{j+1}\right)-x_i\left(s_j\right)\right)\ ,\quad i=1,\ldots,n+1\ , \tag{16}$$

where $h = s_{j+1} - s_j$. Substituting (16) into (15) yields

$$\begin{bmatrix} \widehat{h}_1\left(\widehat{\mathbf{x}}(s_{j+1})\right) \\ \vdots \\ \widehat{h}_n\left(\widehat{\mathbf{x}}(s_{j+1})\right) \\ \sum_{i=1}^{n+1}\left[x_i\left(s_{j+1}\right) - x_i\left(s_j\right)\right]^2 - h^2 \end{bmatrix} = \mathbf{0}\,. \qquad (17)$$

Solution of the algebraic equation (17) is a point of the homotopy path at $s = s_{j+1}$.

Denote the left hand side of equation (17) by $\mathbf{w}\left(\widehat{\mathbf{x}}\left(s_{j+1}\right)\right)$. Then this equation can be presented in the compact form

$$\mathbf{w}\left(\widehat{\mathbf{x}}\left(s_{j+1}\right)\right) = \mathbf{0}\,. \qquad (18)$$

To find $\widehat{\mathbf{x}}\left(s_{j+1}\right)$ we apply the Newton-Raphson method. At each iteration $m+1$ $(m = 0, 1, \ldots)$ the vector $\mathbf{w}\left(\widehat{\mathbf{x}}^{(m)}\left(s_{j+1}\right)\right)$ and the Jacobian matrix $\frac{\mathrm{d}\mathbf{w}}{\mathrm{d}\mathbf{x}}\left(\widehat{\mathbf{x}}^{(m)}\left(s_{j+1}\right)\right)$ have to be calculated. For this purpose $f_k\left(\mathbf{x}^{(m)}\left(s_{j+1}\right)\right)$ and $\frac{\partial f_k}{\partial x_l}\left(\mathbf{x}^{(m)}\left(s_{j+1}\right)\right)$ $(k, l = 1, \ldots, n)$ are required. This is untrivial problem because, the function $\widehat{\mathbf{f}}\left(\mathbf{x}\right)$ is not given in explicit analytical form. To overcome this drawback we set the known values of the parameters $x_i = x_i^{(m)}\left(s_{j+1}\right)$ $(i = 1, \ldots, n)$ and perform the DC and the sensitivity analyses of the circuit driven by the input voltages as in the test, finding $f_k\left(\mathbf{x}^{(m)}\left(s_{j+1}\right)\right)$ and $\frac{\partial f_k}{\partial x_l}\left(\mathbf{x}^{(m)}\left(s_{j+1}\right)\right)$, $(k, l = 1, \ldots, n)$. an appropriate procedure was developed in reference [29], where also the problem of changing the step size h during the computations was solved. The step size should be decreased to a very small value, when the solution varies very fast and should be increased to a larger value when the solution changes slowly. During the computation process the homotopy parameters is selected automatically, similarly as the other variables. Its value can increase or decrease reaching several times the value equal to one, leading to multiple solutions of the test equation. Having several solutions (sets of the parameters) we select these ones which satisfy some physical constraints and discard the others, e.g. containing negative resistances. If more than one solution remain, including the correct solution and virtual ones, then under the applied test they possess equal rights. To determine the actual solution a different test should be arranged and the common set selected. In some cases the method gives just one set of the parameters.

Example 1: Let us consider the bipolar circuit shown in Fig. 5 [29]. Three elements R_3, R_6, R_7 are faulty (more than 50 %) and values of the others are within their tolerance ranges. The values of all the circuit elements are as follows: $R_1 = 278\,\mathrm{k\Omega}$, $R_2 = 22.6\,\mathrm{k\Omega}$, $R_3 = 20\,\mathrm{k\Omega}$, $R_4 = 6.95\,\mathrm{k\Omega}$, $R_5 = 2.78\,\mathrm{k\Omega}$, $R_6 = 100\,\Omega$, $R_7 = 100\,\Omega$, $\beta_1 = 385$, $\beta_2 = 391$. We consider the set of all resistors $R_1, \ldots, R_7$ as possibly faulty. The proposed method gives two sets of the parameters which satisfy the test, including the actual one. The homotopy path is closed, its projection on α-R_3 plane is shown in Fig. 6. The points of intersection of the curve with the vertical line $\alpha = 1$ correspond to two values of the resistance R_3.

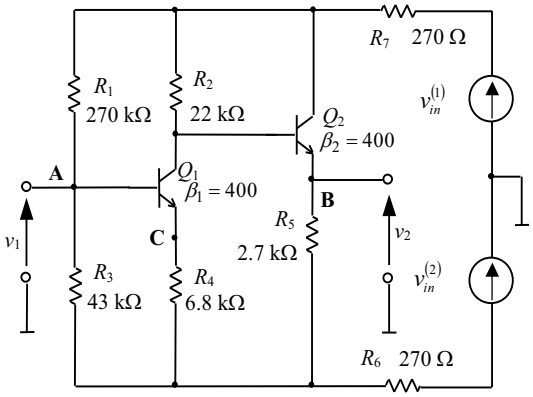

Fig. 5. Circuit for Example 1

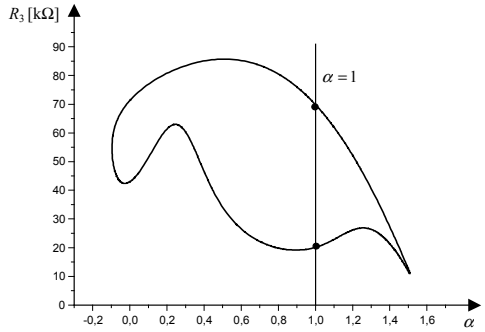

Fig. 6. Projection of the homotopy path on α-R_3 plane

V. Global Fault Diagnosis of Analog CMOS Circuits Manufactured in Submicrometer Technology

Global variations of parameters are due to imperfect control in IC manufacturing. They arise due to statistical fluctuations in process parameters such as oxide thickness, doping, line width, and mask misalignment. Such variations affect all transistors, resistors, and capacitors on a die. In CMOS circuits the parameters chosen most frequently are: threshold voltage @ $V_{bs} = 0$ for large L — V_{th_0}, channel width — W, channel length — L, mobility — U_0, channel doping — N_{ch}, and oxide thickness — t_{ox} for n and p-channel transistors separately. Most of the works in this area have been devoted to the local parametric fault diagnosis due to local defect mechanisms or local variations in parameters across a die. Only a few papers discuss the global parametric fault diagnosis. To tackle that problem the nonlinear regression modeling techniques [5], the artificial neural network [13], and the differential evolution [14] were used. A new approach to the problem of global fault diagnosis is proposed in reference [31], based on the homotopy concept and the simplicial method [9]. This section brings the idea of this approach.

Let us consider the circuits comprising short-channel MOS transistors, characterized by the model BSIM3v3. To use the MOSIS BSIM3 parameters in IsSPICE 4, the nominal geometric specifications L_{nom} and W_{nom}, for each device in net list are corrected and assume the values L_{drawn} and W_{drawn},

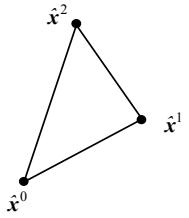

Fig. 7. An exemplary 2-simplex

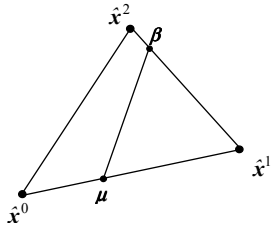

Fig. 8. An approximation $\boldsymbol{\mu\beta}$ of homotopy path on the simplex s

respectively. The deviations of L and W defined for the process corners are labelled DXL and DXW, respectively. Consequently, variations of the channel length and width can be specified by the equations $L = L_{\text{drawn}} + (1 - x_L)\, DXL$ and $W = W_{\text{drawn}} + (1 - x_W)\, DXW$, where x_L and x_W are auxiliary relative parameters. Similarly, variations of the V_{th_0} can be specified by the equation $V_{th_0} = (V_{th_0})_{\text{nom}} + (1 - x_V)\, DVT$, where DVT is the deviation of V_{th_0} defined for the process corners and x_V is a relative parameter. Variations of the other parameters will be described by the equations: $U_0 = (U_0)_{\text{nom}}\, x_U$, $N_{\text{ch}} = (N_{\text{ch}})_{\text{nom}}\, x_N$, $t_{\text{ox}} = (t_{\text{ox}})_{\text{nom}}\, x_t$, where x_U, x_N, and x_t are relative parameters. Thus, each of the above-mentioned parameters is expressed in terms of the corresponding relative parameter. All the parameters are considered separately for n and p-channel transistors. The global parameters relating to L, W, V_{th_0}, U_0, N_{ch}, t_{ox} are defined as follows: $\Delta L = L - L_{\text{drawn}} = (1 - x_L)\, DXL$, $\Delta W = W - W_{\text{drawn}} = (1 - x_W)\, DXW$, $\Delta V_{th_0} = V_{th_0} - (V_{th_0})_{\text{nom}} = (1 - x_V)\, DVT$, $U_0 = (U_0)_{\text{nom}}\, x_U$, $N_{\text{ch}} = (N_{\text{ch}})_{\text{nom}}\, x_N$, $t_{\text{ox}} = (t_{\text{ox}})_{\text{nom}}\, x_t$. Thus, each of the global parameters is represented by the attached relative parameter. If all six above-mentioned global faults are considered the number of the relative parameters equals twelve, independently on size of the circuit. The set of relative parameters will be presented in the vector form $\mathbf{x} = [x_1 \cdots x_n]^{\mathrm{T}}$. To solve test equation (2) the Newton homotopy method (13) will be used, where x_{n+1} is the homotopy parameter, $\mathbf{u}^{dn}$ is defined by (3) and elements of vector $\mathbf{x}^{dn}$ assume drawn values in the case of L and W or nominal in the case of the other parameters. To generate the homotopy path the simplicial method [9], [31] will be used.

The underlying concept of the simplicial method is the simplex [9]. A j-simplex, written as $s = \left\{\widehat{\mathbf{x}}^0, \widehat{\mathbf{x}}^1, \ldots, \widehat{\mathbf{x}}^j\right\}$, is a convex hull of the $j+1$ independent points $\widehat{\mathbf{x}}^i = \left[x_1^i \cdots x_{n+1}^i\right]^{\mathrm{T}}$, $(i = 0, 1, \ldots, j)$

$$\left\{\mathbf{p}\colon \mathbf{p} = \sum_{i=0}^{j} \lambda_i\, \widehat{\mathbf{x}}^i\ , \quad \sum_{i=0}^{j} \lambda_i = 1\ , \quad \lambda_i \geq 0\right\}\ . \tag{19}$$

The convex hull of some but not all vertices $\widehat{\mathbf{x}}^i$ is called a face of s. In a special case, when the face has j vertices, it is termed a facet. For example 2-simplex is a triangle (see Fig. 7), having three vertices $\widehat{\mathbf{x}}^0, \widehat{\mathbf{x}}^1, \widehat{\mathbf{x}}^2$ and three facets $\left\{\widehat{\mathbf{x}}^0, \widehat{\mathbf{x}}^1\right\}$, $\left\{\widehat{\mathbf{x}}^1, \widehat{\mathbf{x}}^2\right\}$, $\left\{\widehat{\mathbf{x}}^2, \widehat{\mathbf{x}}^0\right\}$. Let $s = \left\{\widehat{\mathbf{x}}^0, \widehat{\mathbf{x}}^1, \ldots, \widehat{\mathbf{x}}^{n+1}\right\}$ be an $(n+1)$-simplex having $n+2$ vertices. Then any point $\mathbf{p} \in s$ can be specified by the equation

$$\left\{\mathbf{p}\colon \mathbf{p} = \sum_{i=0}^{n+1} \lambda_i\, \widehat{\mathbf{x}}^i\ , \quad \sum_{i=0}^{n+1} \lambda_i = 1\ , \quad \lambda_i \geq 0\right\}\ . \tag{20}$$

Consider the homotopy function (13) and approximate it on the simplex s. For this purpose we evaluate $\widehat{\mathbf{h}}\left(\widehat{\mathbf{x}}^i\right)$, $i = 0, 1, \ldots, n+1$ and for given point $\mathbf{p}$ described by (20) form

$$\sum_{i=0}^{n+1} \lambda_i\, \widehat{\mathbf{h}}\left(\widehat{\mathbf{x}}^i\right)\ . \tag{21}$$

To create the homotopy path we consider the function (21) and solve, on the simplex s, the equations

$$\sum_{i=0}^{n+1} \lambda_i\, \widehat{\mathbf{h}}\left(\widehat{\mathbf{x}}^i\right) = \mathbf{0}\ , \quad \sum_{i=0}^{n+1} \lambda_i = 1\ , \quad \lambda_i \geq 0\ . \tag{22}$$

Since (22) is a set of $n+1$ individual equations with $n+2$ variables $\lambda_0, \lambda_1, \ldots, \lambda_{n+1}$, the solution will be a straight-line segment. In the typical case the linear segment will connect a point of one facet of s to other facet as it is illustrated in Fig. 8, where the linear segment $\boldsymbol{\mu\beta}$, connecting point $\boldsymbol{\mu}$ of facet $\left\{\widehat{\mathbf{x}}^0, \widehat{\mathbf{x}}^1\right\}$ to point $\boldsymbol{\beta}$ of the facet $\left\{\widehat{\mathbf{x}}^1, \widehat{\mathbf{x}}^2\right\}$, approximates the real homotopy path on the simplex s.

To perform the simplicial algorithm we take an initial simplex s_0 and trace the straight-line segment across this simplex. Then, we form an adjacent simplex s_1 and trace across it other straight-line segment. In this manner a piecewise-linear homotopy path is created. The process is continued until a termination criterion is satisfied. Any intersection point of the homotopy path and the plane $x_{n+1} = \alpha = 1$ is a solution. An exemplary path is shown in Fig. 9.

The key problems of the simplicial algorithm are:

- creating the initial simplex,
- finding the ending point of the segment inside each simplex,
- creating the adjacent simplex.

To solve these problems appropriate procedures are necessary. They are described in reference [31].

Example 2: Let us consider the circuit shown in Fig. 10 comprising 18 MOS transistors characterized by BSIM3v3. We consider the possible global faults of channel length L and threshold voltage V_{th_0} different for PMOS and NMOS.

Using the test described in [31], the method gives two different sets of the parameters, the actual and the virtual ones. To find the set of actual values of the parameters we arrange other test and select the common part of the sets. The

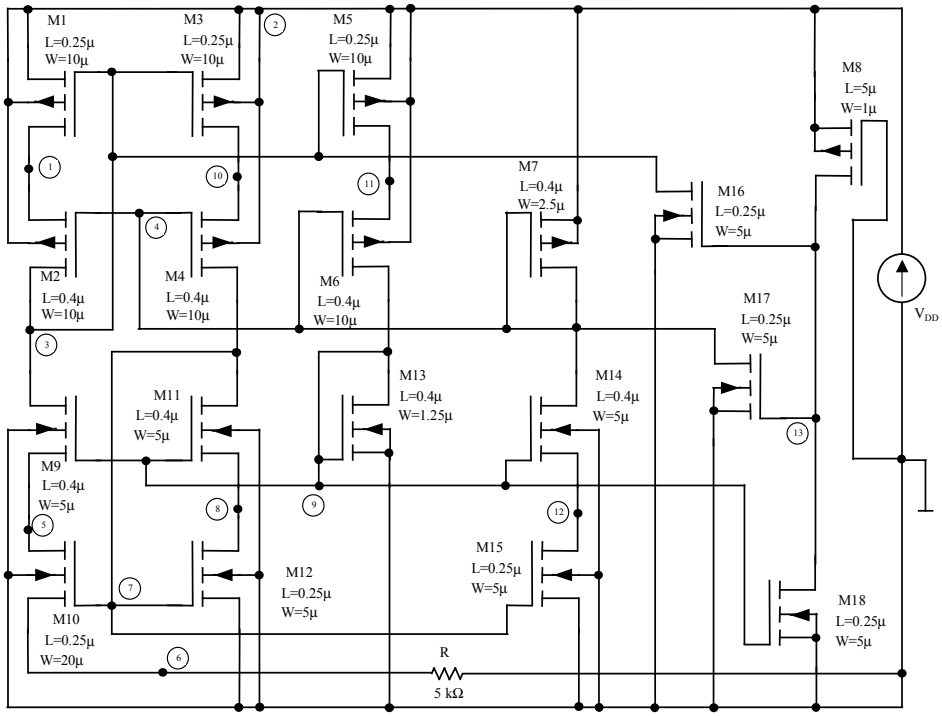

Fig. 10. CMOS circuit for Example 2

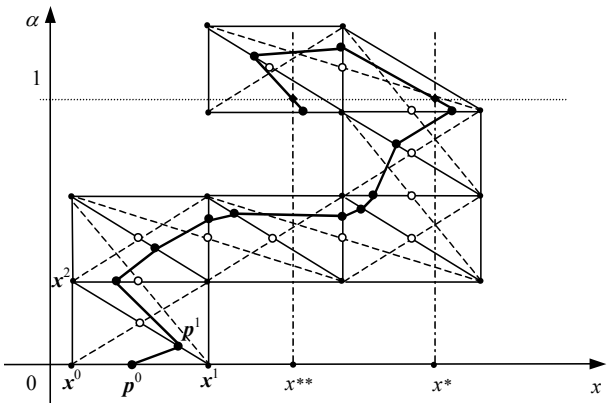

Fig. 9. An exemplary homotopy path leading to solutions $\mathbf{x}^*$ and $\mathbf{x}^{**}$

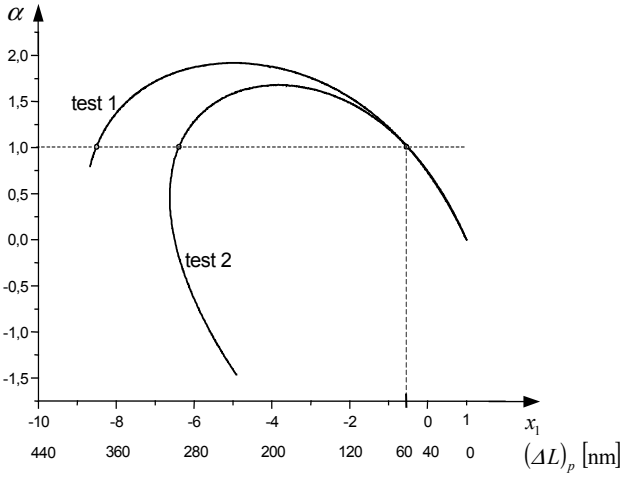

Fig. 11. Projections of the homotopy paths corresponding to the tests 1 and 2 on x_1-α plane

results are illustrated in Fig. 11 and the details are described in reference [31].

VI. Multiple Soft Fault Diagnosis Using Restart Homotopy Method

This section is devoted to multiple soft fault diagnosis of nonlinear circuits containing bipolar and MOS transistors. A method that allows locating faulty elements and evaluating their parameters using a nonlinear test equation which may possess several solutions is described. To find the solutions the homotopy concept is applied and a homotopy differential equation written. Next the terminal value problem is formulated and solved using the restart approach [9]. An extended version of this approach, presented in this section, allows finding different sets of the parameters which satisfy the diagnostic test, rather than one specific set.

To find the solutions of the test equation (2) we form the Newton homotopy equation (7) repeated below

$$\mathbf{h}\left(\mathbf{x},\alpha\right)=\mathbf{f}\left(\mathbf{x}\right)-\left(1-\alpha\right)\mathbf{f}\left(\mathbf{x}^{(0)}\right)$$

and create the homotopy differential equation [32] by differentiating both sides of (7) with respect to α

$$\frac{\partial\mathbf{h}}{\partial\mathbf{x}}\left(\mathbf{x},\alpha\right)\frac{\partial\mathbf{x}}{\partial\alpha}+\frac{\partial\mathbf{h}}{\partial\alpha}\left(\mathbf{x},\alpha\right)=\mathbf{0}\,. \tag{23}$$

Taking into account (7) we present equation (23) in the normal

form

$$\frac{\mathrm{d}\mathbf{x}}{\mathrm{d}\alpha} = -\left[\frac{\mathrm{d}\mathbf{f}}{\mathrm{d}\mathbf{x}}\left(\mathbf{x}\right)\right]^{-1}\mathbf{f}\left(\mathbf{x}^{(0)}\right) . \tag{24}$$

The homotopy differential equation (24) can be solved using the forward Euler algorithm (FEA) as follows

$$\mathbf{x}^{(k+1)} = \mathbf{x}^{(k)} - \left[\frac{\mathrm{d}\mathbf{f}}{\mathrm{d}\mathbf{x}}\left(\mathbf{x}^{(k)}\right)\right]^{-1}\mathbf{f}\left(\mathbf{x}^{(0)}\right)\left(\alpha_{k+1}-\alpha_k\right) \tag{25}$$

with the initial condition $\mathbf{x}\left(0\right) = \mathbf{x}^0$. To avoid finding the inverse of the matrix $\frac{\mathrm{d}\mathbf{f}}{\mathrm{d}\mathbf{x}}\left(\mathbf{x}^{(k)}\right)$ we rewrite equation (25) in the form

$$\left[\frac{\mathrm{d}\mathbf{f}}{\mathrm{d}\mathbf{x}}\left(\mathbf{x}^{(k)}\right)\right]\left(\mathbf{x}^{(k+1)}-\mathbf{x}^{(k)}\right) = -\mathbf{f}\left(\mathbf{x}^{(0)}\right)\left(\alpha_{k+1}-\alpha_k\right) . \tag{26}$$

To find $\mathbf{x}^{(k+1)}$ the linear algebraic equation (26) has to be solved. For this purpose we can use the Gaussian elimination method. Thus, the FEA (26) enables us to go very fast from one step to the other. Unfortunately, the local truncation error of this algorithm is quite large and its numerical stability poor. Hence, the step size $(\alpha_{k+1}-\alpha_k)$ must be chosen very small, which leads to large number of steps and long CPU time. If the step size is not sufficiently small the FEA gives a numerical solution which drifts away from the exact solution. This is why the FEA is seldom used to solve the initial value problem. Our problem, however, is of a different sort, namely a terminal value problem [9], i.e. we are interested in calculating the terminal point $\mathbf{x}^*$ at $\alpha = 1$. In such a case there is no need to stay on the precise solution path, but end up at $\mathbf{x}^*$. For this purpose we adapt the restart method [9] as follows. We apply the FEA (26) with a reasonable step size $(\alpha_{k+1}-\alpha_k)$ and at any step check if $\left\|\mathbf{h}\left(\mathbf{x}^{(k)},\alpha_k\right)\right\| < \varepsilon$, where ε is a small positive number selected on the basis of many numerical experiments. If this condition is fulfilled the procedure is continued, otherwise we do not attempt to get back on the original path, but form a new homotopy, called the restart homotopy [9]. Suppose that for some $k = l_1$ the condition $\left\|\mathbf{h}\left(\mathbf{x}^{(l_1)},\alpha_{l_1}\right)\right\| < \varepsilon$ is violated. Then we create the restart homotopy

$$\mathbf{h}_{l_1}\left(\mathbf{x},\alpha\right) = \mathbf{f}\left(\mathbf{x}\right) - \frac{1-\alpha}{1-\alpha_{l_1}}\,\mathbf{f}\left(\mathbf{x}^{(l_1)}\right) . \tag{27}$$

Next we create the homotopy differential equation and apply the FEA. As a result we obtain the following equation

$$\left[\frac{\mathrm{d}\mathbf{f}}{\mathrm{d}\mathbf{x}}\left(\mathbf{x}^{(k)}\right)\right]\left(\mathbf{x}^{(k+1)}-\mathbf{x}^{(k)}\right) = = -\frac{1}{1-\alpha_{l_1}}\,\mathbf{f}\left(\mathbf{x}^{(l_1)}\right)\left(\alpha_{k+1}-\alpha_k\right) . \tag{28}$$

We solve this equation starting with the initial point $\alpha = \alpha_{l_1}$, $\mathbf{x} = \mathbf{x}^{(l_1)}$ and every time check whether the condition $\left\|\mathbf{h}_{l_1}\left(\mathbf{x}^{(k)},\alpha_k\right)\right\| < \varepsilon$ holds. If at some $k = l_2$ this condition is not fulfilled, which means that the generated point drifts off the new path, the homotopy is restarted again. The procedure is continued and if it is necessary a succeeding restart homotopy is created. When the solution path intersects $\alpha = 1$ plane the corresponding point $\mathbf{x}^*$ is a solution. Since we search for other possible solutions the approach is further performed.

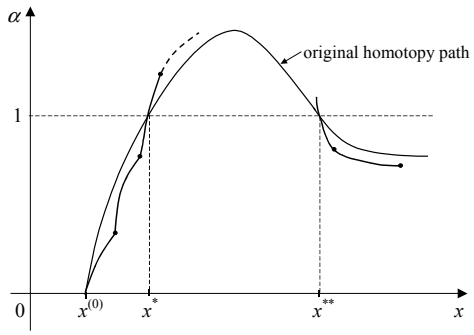

Fig. 12. Illustration of the restart homotopy

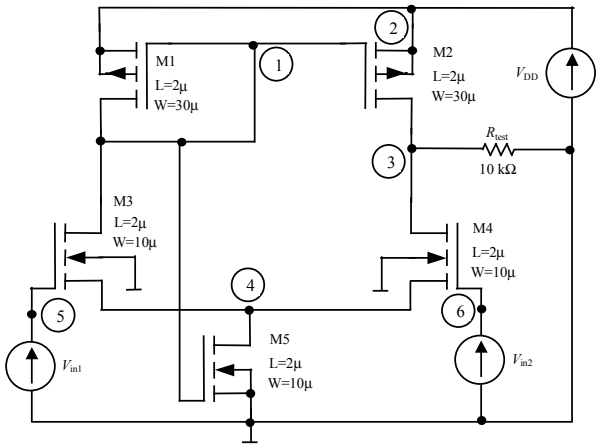

Fig. 13. Circuit for Example 3

We increase α to go far away from the solution point as long as the Newton-Raphson method, used to solve the circuit for given parameters, is convergent. Next the solution path is forced to be reversed and it is checked whether the solution path intersects the plane $\alpha = 1$ again at a different point corresponding to other solution. In such a case a similar procedure is carried out for $\alpha < 1$ and so on. The described approach is terminated when the total number of steps exceeds a preset number $M_{\max}$. Illustrative example of the method is shown in Fig. 12.

Example 3: Let us consider the differential amplifier shown in Fig. 13. The MOS transistors are characterized by the Shichman-Hodges model built up in Level 1 of SPICE, with the parameters indicated in reference [32].

Let the intrinsic transconductance parameters K_p be considered as possibly faulty. To diagnose the circuit the test is performed as described in reference [32]. We consider $5\,\%$ increase of K_p in all PMOS transistors and $10\,\%$ increase of K_p in all NMOS transistors. The proposed method gives two sets of the parameters $\left\{K_p\right\}$, which meet the test. The first set contains the parameters very close to the actual ones, whereas the second set is virtual. Figure 14 shows the projection of the homotopy path on the plane α-K_{p_1}.

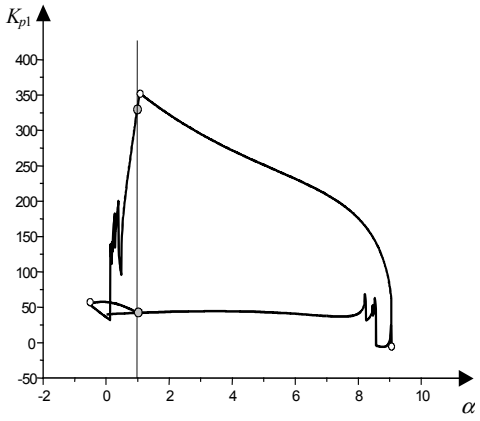

Fig. 14. Projection of the homotopy path on the plane α-K_{p_1}

VII. Catastrophic Fault Diagnosis of the Circuits Having Multiple Operating Points

This section deals, with catastrophic fault diagnosis of nonlinear analog circuits containing bipolar and MOS transistors having multiple operating points (DC solutions). The faults are cuts of some connecting paths and short-circuits of some pairs of points. Simulation-before-test approach is applied for detection and identification of a single catastrophic fault. In the discussed circuits having multiple DC solutions the tested output voltage may assume different values for fixed value of the input voltage. This fact considerably complicates the fault diagnosis. The crucial point of the proposed approach is tracing large number of nonlinear multivalued input-output characteristics at different values of circuit parameters within their tolerance ranges.

Consider a circuit consisting of bipolar transistors, diodes, resistors and voltage sources. The transistors are characterized by the Ebers-Moll model [33], [36] shown in Fig. 15, where $i_{EF} = I_{ES}\left(\exp(v_{d_1}/v_T) - 1\right)$, $i_{CF} = I_{CS}\left(\exp(v_{d_2}/v_T) - 1\right)$. We approximate the exponential characteristics of the diodes included in the model or acting alone using piecewise-linear functions similarly as in [33], [36]. The diode specified by N-segment piecewise-linear characteristic can be modeled by the circuit shown in Fig. 16a including $N-1$ ideal diodes having the characteristic shown in Fig. 16b, where the reversed reference direction of the voltage across the ideal diode is chosen. Then the diode is described by relations

$$i \geq 0\,, \quad v \geq 0\,, \quad iv = 0\,. \tag{29}$$

To trace transfer characteristic $v_0 = f(y)$, where v_0 is the output voltage and y is the input voltage, we extract from the circuit all the ideal diodes, the source y, and the open circuited branch with the output voltage v_0. The last one is replaced by a zero current source and the ideal diodes by voltage sources. As a result an m-port is created as shown in Fig. 17. Using the hybrid representation of the m-port we write

$$\begin{bmatrix} \widehat{\mathbf{i}} \\ \hdashline v_{n+2} \end{bmatrix} = \mathbf{H} \begin{bmatrix} \widehat{\mathbf{v}} \\ \hdashline i_{n+2} \end{bmatrix} + \mathbf{s}\,, \tag{30}$$

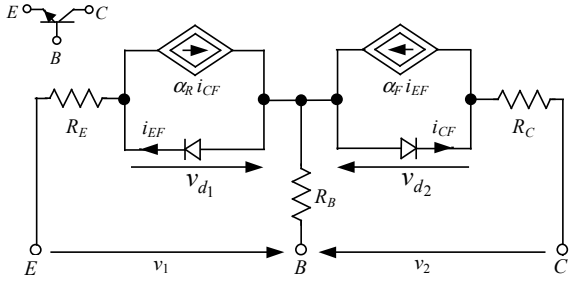

Fig. 15. Ebers-Moll model of npn transistor

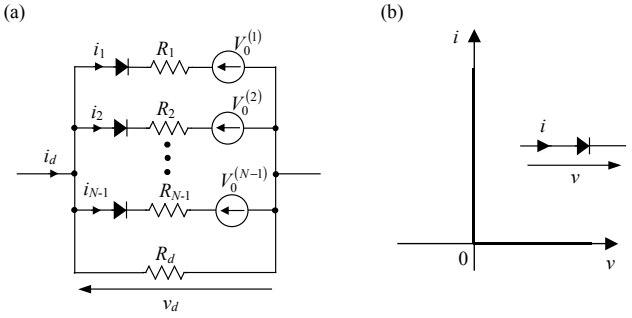

Fig. 16. Diode model (a) and characteristic of the ideal diode (b)

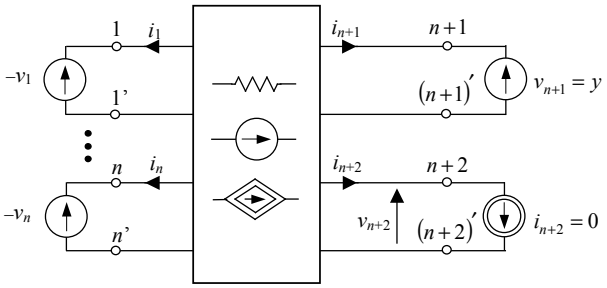

Fig. 17. Rearranged circuit

where

$$\widehat{\mathbf{i}} = \begin{bmatrix} i_1 \\ \vdots \\ i_n \\ \hdashline i_{n+1} \end{bmatrix}\,, \quad \widehat{\mathbf{v}} = \begin{bmatrix} -v_1 \\ \vdots \\ -v_n \\ \hdashline v_{n+1} \end{bmatrix}\,, \quad \mathbf{s} = \begin{bmatrix} s_1 \\ \vdots \\ s_{n+2} \end{bmatrix}\,,$$

and $\mathbf{H} = [h_{ij}]_{(n+2)\times(n+2)}$ is the hybrid matrix. Since $i_{n+2} = 0$ we remove the column $n+2$ of this matrix. Moreover, we remove $(n+1)$-st equation of the hybrid representation, extract $(n+2)$-nd equation and extract the term containing $(n+1)$-st column of $\mathbf{H}$. As a result we obtain

$$\mathbf{i} = \mathbf{M}\mathbf{v} + \begin{bmatrix} h_{1,n+1} \\ \vdots \\ h_{n,n+1} \end{bmatrix} y + \begin{bmatrix} s_1 \\ \vdots \\ s_n \end{bmatrix}\,, \tag{31}$$

$$v_0 = v_{n+2} = -\begin{bmatrix} h_{n+2,1} & \cdots & h_{n+2,n} \end{bmatrix} \mathbf{v} + h_{n+2,n+1}\, y + s_{n+2}\,, \tag{32}$$

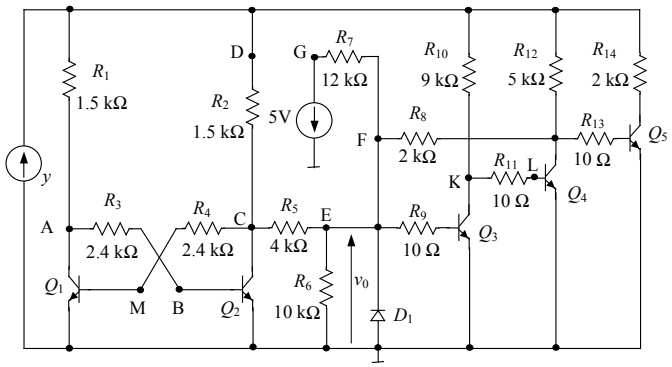

Fig. 18. BJT circuit for an example

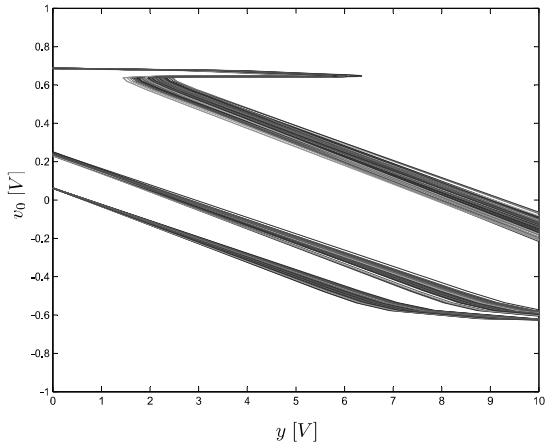

Fig. 19. Banded input-output characteristic

Table F

		Ranges of v_0 variation			
k	y_k	F_0	F_1	. . .	F_M
0	y^-				
1	$y^- + h$				
2	$y^- + 2h$				
.	.	.	.	. . .	.
.	.	.	.	. . .	.
.	.	.	.	. . .	.
N	y^+				

Fig. 20. Structure of table F

where

$$\mathbf{i} = \begin{bmatrix} i_1 \\ \vdots \\ i_n \end{bmatrix}, \ \mathbf{v} = \begin{bmatrix} v_1 \\ \vdots \\ v_n \end{bmatrix}, \ \mathbf{M} = - \begin{bmatrix} h_{11} & \cdots & h_{1n} \\ \cdots & \cdots & \cdots \\ h_{n1} & \cdots & h_{nn} \end{bmatrix}.$$

Letting $\mathbf{z} = [z_1 \cdots z_n]^{\mathrm{T}} = \mathbf{i}$, $\mathbf{x} = [x_1 \cdots x_n]^{\mathrm{T}} = \mathbf{v}$, $\mathbf{b} = [h_{1,n+1} \cdots h_{n,n+1}]^{\mathrm{T}}$, $\mathbf{q} = [s_1 \cdots s_n]^{\mathrm{T}}$ we rewrite equation (31) in the form

$$\mathbf{z} = \mathbf{q} + \mathbf{b}y + \mathbf{M}\mathbf{x} \, . \tag{33}$$

Since for each ideal diode the relations (29) must be fulfilled we can write

$$\mathbf{x} \geq \mathbf{0} \, , \quad \mathbf{z} \geq \mathbf{0} \, , \quad \mathbf{z}^{\mathrm{T}}\mathbf{x} = 0 \, , \tag{34}$$

where the inequalities are meant componentwise. To trace the multi-branched characteristic $v_0 = f(y)$ for $y \in [0, Y]$ we use the algorithm developed in reference [36]. At first we set $y = 0$ and write on the basis of (33) and (34)

$$\begin{aligned} &\mathbf{z} = \mathbf{q} + \mathbf{b} \cdot 0 + \mathbf{M}\mathbf{x} \, , \\ &\mathbf{x} \geq \mathbf{0} \, , \quad \mathbf{z} \geq \mathbf{0} \, , \quad \mathbf{z}^{\mathrm{T}}\mathbf{x} = 0 \, . \end{aligned} \tag{35}$$

The problem specified by (35) is called a linear complementarity problem (LCP) [6], [9], [33], [36]. To solve this problem we combine the homotopy concept with Lemke's method as described in [9], [33]. This approach allows finding several solutions at $y = 0$. Similarly we find the solutions at $y = Y$. The main step of the algorithm is creating new homotopies starting with the found solutions with the homotopy parameter $\alpha = y$, as described in [36]. To build a fault dictionary the algorithm is applied to trace a family of the characteristics for various parameters values from their tolerance ranges. E.g., the family of the characteristics in the circuit shown in Fig. 18 is depicted in Fig. 19.

For fault-free circuit and for each circuit with a single fault we trace a family of the input-output characteristics $v_0 = f(y)$. If the number of the considered faults is M we obtain $M + 1$ families of the characteristics. Each of the families has banded branches like the characteristic depicted in Fig. 19. We choose an interval $[y^-, y^+]$ of y, divide it into N equal subintervals h and consider the points $y_k = y^- + kh$, $k = 0, 1, \ldots, N$. For any of the families of characteristics we find and store the ranges of v_0 variation at all these points. The results are summarized in a table having the structure shown in Fig. 20, labelled F, where F_i, $i = 1, \ldots, M$, denotes i-th fault and F_0 means fault-free circuit. In the place specified by i-th row ($i \in \{0, 1, \ldots, N\}$) and j-th column ($j \in \{0, 1, \ldots, M\}$) the ranges of v_0 variation at $y_i = y^- + ih$ in the circuit with fault F_j are stored. On the basis of this table the fault dictionary is build by selecting the rows for which the number of overlapping ranges of v_0 variation is minimalized. The details are presented in reference [36].

Example 4: Let us consider the BJT circuit shown in Fig. 21. We want to diagnose fault-free circuit (F_0) and $M = 9$ catastrophic faults: cuts of the branches DJ (F_1), BC (F_2), and short circuits of the pairs of points HI (F_3), CK (F_4), GL (F_5), AL (F_6), IL (F_7), EL (F_8), FM (F_9). To build the fault dictionary, table F of size 51×10 is created and row 0 corresponding to this table selected. It allows identifying all the aforementioned catastrophic faults [36], on the basis of the measured output voltage at the input voltage equal to y^-.

VIII. Conclusion

This paper is based on the works published recently by the authors [29], [31]-[32], [34], [36] dealing with some new aspects of fault diagnosis of nonlinear analog circuits. It presents a wide variety of diagnostic problems: soft and hard, local and global, single and multiple fault diagnosis in circuits comprising BJ and MOS transistors manufactured in micrometer and submicrometer technology. The soft fault diagnostic methodologies presented in this paper are based on DC measurements performed at a limited number of test

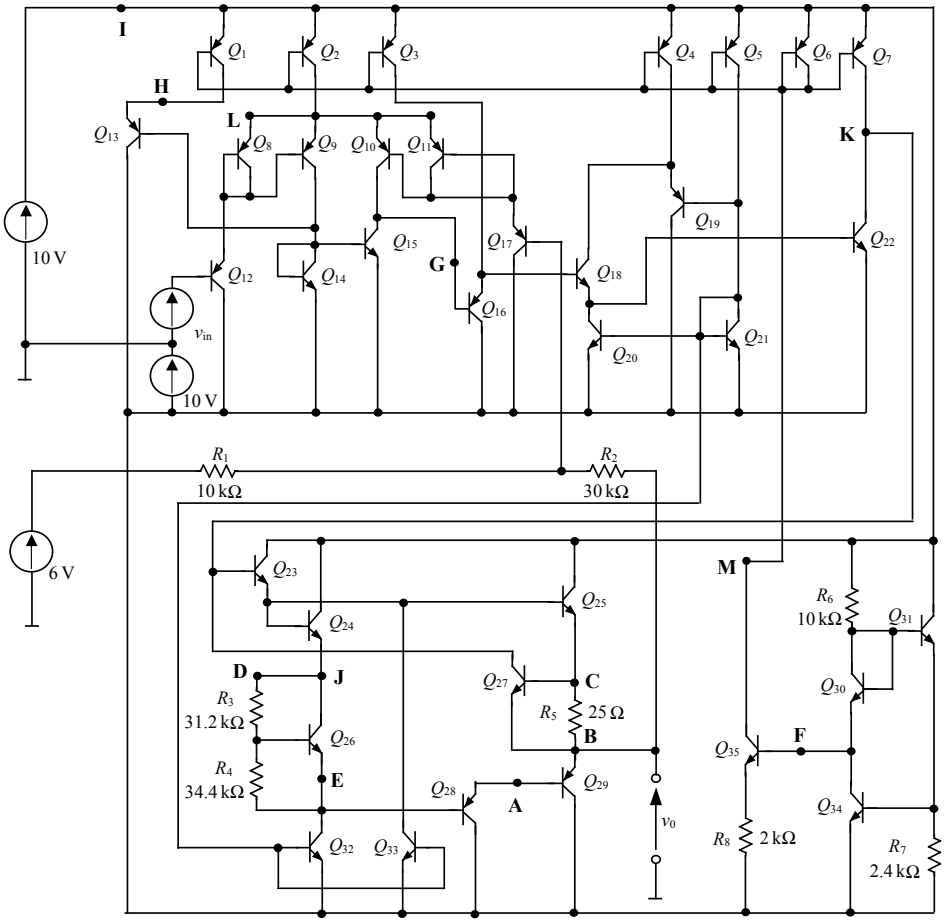

Fig. 21. Circuit for Example 4

points. They lead to a system of nonlinear algebraic test equations with the diagnosed parameters as the unknown variables, which are not given in explicit analytical form and may possess multiple solutions. All the described algorithms allow finding the multiple solutions, being the sets of the parameters that meet the test and next selecting the actual one. For this purpose the homotopy concept is used combined with: parametric representation [29], simplicial algorithm [31], and restart procedure [32]. In the case of hard fault diagnosis a class of circuits having multiple DC solutions (operating points) was considered for the first time in reference [36]. The results summarized in this paper have general meaning, because a hard fault changes the circuit topology and the new circuit may possess multiple DC solutions even if the original circuit has a unique solution. For fault diagnosis of this class of circuits a combination of the homotopy and the theory named linear complementary problem, was used. Numerical experiments including real electronic circuits show that the proposed methods allow effectively locating and identifying multiple soft faults and single hard faults. They are especially useful at the pre-production stage, where corrections of the technological process are possible and CPU time is not crucial.

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