A Single-chip Integration Approach of Switching Cells Suitable for Medium Power Applications

Abdeilah El Khadiry, Abdelhakim Bourennane, Frédéric Richardeau, Eric Imbernon, and Marie Breil

***Abstract*—This paper deals with the monolithic integration of switching cells that are used in power electronics for the realization of static power converters. The aim of the monolithic integration of the power switching cells is to suppress wire bonds in order to improve electrical performance as well as reliability of power modules intended for medium power applications. Within this context, the single chip integration approach presented in this paper constitutes a solution and a promising approach that combines judiciously multiple reverse conducting IGBT switches in a single Si-chip. The operating modes of the integrated structure are validated in an inverter application using 2D Sentaurus simulations. The targeted packaging of the single chip converter on DBC/IMS substrates doesn't use any wire bonding and doesn't exhibit any dv/dt stress directly on the DBC/IMS substrates.**

***Index Terms*—Monolithic integration, on-chip integration, power conversion, switching cells, inverter**

I. Introduction

IN the field of integration in power electronics (for low and medium power applications), different integration approaches were proposed in literature for the integration of power converters (Fig. 1). One approach is based on a monolithic series integration of inverter leg through the use of lateral power devices [1]. The other followed approach is a hybrid integration approach that uses either multiple discrete reverse-conducting IGBT (RC-IGBT[2]) chips that are interconnected using wire bonds, or by interconnecting only two complementary switching cells chips associated on a DBC substrate by wire bonds [3, 4] or by chip-on-chip stacking [5] (which is difficult to realize). In order to suppress wire bonds and to avoid chip-on-chip stacking, we propose a monolithic integration approach that uses multiple vertical RC-IGBTs to realize a single Si-chip static power converter (ac/dc or dc/ac). The monolithic architecture that we propose can be used to integrate multiple switching cells.

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II. Description of Architecture and Operation

The single chip integration approach is illustrated for the case of two switching cells. We integrate on the same Si-chip four RC-IGBTs (named RC1, RC2, RC3 and RC4) that compose the converter circuit shown in Fig. 2.

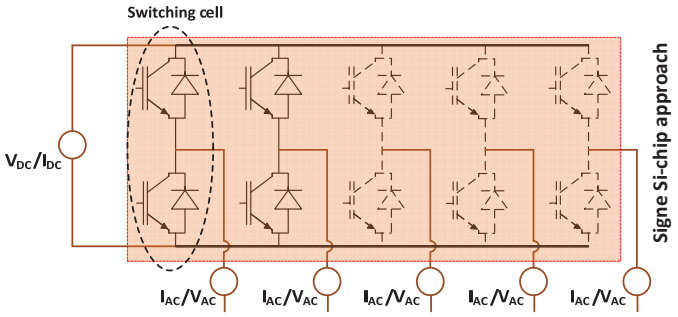


Fig. 1. Typical interleaved power converter architecture

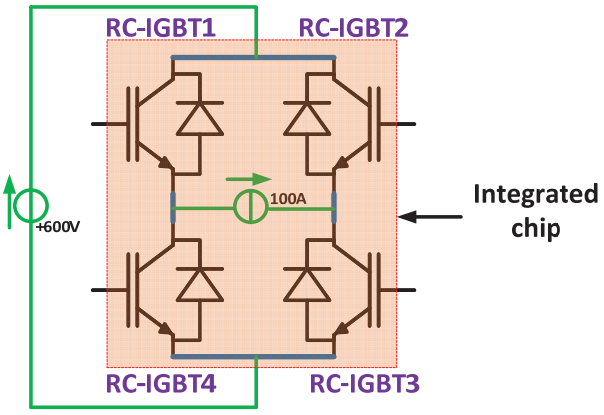


Fig. 2. The H-bridge inverter

The monolithically integrated architecture of the circuit is shown in Fig. 3a. The integration approach of the RC-IGBTs combines a quasi-parallel integration (RC1 with RC2 and RC3 with RC4) and series integration (RC2 in series with RC3 and RC1 in series with RC4). The integration of vertical RC-IGBTs requires the use of insulation regions. The insulation is achieved by reverse junctions formed by P^+ walls/N^- regions [6]. It should be noted that any line on the cross sectional view (Fig. 3a) that connects any two different electrodes indicates that those two different electrodes are at the same electrical

potential during 2D simulations. For the sake of illustration, we have represented in Fig. 3b a cross sectional view of an RC-IGBT section composed of only one MOS section on the front side. On this cross-section, we represented the different regions with their dimensions. Table I lists the geometrical and physical parameters of the different regions.

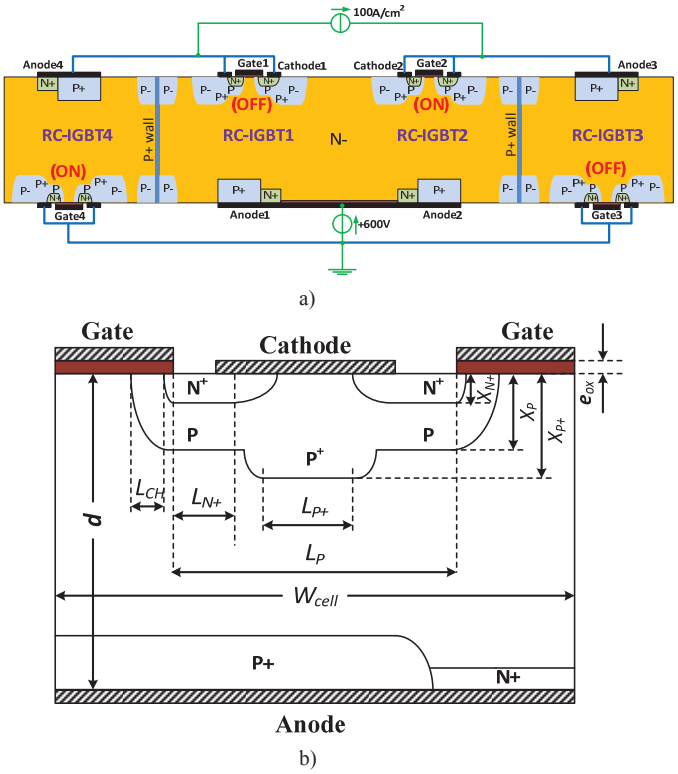


Fig. 3. a) Cross-sectional view of the simulated monolithically integrated H-bridge (equivalent to circuit of Fig. 2), the surface of each RC-GBT section is 1 cm^2 ; b) Cross-sectional view of an RC-IGBT containing for the purpose of illustration only one MOS section

TABLE I
GEOMETRICAL AS WELL AS PHYSICAL PARAMETERS OF THE DIFFERENT REGIONS

Region	Dimension (µm)	Surface concentration (cm^{-3})	Doping profil	Lateral diffusion coefficient
SiO2	L_G =30 e_{ox} =0.055	-	-	-
N-	W_{cell} =70 d =300	10^{+14}	Uniform	0.8
N+	L_{N+} =14 X_{N+} =1	10^{+20}	Gaussian	0.8
P	L_P =40 X_P =5	$2.5\times10^{+17}$	Gaussian	0.8
P+	L_{P+} =26 X_{P+} =7	$5\times10^{+19}$	Gaussian	0.8
Channel	L_{CH} =3.2	-	-	-

In Fig. 3a, we can notice that the MOS-sections of the two RC-IGBTs: RC3 and RC4 are on the backside of the chip while those of RC1 and RC2 are on the front-side of the chip. Through a judicious placement of the RC-IGBTs (RC1, RC2, RC3 and RC4), we obtain a monolithic architecture, for the converter circuit of Fig. 2, in which wire bonds are suppressed. Indeed, the interconnection between the different main power electrodes is achieved through a metal layer that could be realized on a PCB for example for the front-side of the chip and through a metal layer on the DBC/IMS for the backside of the chip. A cross-sectional view of a packaged single-chip integrated converter that shows the interconnection on the front side as well as on the backside is illustrated on Fig. 4.

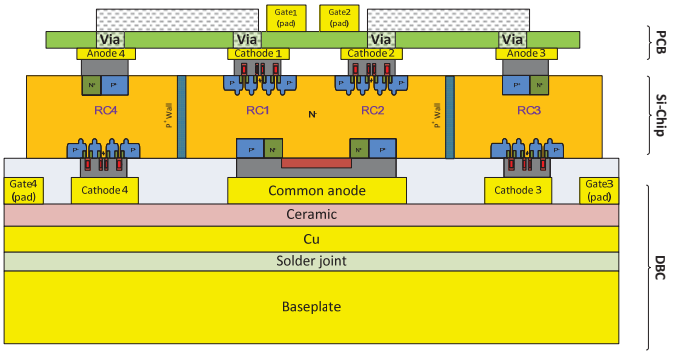


Fig. 4. A simplified cross-sectional view illustrating a packaging of the proposed monolithically integrated H-bridge converter

The advantages of this integration approach are:

- High current carrying capability: use of devices of vertical structure.
- The switching cells loops have a shorter length: as compared to the approach that uses simple discrete RC-IGBTs, the switching cell requires two sections of wire bonds whereas this approach requires only a single section of thick copper bridge on the front side of the chip. This permits the reduction of stray inductance.
- The voltage variations (dv/dt) takes place only on the front side of the chip: the suppression of voltage variations (dv/dt) on the back-side permits the suppression of the common mode current through the DBC/IMS substrate.
- The local decoupling capacitor: The electrodes that must be decoupled (anode1-anode2 and cathode3-cathode4) are close to each other in the module, that would allow the integration of ceramic SMC capacitors directly on the DBC/IMS substrate.
- Generic: The approach can allow the integration of multiple RC-IGBTs in the same chip. The converter function can be obtained by a simple adaptation of gate control signals and sources.
- Packaging steps and time reduction: a single chip is packaged.
- This approach allows to replace all of the wire bonds on the front of the chip by a PCB: the use of large and short copper tracks are less inductive and less resistive than wire bonds. In addition, PCB is mainly more economical in terms of productivity, because all of connections can be realized at the same time and the PCB can be functionalized by adding sensors, drivers ...etc.

For the purpose of explaining the monolithic converter operation, the proposed chip is set in the conditions given in Fig. 3a. For the inverter operation, we can distinguish two main operating modes: one mode corresponds to the case in which RC1 and RC3 are in the on-state while RC2 and RC4 are in the blocking state and a second mode that corresponds to the case in which RC2 and RC4 are in the on-state while RC1 and RC3 are in the off-state.

We can remark from the two operating modes that RC1 and RC2 that share the same N- drift region (see Fig. 3a) are in two different states. Indeed, in one of the two operating modes RC1 is in on-state while RC2 is in the off-state and supports the applied voltage (600V in this case). It should be noted that RC1 and RC2 are not separated from each other using a P^+ wall. In order to reduce power dissipation within RC2 (in off-state), it is mandatory to reduce the leakage current through RC2. This leakage current depends on the distance that separates RC1 which is in on-state and RC2 which is in off-state [2]. Moreover, a judicious placement of the backside diffusions (N^+ and P^+) of RC1 and RC2 contributes to the reduction of the leakage current through the section in off-state (RC2). The chosen placement of the P^+ and N^+ backside diffusions is illustrated in Fig. 3a.

III. Simulations Results

A. *Static simulations*

Sentaurus TCAD 2D-simulations [7] were used to validate the operating modes of the monolithic structure in an inverter bridge application given in Fig. 2. The simulated monolithic chip is illustrated in Fig. 3a. In order to operate the mono-chip structure as an inverter, a 600V DC voltage is applied between the two electrodes on the backside of the chip (anode1–anode2 and cathode3-cathode4) and we impose a 100 A current at the two electrodes on the front side of the chip (anode4-cathode1 and anode3-cathode2) (see Fig. 3a).

For the purpose of validating the device operating modes, the following structure parameters and conditions were adopted under Sentaurus TCAD:

- The area factor is adjusted so that each RC-IGBT section reaches a surface of 1 cm2. The effective width of each RC-IGBT section (width of P+ + width of N+) is 70 □m.
- The separation distance between RC1 and RC2 is 1 mm.
- The insulation region (wall P+) has a width of 10 µm and a doping concentration of 1020 at/cm3.
- For simulation purposes, the interconnection between the electrodes that are set to the same electrical potential is achieved simply by attributing the same electrode name to the two electrodes (that are at the same electrical potential). The connection of the current source (100 A) is achieved by placing it between the two electrodes (anode4-cathode1 and anode3-cathode2). This is illustrated in Fig. 3a.

The simulated two operating modes of the bridge inverter are:

- Mode 1: RC1 and RC3 in on-state while RC2 and RC4 in off-state (see Figures 5a and 5b).

In this operating mode, it is the IGBT part of the RC1 and RC3 sections that conduct, the leakage current in the two sections RC2 and RC4 in the blocking state are $I_{cathode}(RC2)=1.1x10^{-5}A$ and $I_{cathode}(RC4)=1.4x10^{-5}A$, respectively.

The leakage current is lower than 1/1000 of the nominal current which is clearly acceptable for the intended medium applications. The space charge region extends on both sides of the reverse biased junctions $P_{(cathode2)}/N^-$ and $P_{(cathode4)}/N^-$ as well as on both sides of the reverse P^+/N^- junctions formed by the insulation region P^+(wall) and drift region N-.

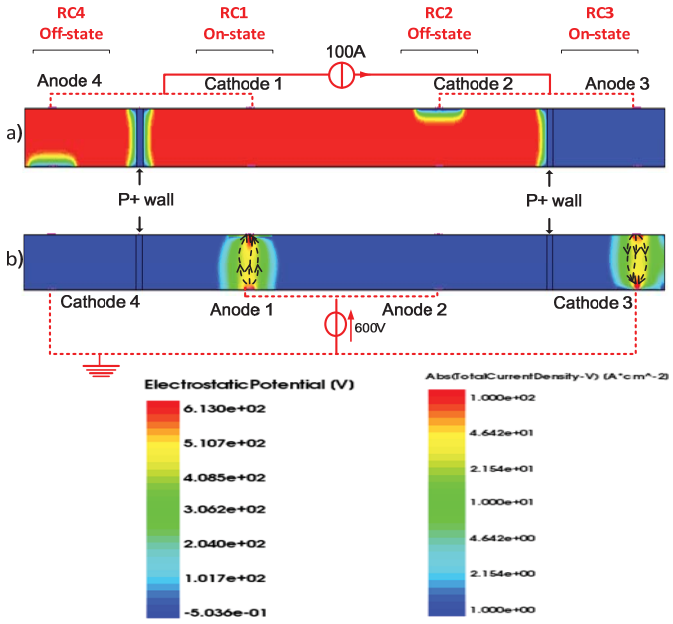


Fig. 5. 2D simulation results for mode 1 (IGBTs conduction), a) Equipotential lines distribution, b) Current flow lines distribution

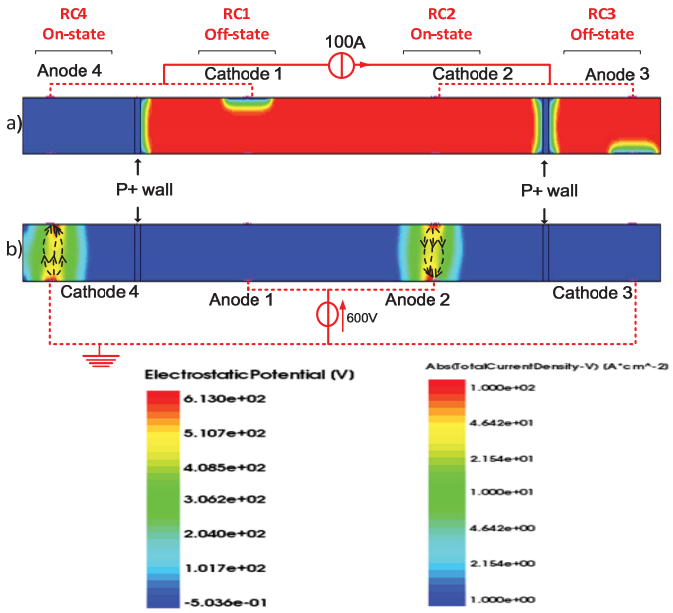


Fig. 6. 2D simulation results for mode 2 (Diodes conduction) a) Equipotential lines distribution, b) Current flow lines distribution

- Mode 2: RC1 and RC3 in off-state while RC2 and RC4 in on-state (see Fig. 6a and 6b).
  In this operating mode, it is the internal diodes of the two RC-IGBT cells RC2 and RC4 that ensure current conduction. The leakage current in the two sections RC1 and RC3 in the blocking state are Icathode(RC1)=1.2x10-5A and Icathode(RC3)=1.7x10-5A.
  The simulated leakage current is here also lower than 1/1000 of the nominal current which is acceptable for the intended medium power applications. The space charge region extends on both sides of the reverse biased junctions P(cathode1)/N- and P(cathode3)/N- as well as on both sides of the reverse P+/N- junctions formed by the insulation region P+(wall) and drift region N-.

These simulations allowed validating the static operating modes of the structure in an inverter mode over two periods. Source S1 is a DC voltage source set to 600V, the gates control voltages (Fig. 7) are generated in such a way to have a dead time where all the IGBTs of the integrated cells are blocked during a time of 1µs. The output voltage V(out)=V(S2)=±600V is given in Fig. 8.

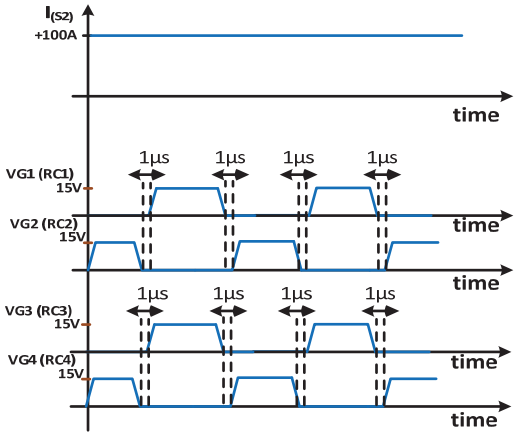


Fig. 7. Control signals for the inverter application

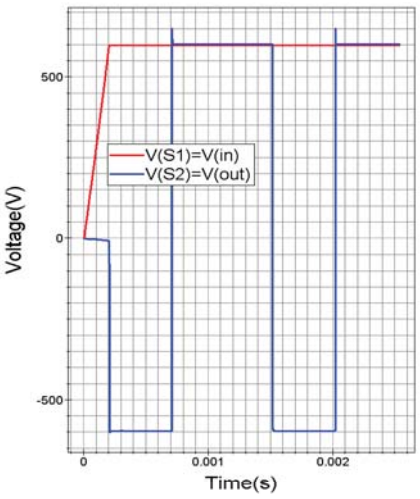


Fig. 8. Simulation result for the case of the inverter bridge V(S1)=V(in)=+600V (DC voltage source) I(S2)= +100A (DC current source) V(S2)=V(out)= ±600V

B. *Dynamic simulations*

Dynamic switching phases for the case of the IGBT conduction of the two sections RC1 and RC3 (turn-on and turn-off), and for the case of the diodes conduction of the two sections RC2 and RC4 (turn-on and turn-off) are shown in Fig. 9.

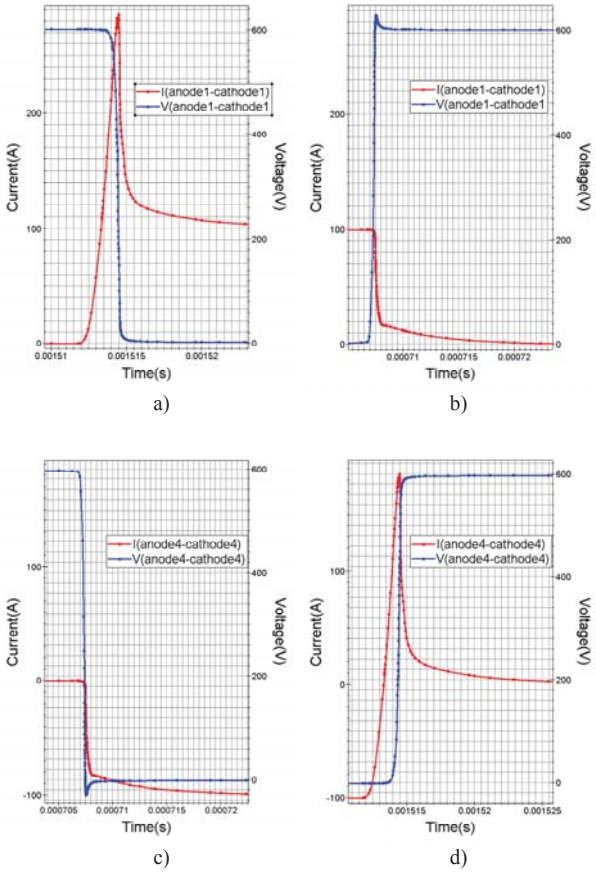
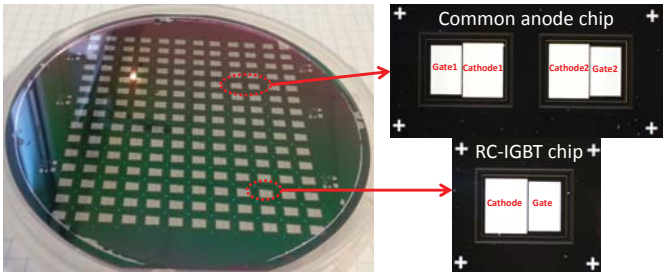


Fig. 9. Dynamic switching phases of RC1(IGBT conduction) and RC4 (diode conduction): a) RC1 turn-on, b) RC1 turn-off, c) RC4 turn-on, d) RC4 turn-off

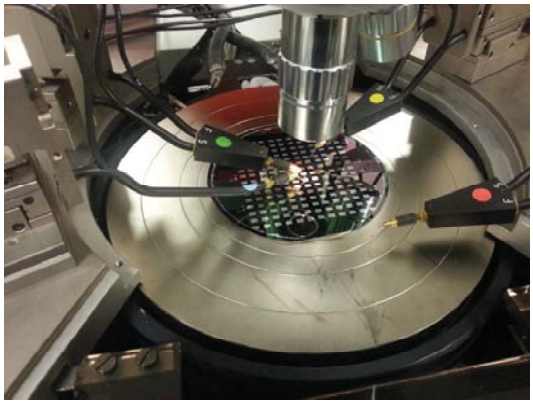
IV. Experimental Results

The technological realization of the proposed multi-poles chip requires the realization of the P^+ wall. The development of this specific technological step is being in progress, we realized the middle region of the single chip (common anode) as well as the RC-IGBT structures using the flexible IGBT technology process at the micro and nano technologies platform in the Laboratory of Analysis and Architecture of Systems (LAAS-CNRS). The starting silicon wafers are of type N and uniformly doped (10^{14} at.cm^{-3}). The wafer thickness is 300 µm.

The common anode region is composed of two RC-IGBTs: RC1 and RC2. The realized separate RC-IGBTs will be used to form the common cathode chip. The association of the common anode chip with two RC-IGBTs will allow realizing the H-bridge inverter. Fig. 10a shows the realized Si-wafer contained the common chip as well as RC-IGBTs chips. On-wafer electrical characterizations were carried-out as shown in Fig. 10b.



a)



b)

Fig. 10. Devices realization and characterization a) wafer top view, b) on-wafer electrical characterization

Fig. 11 and Fig. 12 show the forward and reverse on-state I(V) characteristics of the realized RC-IGBTs, respectively. The channel conduction of the RC-IGBT in the reverse mode is shown in Fig. 13 this propriety of this device permits the reduction of the thermal losses in switching modes. Fig. 14 shows the I(V) characteristics of the two RC-IGBT sections that compose the common anode chip for the case in which one RC-IGBT section is in on-state while the other RC-IGBT section is in off-state. It can be easily seen that the leakage current level through the RC-IGBT section in off-state is negligible as compared to the current level that flows through the RC-IGBT section which is in on-state.

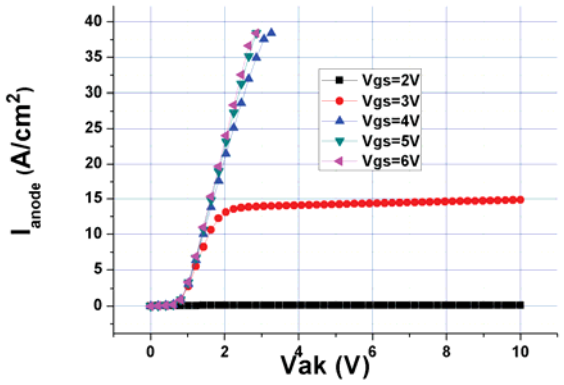


Fig. 11. RC-IGBT forward on-state I(V) characteristics

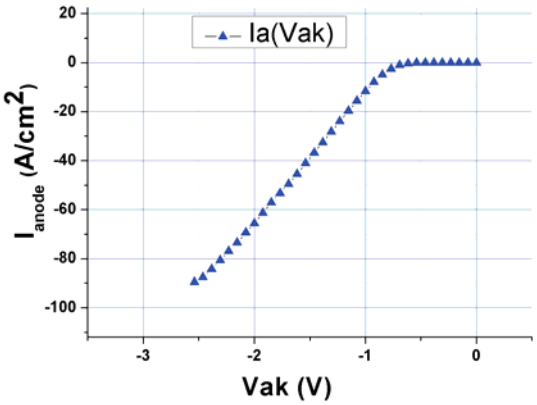


Fig. 12. RC-IGBT reverse conduction

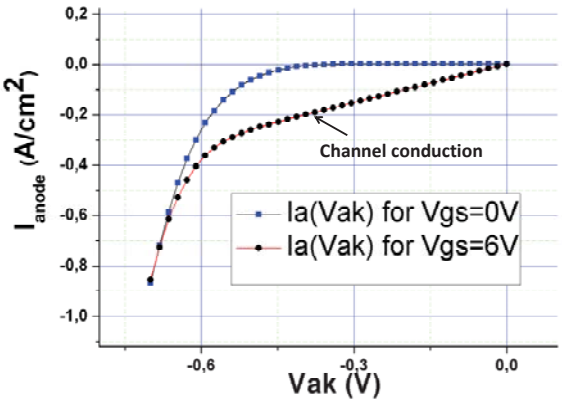


Fig. 13. Channel conduction of RC-IGBT reverse mode

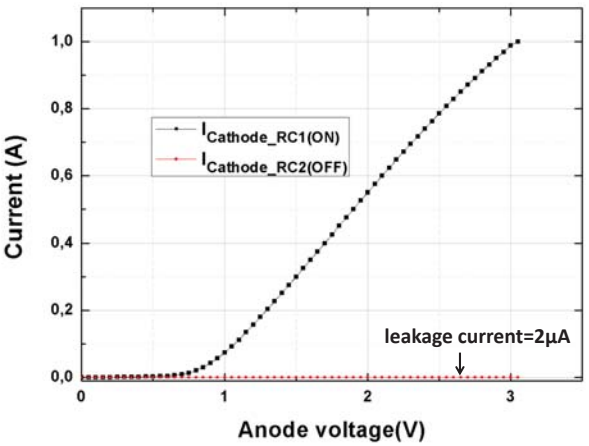


Fig. 14. Leakage current in the common anode chip when one RC-IGBT is in on-state while the other RC-IGBT is in off-state

V. Conclusion

In this paper, a monolithic structure that integrates two switching cells of an H-bridge converter dedicated for medium power applications is proposed and studied by 2D simulations. The proposed approach of integration judiciously combines in a single silicon chip vertical RC-IGBTs. This approach is interesting because it can allow to suppress wire bonds and

reduces the number of technological steps for the realization of the packaging. Indeed, Due to the fact that the power electrodes that should be interconnected are located on the same plane (front-side of the single-chip) planar conductive tracks on the same PCB substrate can be used making it possible to realize a converter module without wires bonds. Moreover, this PCB can include drivers, sensors …etc and could make possible cooling from the upper face of the chip. The PCB conductive tracks are less inductive than wire bonds. One can therefore expect improvement in the electrical performance of the single-chip converter as well as reliability.

Through 2D simulations under Sentaurus TCAD, the static and dynamic operating modes of the proposed architecture are validated in an inverter application.

The obtained experimental results validate the RC-IGBT as well as the common anode chip operating modes. It should be noted that the specific technological steps (wall P^+) for the realization of the single chip are in progress.

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