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Parallel data processing in a 3-channel integrated time-interval counter

Abstract

In this paper, we discuss an issue of parallel data processing in multichannel time interval counters (TICs). Particularly we analyze this problem within the framework of a 3-channel TIC developed for the international project Legal Time Distribution System (LTDS). The TIC provides the high measurement precision (< 15 ps) and wide range (> 1s) that are obtained by combining reference clock period counting with in-period interpolation. A measurement process consists of three main stages: (1) events registration, (2) data processing and (3) data transfer. In the event registration stage all input events are identified and registered with related unique timestamps based on a consistent time scale. To achieve high measurement precision, the stream of timestamps is then processed using actual transfer characteristics of the TIC and offset values of all measurement channels. We describe the concept of parallel data processing and its implementation in a Spartan-6 FPGA device (XC6SLX75, *Xilinx*).

Keywords: programmable device, time-to-digital converters, interpolating time counters, parallel data processing.

1. Introduction

Precise multichannel TICs are applicable in many areas such as e.g. physics experiments [1] or laser range finding systems [2]. They are particularly important in time laboratories to compare the quality of different clock sources. For such a purpose, we designed a 3-channel integrated TIC which is a part of the ongoing international project called Legal Time Distribution System (LTDS) [3]. The aim of this project is to develop a complete system able to provide a legal time scale for time-sensitive operation, e.g. bank transfers, online documents circulation synchronization, etc.

The TIC collects timestamps from up to 3 clock sources that typically generate a 10 MHz sinusoidal waveform and a 1 PPS (Pulse Per Second) signal. The measurement method is based on counting consecutive periods of the reference clock signal (T_o=2 ns) by a period counter (timestamp method) and in-period interpolation (Fig. 1). The common time scale, which is generated by the period counter, is the same for each registered event regardless of a measurement channel number. A simplified block diagram of the time counter is shown in Fig. 2.

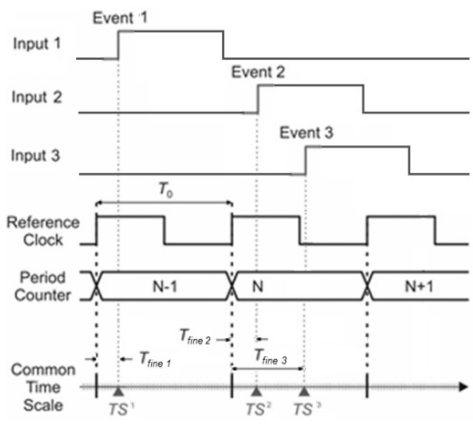

Fig. 1. Measurement method based on timestamps and interpolation

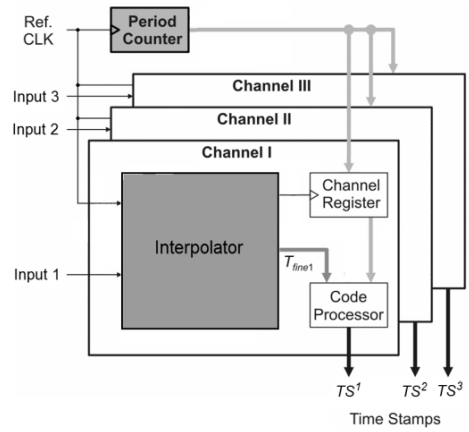

Fig. 2. Simplified block diagram of the counter

The timestamp value of the *i*-th input event is calculated from the simple equation:

$$TS^i = (N-1)T_o + T_{fine,i}\,, \tag{1}$$

where $N-1$ refers to the content of the period counter latched into a Channel Register and $T_{fine,i}$ is the result of interpolation. Calculations are made in a Code Processor based on the actual transfer characteristic of the interpolator involved. The collected timestamps constitute a valuable source of information about current instability of tested clocks.

The timestamps are collected independently for each input. That requires effective parallel processing of data. Furthermore, it is important for the end-user to have final results of measurement stored in chronological order. As a consequence, an extra effort has to be taken to first calculate timestamp values, and then sort them taking into account input offsets. Both operations are considered in the next sections.

2. Parallel data processing

Modern TICs are characterized by the high accuracy and precision, both on the level of even a few picoseconds. To achieve such high parameters, there is a need to minimize nonlinearity errors by calculating the results on the basis of the actual transfer characteristic. Besides that, each measurement channel has a different input offset due to the use of non-ideal electronic elements (variations of propagation time, comparison levels, etc.) and different lengths of signal paths. In order to obtain reliable results on the common time scale, the offsets has to be compensated. In the designed TIC both tasks are performed in a two-level code processor (Fig. 3), which is multiplied by the number of measurement channels.

The code processor creates a collection of n data stamps at the output of each measurement channel, denoted as

$$TS_n^{i*} = F^i TS_n^i + k^i, \tag{2}$$

where F^i is the transfer function of the *i*-th interpolator and k is the value of the offset. Such collections of data are then transmitted to a computer for further use by software application (for calculation of time intervals, periods, etc.). It should be pointed out that data processing may be done by the code processors implemented in an FPGA device or by the software application. We chose the first solution because it increased the measurement speed, made the counter more reliable and easier to program.

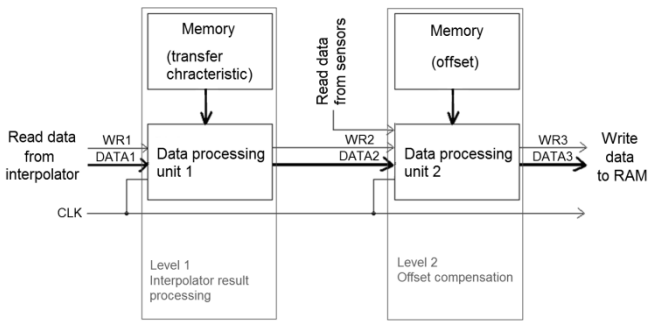

Fig. 3. The concept of two-level data processing performed in a code processor

The data resolution and its representation are crucial for data processing. These are decisive for complexity of hardware implementation and may generate an additional measurement error in case of poor resolution. We made an assumption that the interpolation part ($T_{fine,i}$) of the output data from the code processor should be represented with the resolution of about 1 ps. Then taking into account the range of interpolation (2 ns), the 11-bit word was needed ($2000/2^{11} = 0.98$ ps).

The transfer characteristics and offset compensation vectors are saved in the memory after performing calibration procedures. Given the importance of these operations on the final precision and the counter accuracy, we describe them more carefully. Obviously all calibration procedures are performed automatically under the control of the FSM (finite-state machine) unit implemented in the logical resources of the same FPGA device. Thus, the calibration data does not need to be transmitted to the computer. The calibration process can be launched on demand, especially when environmental conditions are significantly changed.

3. Transfer function of interpolators

Actual transfer characteristics of interpolators are essential for precise measurements because their precisely identified shape allows reducing the nonlinearity error of time-to-digital conversion. The most popular method to identify them is based on the statistical code density test [4]. The test is performed in two phases, i.e.: (1) bin width evaluation, and (2) transfer function evaluation [5]. In the bin width evaluation phase, the pulses of an asynchronous calibrator are digitized by the interpolator and interpolating code numbers are counted. Finally each code number is represented by the fraction of the clock period (Fig. 4a). It can be noted that the precision of this characteristic strictly depends on the number of measurements. We checked experimentally that 2 million measurements was enough.

In the transfer function evaluation phase, a table containing the transfer data of a given interpolator is calculated (Fig 4b). The FSM controller increments the address of memory corresponding to consecutive code numbers of the bin width characteristic, accumulates the sum of successively read bin width words and writes the results to the memory of the transfer function. After that all the interpolator code numbers are represented by the fractional parts of the clock period.

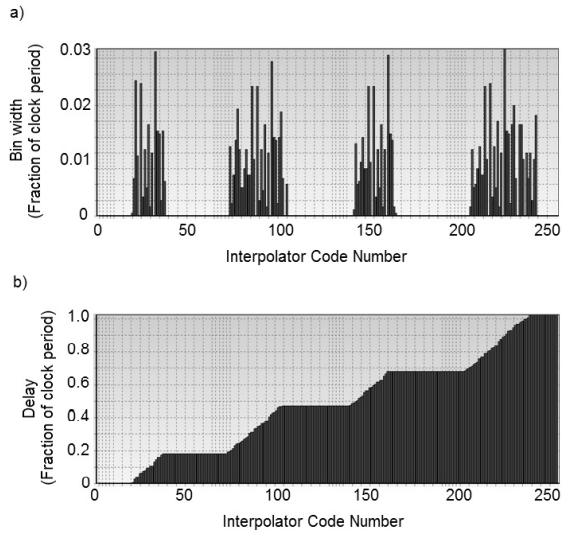

Fig. 4. Characteristics of the interpolator: a) bin width, b) transfer function

4. Offset compensation table

To adjust the common time scale to three measurement channels, the correcting values of time offsets must be known and written to the memory of the compensation table. The measurements of offsets may be made using an asynchronous calibration signal delivered to all inputs of the counter at the same time. The values of the offsets measured in such a way are satisfactory for less precise counters (precision > 10 ps). However, for more precise counters, we can observe that the offsets measured during the calibration mode may differ from the right value obtained after switching the inputs into the measurement mode. Therefore we proposed measurements of the offsets based on the use of a reference time interval (between signals START and STOP) generated by a very stable generator. We should measure this time interval using all possible variants of input configurations. The results of measurements of an example time interval $t = 4.8$ ns are given in Table 1. The obtained values of the time interval vary from 4.165 ns to 5.443 ns without compensation and from 4.797 ns to 4.811 ns after compensation.

Tab. 1. The results of measurements of the stable delay (4.8 ns) for various input configurations

Inputs configuration (START → STOP)	Measured delay *t* ns	Compensated delay *t** ns
Input 1 → Input 2	4.408321	4.804321
Input 1 → Input 3	4.164805	4.796805
Input 2 → Input 1	5.203037	4.807037
Input 2 → Input 3	4.562156	4.798156
Input 3 → Input 1	5.442554	4.810554
Input 3 → Input 2	5.045966	4.809966
Std_dev	0.49982969	0.00587284

To get the compensated values of the time interval *t**, we used the set of formulas:

$$t^*_{Ch2\to Ch1} = t_{Ch2\to Ch1} + k_{Ch2} - k_{Ch1}, \quad (3)$$

$$t^*_{Ch2\to Ch3} = t_{Ch2\to Ch3} + k_{Ch2} - k_{Ch3}, \quad (4)$$

$$\vdots$$

where $k_{Ch1}, k_{Ch2}, k_{Ch3}$ represent the offset values in channels *Ch1*, *Ch2* and *Ch3*. In our case, those values were obtained by simple calculation as follows k_{Ch1}= 1.571, k_{Ch2}= 1.175, k_{Ch3} = 0.939 with *std_dev* below 6 ps. The obtained values might be matched with the data read from external sensors (temperature, voltage), which is important for measurements provided in non-stable environmental conditions. For example, we observed that the offset value might vary even up to 200 ps with the changes of temperature within the range from –10 to 60°C.

5. Conclusions

In the designed TIC we implemented three autonomous data-processing modules, one for each measurement channel, for calculating measurement data separately and possibly fast. Moreover, thanks to the hardware implementation of calibration algorithms we also achieved the shorter execution time of calibration procedures, a considerably smaller amount of data to be transferred to the control computer, and a lower complexity of the control software. The VHDL language was employed for specification of data-processing modules. This makes them more susceptible to adapt in newly developed counters, especially with the reference to modern FPGA devices.

We implemented some untypical algorithms to decrease the developing time of the counter, such as: a verification procedure for processed data, diagnostic and control procedures for implemented operation modes, and some additional options to check the quality of made measurements. It should be emphasized that the 2-level data processing organization for full hardware implementation has not been presented in detail yet. We have studied both tasks (transfer characteristic identification and offset compensation) very carefully, however, special attention has been paid to the offset compensation, typically realized by the software.

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